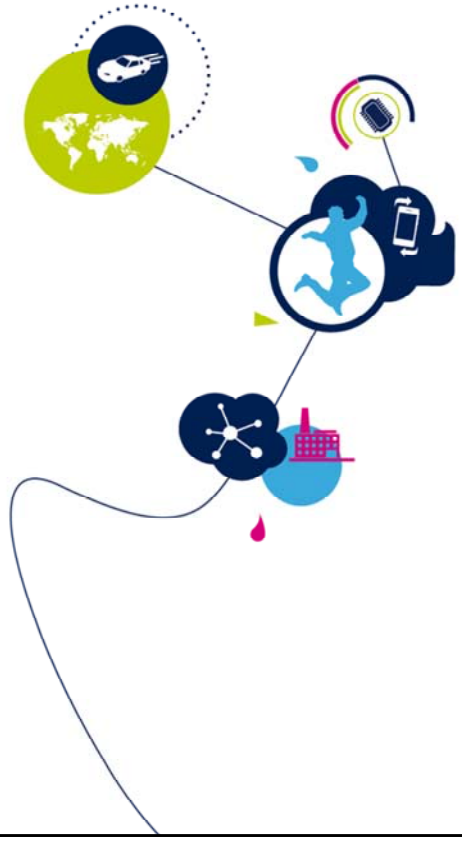
STM32MP1 - HDMI-CEC

HDMI-CEC controller
Revision 1.0



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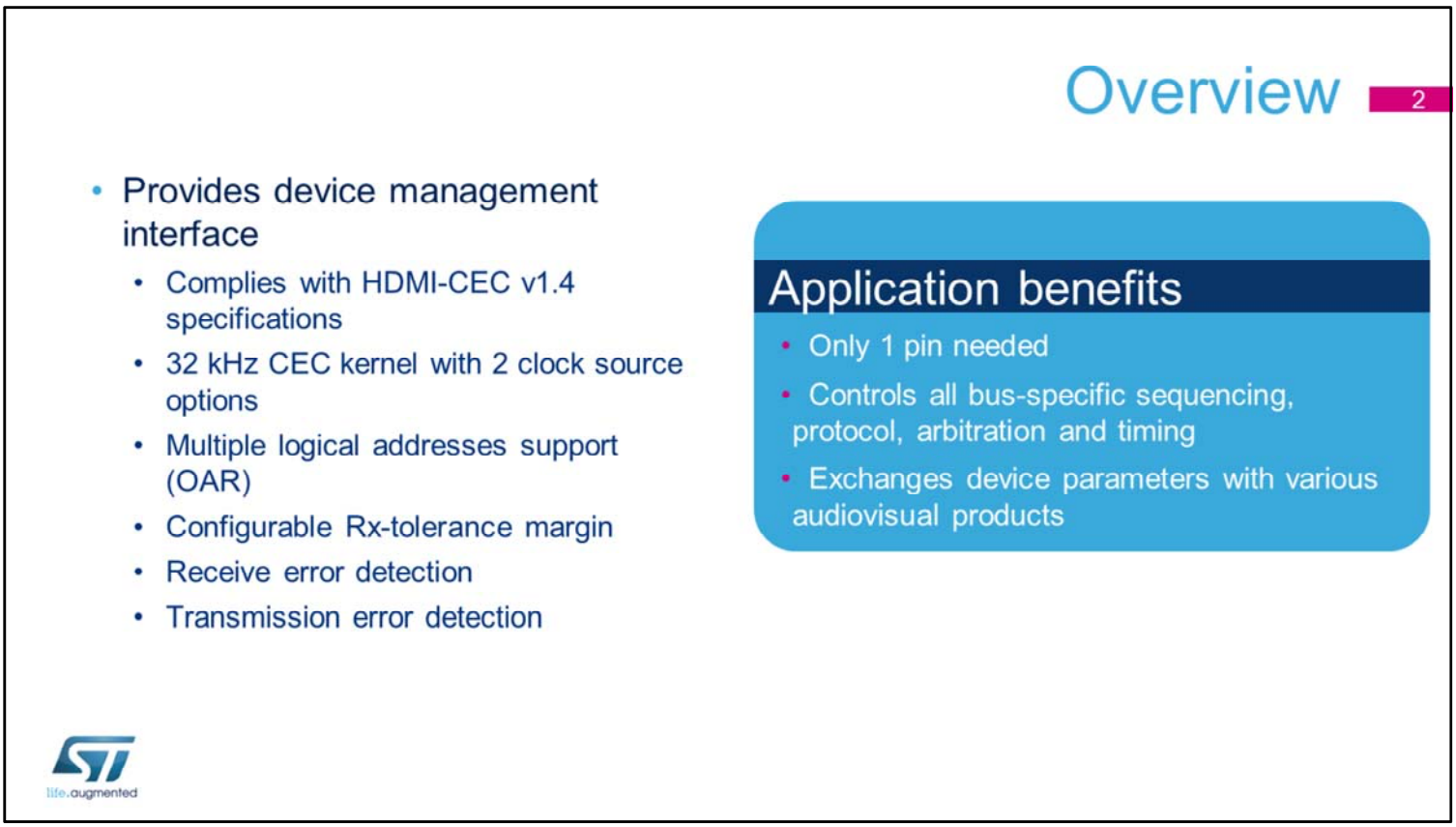
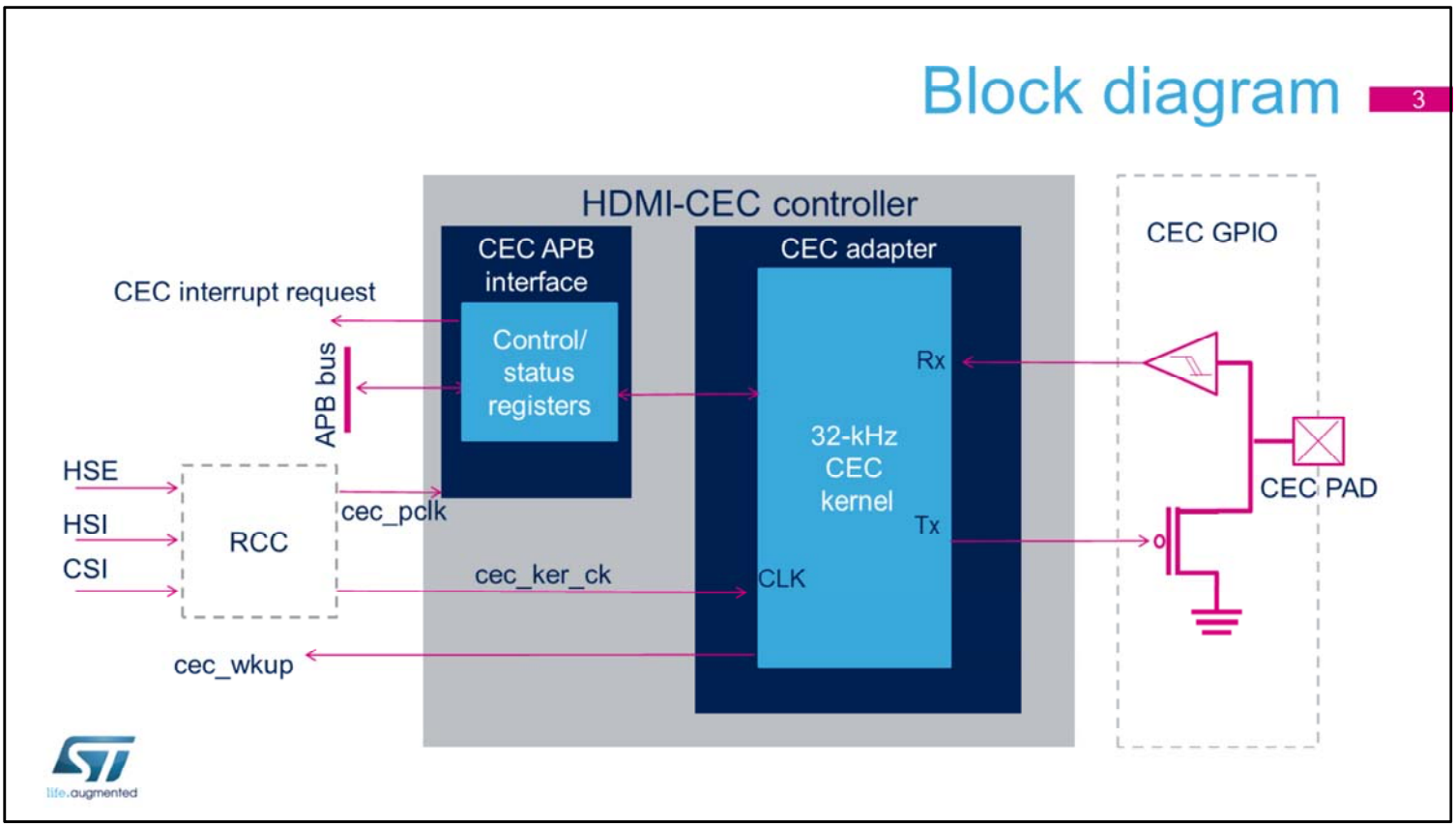
Hello, and welcome to this presentation of the STM32 HDMI-CEC controller module. It covers the main features of this controller that provides high-level control functions between all of the various audiovisual products in a user environment.



The HDMI-CEC controller integrated inside STM32 microcontrollers provides a hardware management interface allowing an STM32 to exchange device parameters with various products in a user environment.
Configurable clock sources, peripheral address and a number of received/transmission event flags are available for this.
Applications benefit from a low pin count standard interface to exchange device parameters.



HDMI-CEC stands for “High-Definition Multimedia Interface” - “Consumer Electronics Control”. The controller complies with HDMI-CEC v1.4 specifications. It provides functions needed to interface with various audiovisual products.

It consists of an “CEC Adapter" and an “CEC Advanced Peripheral Bus (APB) interface".
The “CEC adapter” provides functions such as frame decoding and checking, while the “CEC APB interface” manages the control and status registers, data in registers and data out registers and synchronous interrupt requests.

Two clocks are available for the HDMI-CEC controller, the APB clock (CEC_PCLK) for the “APB interface” and the 32-kHz Kernel clock (CEC_KER_CK) for the “CEC adapter”. The Kernel clock can be derived from HSE, CSI or HSI clock sources.

Message structure

Supported frame format

- Message:
  - single frame which consists of a start bit followed by a header block and optionally an opcode and a variable number of operand blocks.

- Header, opcode, operand blocks::
  - 8-bit payload – the most significant bit is transmitted first - followed by an end of message (EOM) bit and an acknowledge (ACK) bit.

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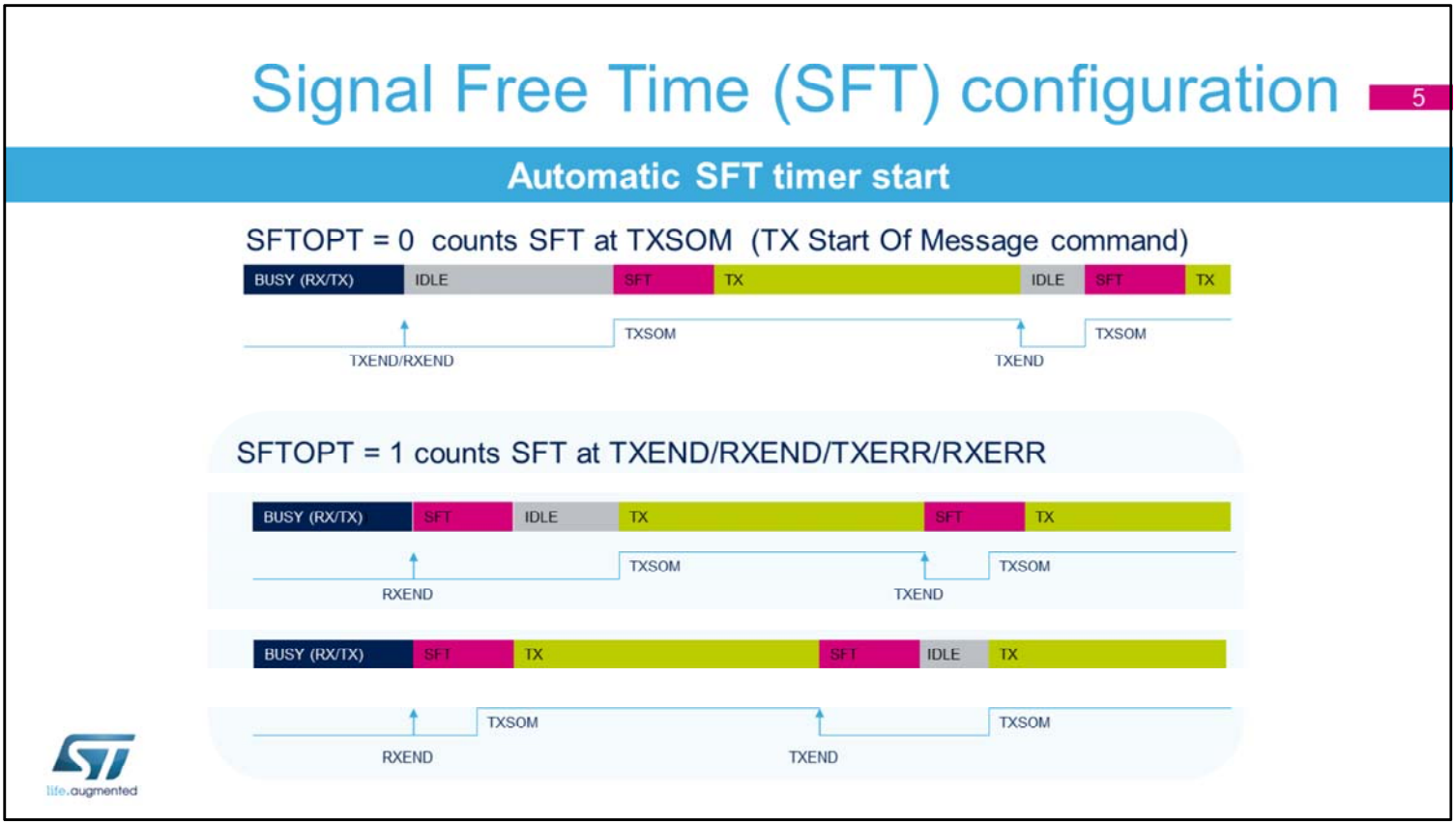
The supported frame format consists of a start bit followed by a header block and optionally an opcode and then a variable number of operand blocks.
Header, opcode, operand blocks consist of an 8-bit payload, where the most significant bit is transmitted first, followed by an end of message (EOM) bit and an acknowledge (ACK) bit.

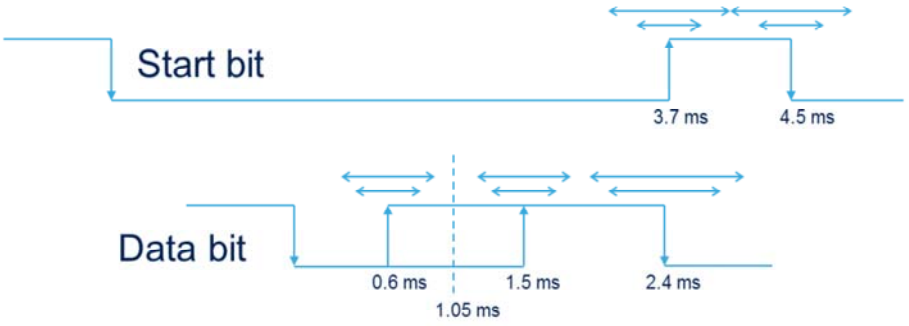


When a transmit command is sent, the HDMI-CEC sends a Start bit after the following number of nominal data bit periods of inactivity which depends on the programmed Signal Free Time (SFT) value.
In the SFT=0x0 configuration, the HDMI-CEC controller automatically calculates the SFT value, ensuring compliance with the HDMI-CEC Standard. It is also possible to configure the various fixed time.

When the SFTOPT bit is set to ‘0’, the HDMI-CEC controller starts counting the SFT value when the start-of-transmission command is set by software (bit TXSOM is set to ‘1’).
When the SFTOPT bit is set to ‘1’, the HDMI-CEC controller starts counting the SFT value when a bus-idle or line error condition is detected. If the SFT timer is completed when the TXSOM bit is set to ‘1’, the transmission starts immediately without latency.

RX tolerance margins

- RxTol bit
  - Standard tolerance (in line with CEC specification)
    - Start bit: ±200 µs rise & fall. Data bit: ± 200 µs rise, and ± 350µs fall
  - Extended tolerance
    - Start bit: ± 400 µs rise & fall. Data bit: ± 300 µs rise, and ± 500 µs fall



The HDMI-CEC controller supports two RX tolerance margin modes.
First a Standard tolerance mode in line with CEC specifications, ±200 µs on start bit rise and fall time and ± 200 µs on the rising edge of a data bit and ± 350 µs on the falling edge of a data bit.
The second mode is an Extended tolerance mode, where the timing for the Start bit is extended to ± 400 µs for rise and fall transition and ± 300 µs on the rising edge of a data bit and ± 500 µs on the falling edge of a data bit.

Errors handling

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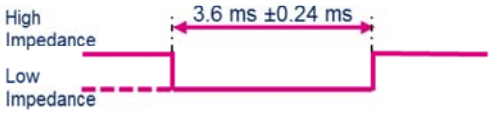
- An error is defined as a period between falling edges that is less than a minimum data bit period (i.e. too short to be a valid bit). Other timing errors are not considered in CEC specification – the user defines the action.
- The error notification (error bit) is a low period on the CEC line of 1.4 to 1.6 times the nominal data bit period, that is, 3.6 ms nominally:



- A message is considered lost and therefore may be retransmitted under the following conditions:
  - a message is not acknowledged in a directly addressed message
  - a message is negatively acknowledged in a broadcast message
  - a low impedance is detected on the CEC line when not expected (line error)

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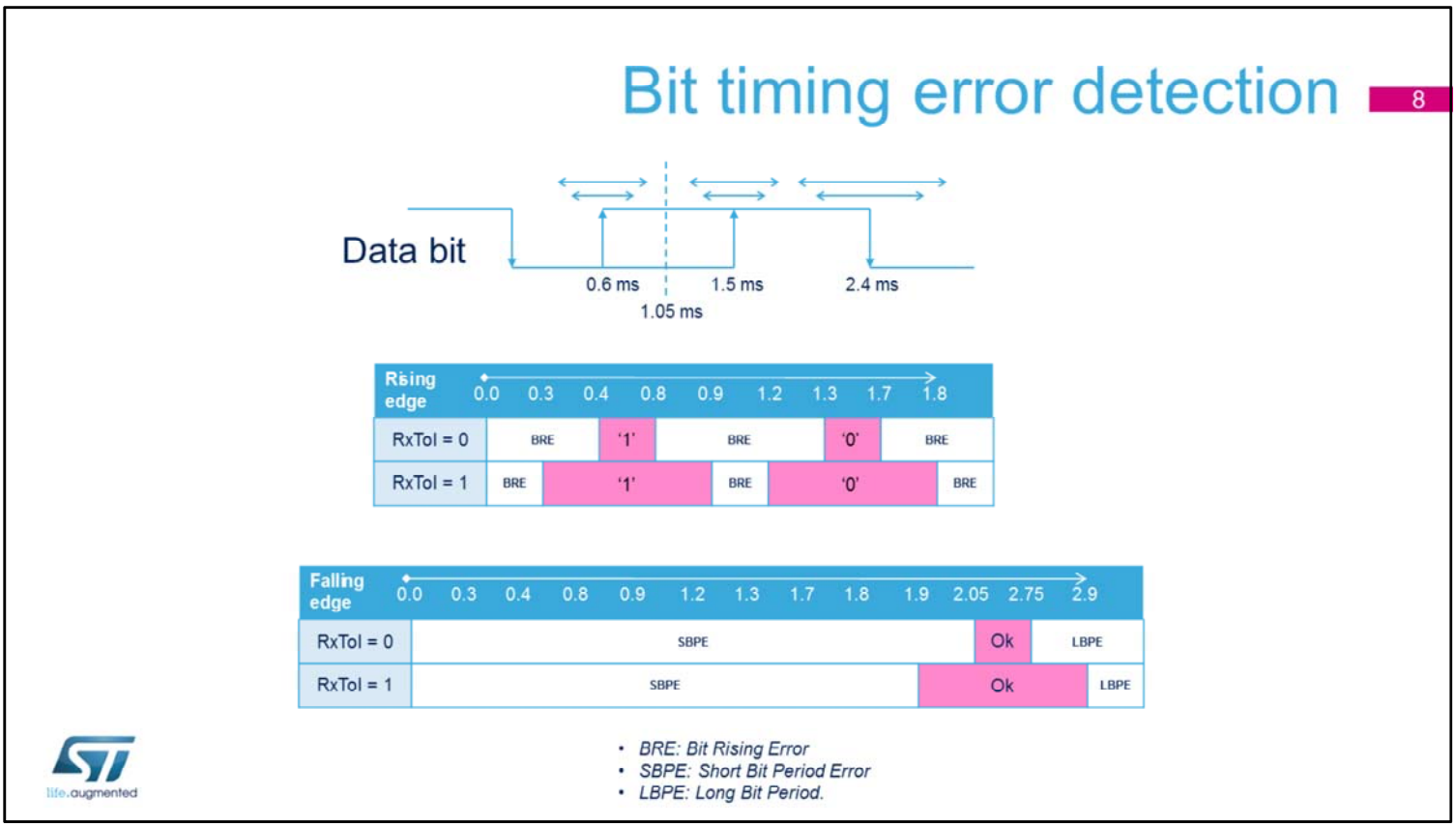
A received data bit (excluding the start bit) is considered invalid if:

- the period between the rising and the falling edge exceeds the tolerance margins as defined by the HDMI-CEC specification. In this case a Bit Timing Error (BTE) is issued.
- the period between falling edges exceeds the tolerance margins as defined by the HDMI-CEC specification. In this case a Bit Period Error (BPE) is issued.

If a BTE or BPE error is detected, the CEC peripheral notifies the other followers, and primarily the initiator, by generating an Error bit: a low period on the CEC line of 1.4 to 1.6 times the nominal data bit period, that is, 3.6 ms nominally.

A message is considered lost and therefore may be retransmitted under the following conditions:

- a message is not acknowledged in a directly addressed message,
- a message is negatively acknowledged in a broadcast message,
- a low impedance is detected on the CEC line when not expected (line error).



This slide describes the various bit timing errors during message reception:

- Bit Rising Error (BRE) is set by hardware when a rising edge is detected within a data bit outside of the Rx-windows configured by RxTol. Upon BRE detection, CEC message reception is optionally aborted if bit BRESTP is set to ‘1’ and an error bit is optionally generated on the CEC line if bit BREGEN is set to ‘1’.

- Short Bit Period Error (SBPE) is set by hardware when a falling edge is detected ending the data bit before than expected by the RxTol margin. Upon SBPE detection, an error bit is always generated on the CEC line and reception is aborted. CEC starts waiting for the next Start bit once the CEC line is idle again.

- Long Bit Period Error (LPBE) is set by hardware either when a rising or falling edge is detected after the maximum RxTol margin. Upon LBPE detection message, reception is always aborted and an error bit is optionally generated on the CEC line if LPBPEGEN is set to ‘1’.

HDMI-CEC interrupts (1/2)

Interrupt event	Description
RXBR	Rx-Byte Received
RXEND	End of reception
RXOVR	Rx-Overrun
BRE	RxBit Rising Error
SBPE	Rx-Short Bit Period Error
LBPE	Rx-Long Bit Period Error
RXACKE	Rx-Missing Acknowledge Error

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Here is an overview of HDMI-CEC reception interrupt events.
An interrupt can be produced during reception if a Receive Block Transfer is finished or if a Receive Error occurs.

HDMI-CEC interrupts (2/2)

Interrupt event	Description
ARBLST	Arbitration lost
TXBR	Tx-Byte Request
TXEND	End of transmission
TXUDR	Tx-Buffer Underrun
TXERR	Tx-Error
TXACKE	Tx-Missing Acknowledge Error

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Here is an overview of HDMI-CEC transmission interrupt events.
An interrupt can be produced during transmission if a Transmit Block Transfer is finished or if a Transmit Error occurs.

Low-power modes

System mode	Description
Run	Active.
Sleep (MPU or MCU sub-system state)	Active.
Stop + LP-Stop	The peripheral is not active but v from the HDMI-CEC controller cause the device to wake up from Stop modes on data reception.
LPLV-Stop	Not Active. The peripheral registers content is retained.
Standby	The peripheral is powered down and must be reinitialized after exiting Standby mode.

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The HDMI-CEC peripheral is active in Run and Sleep modes.
It is not active in Stop modes but interrupts from the HDMI-CEC controller cause the device to wake up from Stop modes on data reception as this peripheral has a clock domain independent from the CPU clock.
In Standby mode, the peripheral is in power-down, and it must be reinitialized after exiting Standby.

Related peripherals

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- This is a list of peripherals related to the HDMI-CEC controller. Please refer to these trainings for more information if needed.
  - Reset and clock control (RCC)
  - Interrupts (NVIC)
  - General-purpose inputs/outputs (GPIO)

Here is a list of peripherals related to the HDMI-CEC controller. Users should be familiar with all the relationships between these peripherals to correctly configure and use the HDMI-CEC interface.