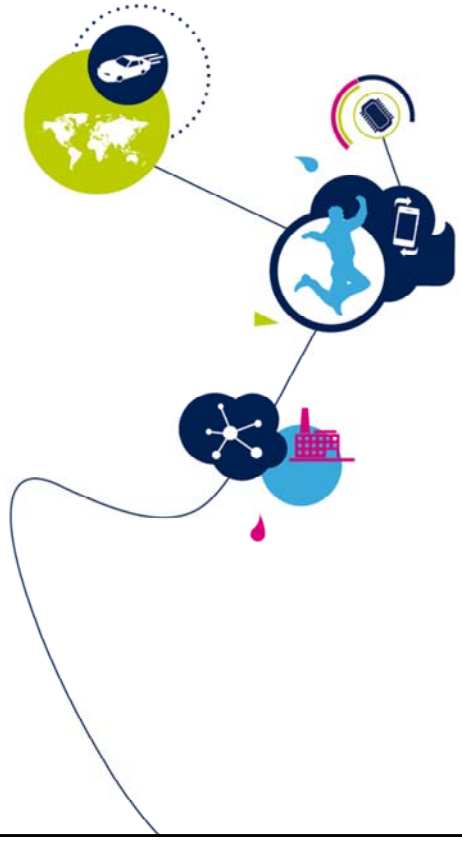
# STM32G4 - VREFBUF

Voltage Reference Buffer

Revision 1.0



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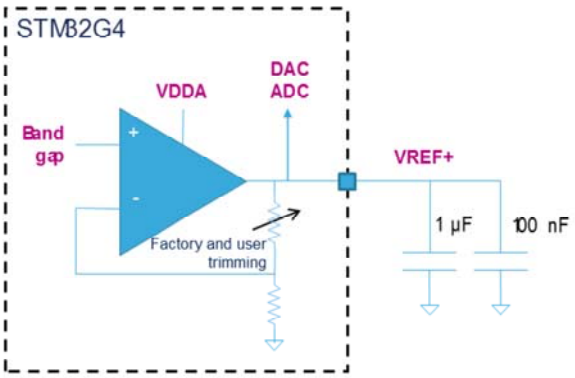
Hello, and welcome to this presentation of the STM32G4 Voltage Reference buffer.
It covers the main features of this block, which creates an on-chip reference voltage.

## Overview






- Provides an analog reference voltage
  - 2.9 / 2.5 / 2.048 V reference voltage for ADC/DAC
  - Can provide reference voltage and support external loads up to 6.5 mA with low quiescent current

### Application benefits

- Not necessary to have external reference voltage IC
- On-chip VREF generator provides VDDA-independent reference voltage

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The VREF buffer embedded in STM32G4 microcontrollers provides a stable voltage based on an internal bandgap reference for use by both the analog-to-digital and digital-to-analog converters.
Its output voltage is programmable to 2.0, 2.5 or 2.048 Volt.
This output voltage can also support external loads up to 6.5 mA.
External bulk and bypass capacitors are required when the internal VREF buffer is used.
Applications can benefit from this on-chip voltage reference as it eliminates the need for an expensive, external standalone reference voltage IC.
For space-constrained systems, it is common to use the analog supply as the reference voltage.
By using this VREF buffer instead, it can create a stable voltage even if the analog supply is changing, for

example when the VDDA supply comes from a battery output.

# Features (1/2)



- Supports 3 voltages controlled with **VRS** bit in VREF_CSR register:
  - VREFBUF_OUT1 ~= **2 .048 V**, this requires VDDA ≥ 2.40 V
  - VREFBUF_OUT1 ~= **2 .5 V**, this requires VDDA ≥ 2.80V
  - VREFBUF_OUT1 ~= **2 .9 V**, this requires VDDA ≥ 3.135 V
- Internal reference output on VREF+ pin
  - Current load up to 6.5 mA , consumption 45 µA (typ.)
- Requires external capacitance on VREF+ pin
- Not available on all packages (VREF+ double-bonded with VDDA)
- Factory and user calibrated

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Two reference voltage values can be chosen.
Each of the 3 selectable VREFBUF voltages implies a minimum value of VDDA power supply.
The VREF+ pin can deliver up to 6.5 mA.
In this case, the VREFBUF consumption from VDDA is 45 µA.
The voltage is held with the external capacitor.
In the 32-pin packages, since the VREF+ pin is double-bonded with the VDDA pin, the voltage reference buffer is not available and must be kept disabled.

# Features (2/2)



- Configuration with ENVR and HIZ bits in the VREF_CSR

| ENVR | HIZ | Configuration |
|---|---|---|
| 0 | 0 | VREF buffer OFF<br>VREF+ pin pulled-down to VSSA |
| 0 | 1 | External voltage reference mode (default):<br>• VREF buffer OFF<br>• VREF+ pin floating |
| 1 | 0 | Internal voltage reference mode:<br>• VREF buffer ON<br>• VREF+ pin connected to the VREF buffer output |
| 1 | 1 | Hold mode:<br>• VREF buffer ON<br>• VREF+ pin floating<br>➢ The voltage is held with an external capacitor |

- VRR bit is set when the output reaches the defined value

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The internal voltage reference can be configured in four different modes depending on ENVR and HIZ bits configuration.
After enabling the VREFBUF buffer by setting ENVR bit and clearing HIZ bit in the VREFBUF_CSR register, the user must wait until the VRR bit is set, meaning that the voltage reference output has reached its expected value.
When an external voltage reference is implemented, VREF+ pin is an input.
When VREFBUF is used as an internal voltage reference, it is output on VREF+ pin in order to provide this reference to external devices.

# Low-power modes



| Mode | Description |
|---|---|
| Run | Active |
| Sleep | Active |
| Low-power run | Active |
| Low-power sleep | Active |
| Stop 0/Stop 1 | Active |
| Standby | Powered-down<br>➢ The peripheral must be reinitialized after exiting Standby mode |

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The VREF Buffer is active in the following power modes: Run, Sleep, Low-power run, Low-power sleep, Stop 0 and Stop 1 modes.
In Standby and Shutdown modes, the VREF buffer is powered-down and it must be reinitialized after waking up from these modes.

## Performance



| Symbol | Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| $V_{DDA}$ | $V_{REF}$ = 2.048 | 2.4 | | 3.6 | V |
| | $V_{REF}$ = 2.5 | 2.8 | | 3.6 | V |
| | $V_{REF}$ = 2.9 | 3.135 | | 3.6 | V |
| $V_{REF\_OUT\_ERROR}$ | $V_{REF}$ = 2.048 | 2.044 | 2.048 | 2.052 | V |
| | $V_{REF}$ = 2.5 | 2.496 | 2.500 | 2.504 | V |
| | $V_{REF}$ = 2.9 | 2.896 | 2.900 | 2.904 | V |
| $I_{LOAD}$ | Max. load current | | | 6.5 | mA |
| $I_{VDDA}$ | $I_{LOAD}$ = 0 µA | | 16 | 25 | µA |
| | $I_{LOAD}$ = 500 µA | | 18 | 30 | µA |
| | $I_{LOAD}$ = 4 mA | | 35 | 50 | µA |
| | $I_{LOAD}$ = 6.5 mA | | 45 | 80 | µA |
| PSRR | DC | 40 | 55 | | dB |
| $t_{START}$ | $C_{LOAD}$ = 1.1 µF | | 500 | 650 | µs |

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This table shows certain performance parameters for the VREF buffer.
The VREF buffer can work from 2.4 to 3.6 Volt for a 2.048 Volt output, 2.8 to 3.6 Volt for a 2.5 Volt output and 3.135 to 3.6 Volt for a 2.9 Volt output.
The quiescent current is very small even with a 6.5 mA output current.
It is possible to disable the VREF buffer when it is not being used.
It can be available again 500 microseconds after it is re-enabled.
The DC Power supply rejection is 55 dB.

# Related peripherals

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- Refer to these trainings linked to this peripheral for more information:
  - Analog-to-digital converter (ADC)
  - Digital-to-analog converter (DAC)

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The STM32G4's analog-to-digital and digital-to-analog converters use this VREF Buffer output.
Please refer to the training modules for these peripheral for additional information.