Hello, and welcome to this presentation of the ARM® Cortex® -M4 Core.
In addition to the main Cortex® -M4 CPU, the STM32WB microcontroller embeds a Cortex® -M0+ core. The Cortex® -M4 core benefits from the powerful performance of its 32-bit processor architecture and particularly high level of deterministic processing while the Cortex® -M0+ core manages the real-time radio operations.
Based on the ARM Cortex-M4 core, the STM32WB series doubles the DSP capability of a single cycle DSP MAC for data processing and the single-precision FPU performance. In addition to the radio control capability offered by the ARM® Cortex® -M0+ core, the STM32WB offers more control performance and enhanced execution determinism.
Many application domains can benefit from the dual-core architecture of the STM32WB devices.
The Cortex®-M4 in the STM32WB microcontroller offers support for 8 independent memory regions, with independent configurable attributes for:

- Access permission: read/write allowed or not in privileged/unprivileged mode,
- Execution permission: executable region or region prohibited for instruction fetch,
- And cache policies that affect ART accelerator instruction cache behavior.

Memory protection unit

- MPU attribute settings affect ART accelerator instruction cache behavior
- 8 independent memory regions
  - Cache On / Off?
  - Can execute code?
  - Unprivileged mode access?
For more details, please visit the ARM website on which you can find all information about the Cortex-M4 core.