Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the microcontroller.
General-purpose IO pins of STM32 microcontrollers provide an interface with the external environment. This configurable interface is used by the MCU and also all other embedded peripherals to interface with both digital and analog signals. Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.
General-purpose I/Os provide bidirectional operation – input and output – with an independent configuration for each I/O pin. They are shared across up to 7 ports named GPIOA to GPIOF, 16 I/O pins per port and GPIOG, 11 I/O pins. All pins support external interrupt and wake-up capabilities. Atomic bit set and bit reset operations are supported through BSRR and BRR registers. Independent configuration for each I/O pin is possible.

GPIOx directly connected to AHB2 bus

Most I/O pins are 5 V tolerant.

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Key features

- Bi-directional operation of up to 6x16+11=107 (1) I/O pins
  - Shared across up to 7 GPIO ports
    - GPIOA to GPIOF, 16 I/O pins per port
    - GPIOG, 11 I/O pins
  - All pins support external interrupt and wake-up capabilities
  - Atomic bit set and bit reset using BSRR and BRR registers
  - Independent configuration for each I/O pin

- GPIOx directly connected to AHB2 bus

- Most I/O pins are 5 V tolerant

*: depends on part numbers and packages

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Most of the I/O pins are 5 V tolerant.
General-purpose I/O pins can be configured into several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input with optional pull down.
An I/O pin could be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 ranges to ensure the best compromise between maximum speed and emissions from the I/O switching and to adjust the application’s EMI performance.
I/O pins are also used by other integrated peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.
The configuration of the I/O ports can be locked to increase application robustness. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.
Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment. Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to the I/O pin at a single time. Of course, this selection can be changed during run time of the application through the GPIOx_AFRL and AFRH registers.
The configuration of any IO pin is achieved through 4 registers: GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR.

- Register GPIOx_MODER selects the functionality of the IO pin: digital input, digital output, digital alternate function or analog.
- Register GPIOx_OTYPER is relevant when the pin is an output: it selects open drain vs push-pull operation.
- Register GPIOx_OSPEEDR selects the speed of the signal received or transmitted by the pin.
- Register GPIOx_PUPDR enables /disables pull-up and pull-down resistors.
During and after reset, the alternate functions are not active, only debug pins can be used in Alternate Function mode.

JTAG/Serial Wire Debug pins remaining in alternate function configuration mode are listed in this slide.
Special considerations for HSE/LSE pins

- Oscillator pins can be used as standard I/O pins

- When the oscillator is switched OFF, related pins behave as I/O pins
  - Valid for both HSE / LSE
  - This state is the default one after reset

- When user external clock mode is used, the second pin behaves as an I/O pin
  - Only OSC_IN or OSC32_IN is used as clock source
  - OSC_OUT and OSC32_OUT are standard I/O pins

When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after a device reset.

When the external clock source is used instead of a crystal oscillator, only the related OSC_IN pin is used for the clock and the OSC_OUT pin can be used as a standard I/O pin.
This slide explains the legend and abbreviations used in the pinout table present in the STM32G4 data sheet. FT means Five Volt tolerant and TT means Three Volt tolerant.

A suffix further describes the IO pin:

- _a means analog
- _c means USB Type-C Power Delivery capable
- _d means USB Type-C PD Dead Battery function
- _f means Fast mode plus capable.

For instance, a FT_fa pin is 5 volt tolerant, supporting an analog configuration and also a digital configuration with fast mode plus.
I/O pins remain active in all modes except Standby and Shutdown, where the only available configuration is input with internal pull-up, pull-down resistor or floating input. When exiting Shutdown mode, the I/O configuration is lost.
When the MCU is under reset, I/O pins are forced into an analog input mode.
When the microcontroller is unpowered, it still presents the “dead battery” Rd pull-down, provided that UCPD_DBCC1 and UCPD_DBCC2 pins are each connected to UCPD_CC1 and UCPD_CC2 pins respectively.

Since JTAG TRST and UCPD_CC2 are multiplexed on the PB4 pin, it is not possible to use JTAG and dead battery signaling at the same time.

For non dead battery applications, JTAG is available on the condition that PB4 state is not pulled down. This can be achieved by either pulling down the DBCC2 pin or connecting an external pull-up on PB4.

Software can disable the dead battery signaling by setting the UCPD1_DBDIS bit in the PWR_CR3 register.
PB8 may be used as boot pin (BOOT0) or as a GPIO. Depending on the nSWBOOT0 bit in the user option byte, it switches from the input mode to the analog input mode:
- After the option byte loading phase if nSWBOOT0 = 1,
- After reset if nSWBOOT0 = 0.

So PB8_BOOT0 is not a dedicated pin. It can be used during reset time to select the boot mode and can become a general purpose I/O during the run-time.

PB8 GPIO is available by default, because the production value of the nSWBOOT0 option bit is 0.
PG10 may be used as reset pin (NRST) or as a GPIO. Depending on the NRST_MODE bits in the user option byte, it switches to those mode:

- Reset input/output: default at power-on reset or after option bytes loading NRST_MODE = 3,
- Reset input only: after option bytes loading NRST_MODE = 1,
- GPIO PG10 mode: after option bytes loading NRST_MODE = 2.

Reset input/output is available by default, because the production value of the NRST_MODE option bits is 3.
This table shows the differences with the STM32L4 microcontroller. Analog with pull-down is a configuration which is supported the STM32G4, but not by the STM32L4. Note that the STM32G4 also supports the analog mode without pull-down. The purpose of this analog + pull-down capability is to force a low level on the pin when the external analog line is disconnected, in order to avoid a floating state.
For more details about the System Configuration module, refer to the reference manual for STM32G4 microcontrollers. Refer also to these trainings for more information if needed:

- USB Type-C™ Power Delivery (UCPD)
- Debug (DBG)