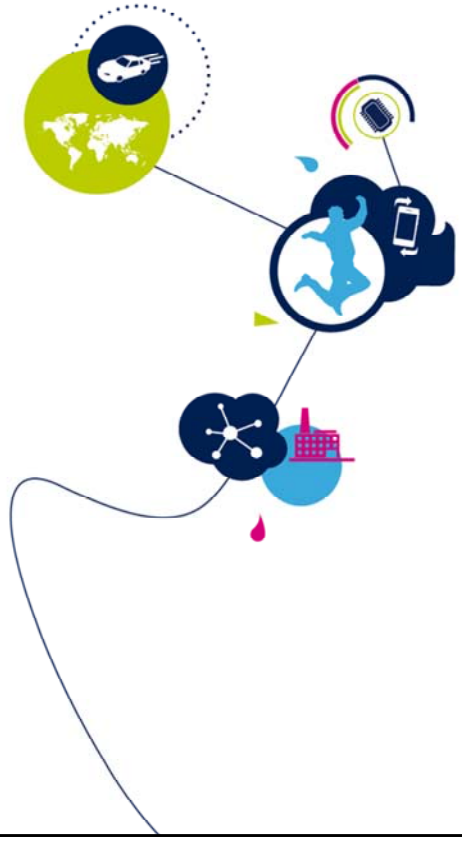
STM32G4 - GPIO

General-purpose input/output interface
Revision 1.0



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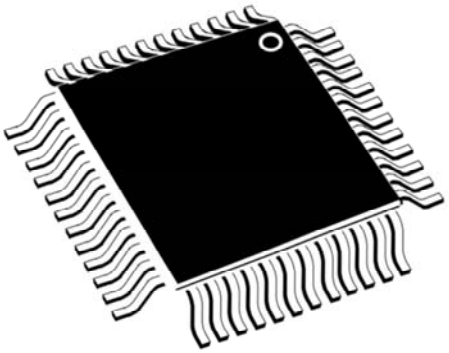
Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the microcontroller.

Overview



- Provides interface for interaction with external environment
  - Fully configurable
  - With interrupt and wake-up capability

Application benefits

- Direct microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to AHB2 allows fast toggle/sampling response

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General-purpose IO pins of STM32 microcontrollers provide an interface with the external environment. This configurable interface is used by the MCU and also all other embedded peripherals to interface with both digital and analog signals.
Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.

Key features

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- Bi-directional operation of up to 6x16+11=107 (1) I/O pins
  - Shared across up to 7 GPIO ports
    - GPIOA to GPIOF, 16 I/O pins per port
    - GPIOG, 11 I/O pins
  - All pins support external interrupt and wake-up capabilities
  - Atomic bit set and bit reset using BSRR and BRR registers
  - Independent configuration for each I/O pin
- GPIOx directly connected to AHB2 bus
- Most I/O pins are 5 V tolerant

(1) : depends on part numbers and packages

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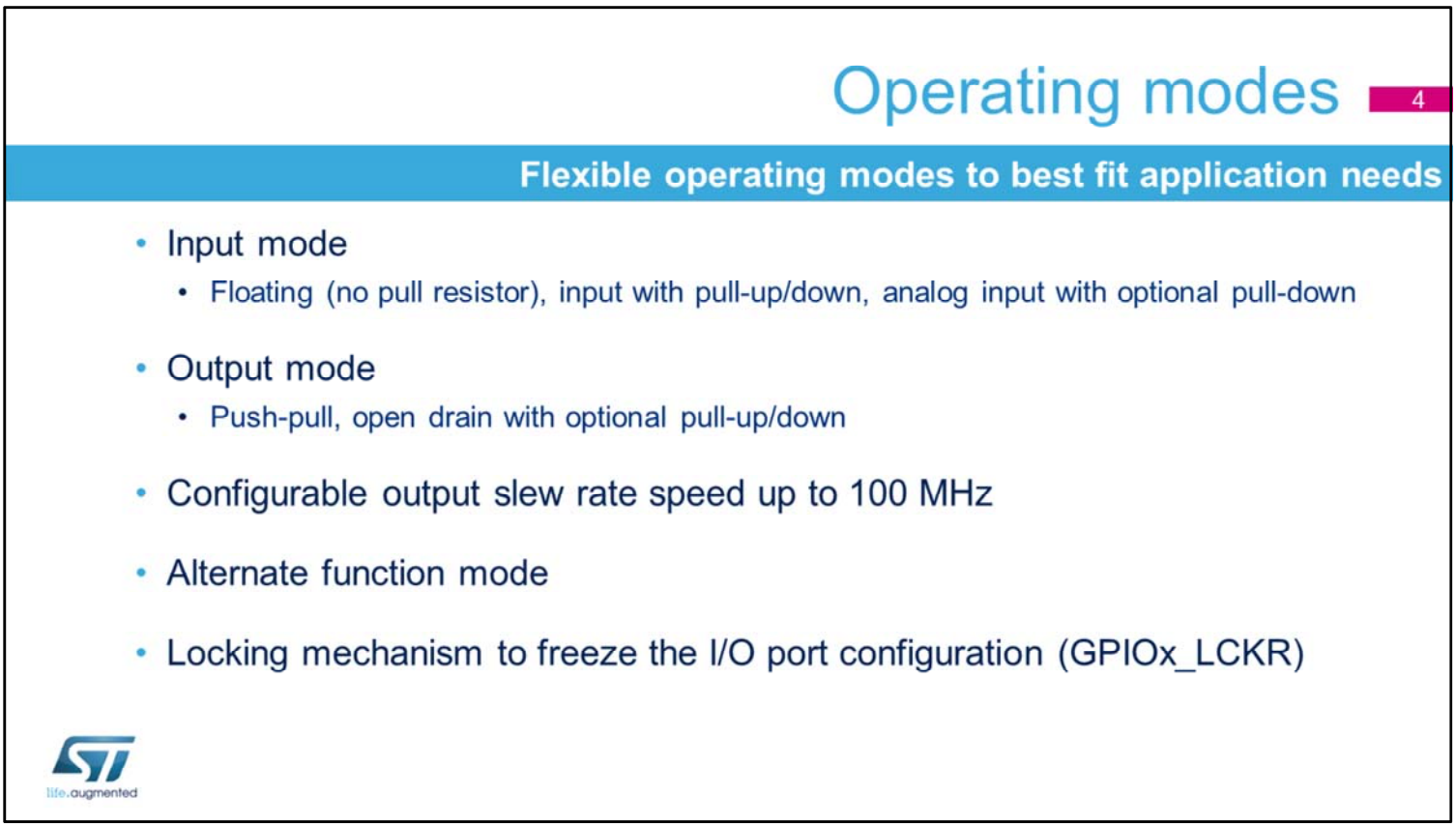
General-purpose I/Os provide bidirectional operation – input and output – with an independent configuration for each I/O pin. They are shared across up to 7 ports named GPIOA to GPIOG.
Each of them hosts up to 16 I/O pins, except the 11 I/O pins port G.
I/O ports support atomic bit set and reset operations through BSRR and BRR registers.
I/O ports are directly connected to the AHB2 bus, in order to allow fast I/O pin operations capable of changing every two clock cycles.
Most of the I/O pins are 5 V tolerant.



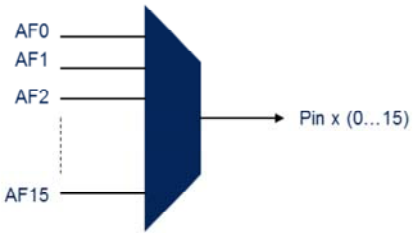
General-purpose I/O pins can be configured into several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input with optional pull down.
An I/O pin could be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 ranges to ensure the best compromise between maximum speed and emissions from the I/O switching and to adjust the application's EMI performance.
I/O pins are also used by other integrated peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.

The configuration of the I/O ports can be locked to increase application robustness. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.

Alternate functions

Structure of I/O pins is used as interface by other embedded peripherals

- Several integrated peripherals share the same I/O pins
  - For instance USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, …
- Alternate function multiplexer selects the peripheral connected to the I/O pin
  - Only one alternate function is connected to a specific I/O pin at a single time
  - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers (x = A…G)



Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment.
Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to the I/O pin at a single time. Of course, this selection can be changed during run time of the application through the GPIOx_AFRL and AFRH registers.

IO pin configuration

MODE(i)[1:0]	OTYPE(i)	PUPD(i)[1:0]	I/O configuration	
0b01	0	0b00	General Purpose output	Push-Pull
	0	0b01		Push-Pull + Pull-Up
	0	0b10		Push-Pull + Pull-Down
	0	0b11	Reserved	
	1	0b00	General Purpose output	Open-Drain
	1	0b01		Open-Drain + Pull-Up
	1	0b10		Open-Drain + Pull-Down
	1	0b11	Reserved (GP output Open-Drain)	
0b10	0	0b00	Alternate Function	Push-Pull
	0	0b01		Push-Pull + Pull-Up
	0	0b10		Push-Pull + Pull-Down
	0	0b11	Reserved	
	1	0b00	Alternate Function	Open-Drain
	1	0b01		Open-Drain + Pull-Up
	1	0b10		Open-Drain + Pull-Down
	1	0b11	Reserved	
0b00	x	0b00	Input	Floating
	x	0b01		Pull-Up
	x	0b10		Pull-Down
	x	0b11	Reserved (input floating)	
0b11	x	0b00	Input/output	Analog
	x	0b01	Reserved	
	x	0b10	Input/output	Analog, Pull-Down
	x	0b11	Reserved	

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The configuration of any IO pin is achieved through 4 registers: GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR.

- Register GPIOx_MODER selects the functionality of the IO pin: digital input, digital output, digital alternate function or analog.
- Register GPIOx_OTYPER is relevant when the pin is an output: it selects open drain vs push-pull operation.
- Register GPIOx_OSPEEDR selects the speed of the signal received or transmitted by the pin.
- Register GPIOx_PUPDR enables /disables pull-up and pull-down resistors.

Special considerations for I/O pins

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions are not active
  - I/O ports default to analog mode
  - Saves current consumption during and after reset (Schmitt trigger is off)
- Only JTAG/SWD debug pins remain in Alternate Function pull-up/pull-down configuration
  - PA13: JTMS/SWDIO
  - PA14: JTCK/SWCLK
  - PA15: JTDI
  - PB3: JTDO
  - PB4: NJTRST

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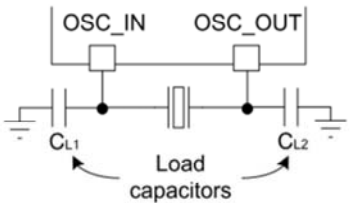
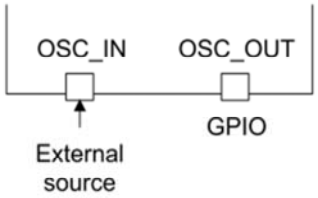
During and after reset, the alternate functions are not active, only debug pins can be used in Alternate Function mode.
JTAG/Serial Wire Debug pins remaining in alternate function configuration mode are listed in this slide.

Special considerations for HSE/LSE pins

Oscillator pins can be used as standard I/O pins

- When the oscillator is switched OFF, related pins behave as I/O pins
  - Valid for both HSE / LSE
  - This state is the default one after reset
- When user external clock mode is used, the second pin behaves as an I/O pin
  - Only OSC_IN or OSC32_IN is used as clock source
  - OSC_OUT and OSC32_OUT are standard I/O pins





When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after a device reset.
When the external clock source is used instead of a crystal oscillator, only the related OSC_IN pin is used for the clock and the OSC_OUT pin can be used as a standard I/O pin.

Multi-supply I/O pins

Legend/abbreviations used in the pinout table

- FT: 5 V tolerant I/O, TT: 3.6 V tolerant I/O
- Option for TT or FT I/Os:

Abbreviation suffix	Description
_a	I/O, with Analog switch function supplied by VDDA
_c	I/O, USB Type-C™ PD capable
_d	I/O, USB Type-C™ PD Dead Battery function
_f	I/O, Fast mode + capable

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This slide explains the legend and abbreviations used in the pinout table present in the STM32G4 data sheet.
FT means Five Volt tolerant and TT means Three Volt tolerant.
A suffix further describes the IO pin:

- _a means analog
- _c means USB Type-C Power Delivery capable
- _d means USB Type-C PD Dead Battery function
- _f means Fast mode plus capable.

For instance, a FT_fa pin is 5 volt tolerant, supporting an analog configuration and also a digital configuration with fast mode plus.

Low-power modes

Mode	I/O Description
Run	Active
Sleep	
Low-power run	
Low-power sleep	
Stop 0	
Stop 1	
Standby	I/Os can be configured with internal pull-up, pull-down or floating in Standby mode
Shutdown	I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode
Reset	Forced to analog input mode when the MCU is under reset

I/O pins remain active in all modes except Standby and Shutdown, where the only available configuration is input with internal pull-up, pull-down resistor or floating input.
When exiting Shutdown mode, the I/O configuration is lost.
When the MCU is under reset, I/O pins are forced into an analog input mode.

Special considerations for I/O pins

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- The voltage level on the UCPD DBCC lines (PA9/PA10) enables a pull down on the CC lines (PB6/PB4 respectively)
  - For dead battery applications: only SWD can be used
    - It is not possible to use the JTAG due to the pull down on PB4
  - For non dead battery applications, JTAG is available by either pulling low the DBCC2 pin (PA10) or connecting an external pull up on PB4
- The pull down effect on the CC lines can be removed by using the bit **UCPD1_DBDIS** (USB Type-C™ and Power Delivery Dead Battery disable) in the PWR_CR3 register

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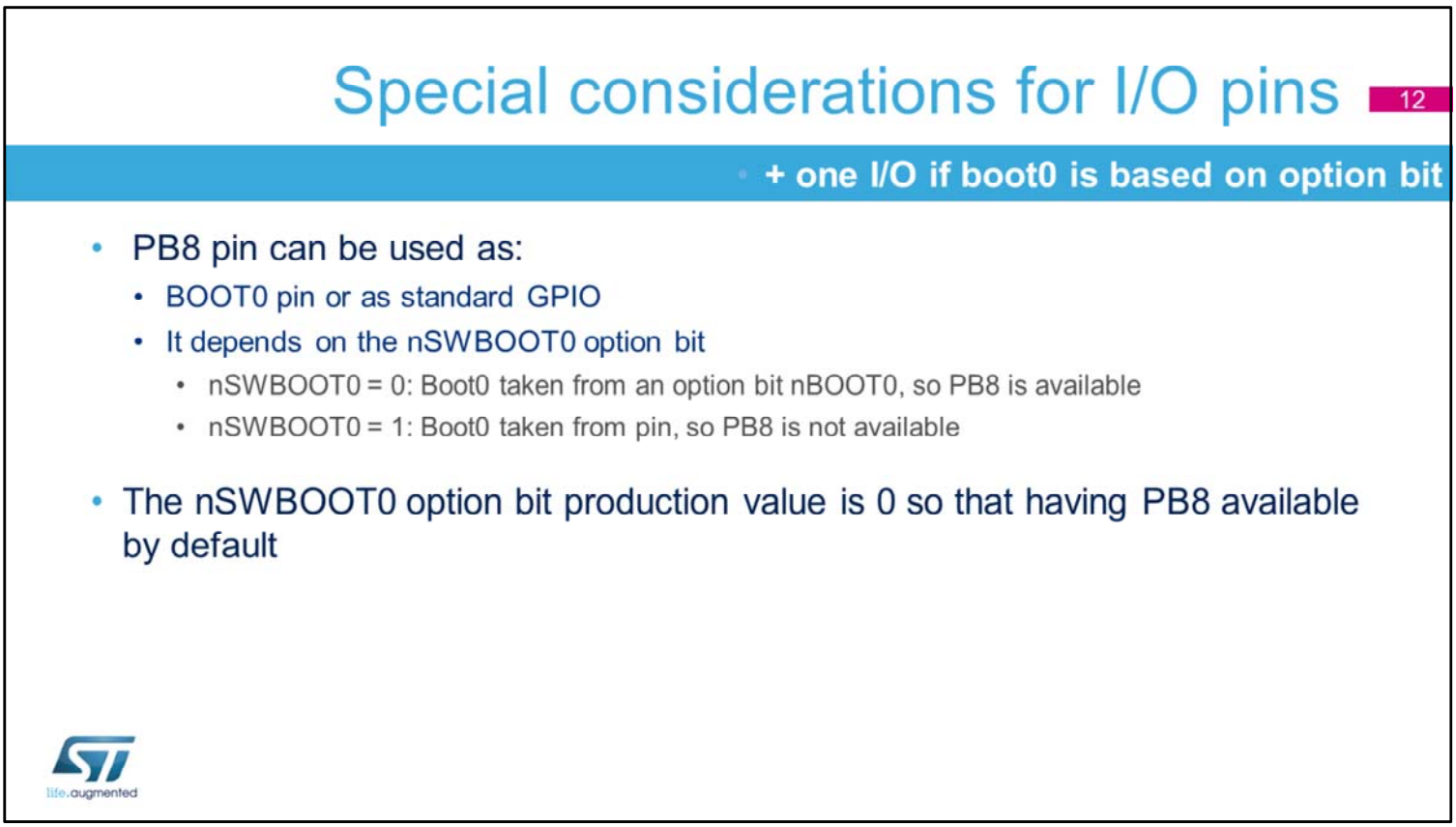
When the microcontroller is unpowered, it still presents the “dead battery” Rd pull-down, provided that UCPD_DBCC1 and UCPD_DBCC2 pins are each connected to UCPD_CC1 and UCPD_CC2 pins respectively.
Since JTAG TRST and UCPD_CC2 are multiplexed on the PB4 pin, it is not possible to use JTAG and dead battery signaling at the same time.
For non dead battery applications, JTAG is available on the condition that PB4 state is not pulled down. This can be achieved by either pulling down the DBCC2 pin or connecting an external pull-up on PB4.
Software can disable the dead battery signaling by setting the UCPD1_DBDIS bit in the PWR_CR3 register.



PB8 may be used as boot pin (BOOT0) or as a GPIO. Depending on the nSWBOOT0 bit in the user option byte, it switches from the input mode to the analog input mode:

• After the option byte loading phase if nSWBOOT0 = 1,
• After reset if nSWBOOT0 = 0.

So PB8_BOOT0 is not a dedicated pin. It can be used during reset time to select the boot mode and can become a general purpose I/O during the run-time.
PB8 GPIO is available by default, because the production value of the nSWBOOT0 option bit is 0.

Special considerations for I/O pins

NRST shared with PG10

- PG10 pin can be used as:
  - NRST or as standard GPIO
  - It depends on the NRST_MODE option bits
- The NRST_MODE option bits production value is 3 corresponding to Input/Output reset pin NRST (Legacy)
  - Thus PG10 is not by default available

PG10 may be used as reset pin (NRST) or as a GPIO. Depending on the NRST_MODE bits in the user option byte, it switches to those mode:
• Reset input/output: default at power-on reset or after option bytes loading NRST_MODE = 3,
• Reset input only: after option bytes loading NRST_MODE = 1,
• GPIO PG10 mode: after option bytes loading NRST_MODE = 2.
Reset input/ouput is available by default, because the production value of the NRST_MODE option bits is 3.

Differences with STM32L4

- Same as STMG32L4 with one difference:
  - In STM32L4, when the GPIO is configured in analog mode, the pull up/pull down are disabled by hardware
  - In STM32G4, when the GPIO is configured in analog mode it becomes possible to enable/disable the pull down, so the combination PUPD = 0b10 is no more reserved
    - The pull up remains disabled by hardware
  - Safety reason: external analog line disconnection

MODE(i)[1:0]	OTYPE(i)	PUPD(i)[1:0]	I/O configuration	
0b11	x	0b00	Input/output	Analog
	x	0b01	Reserved	
	x	0b10	STM32L4: Input/output	Reserved
			STM32G4: Input/output	Analog, Pull Down
	x	0b11	Reserved	

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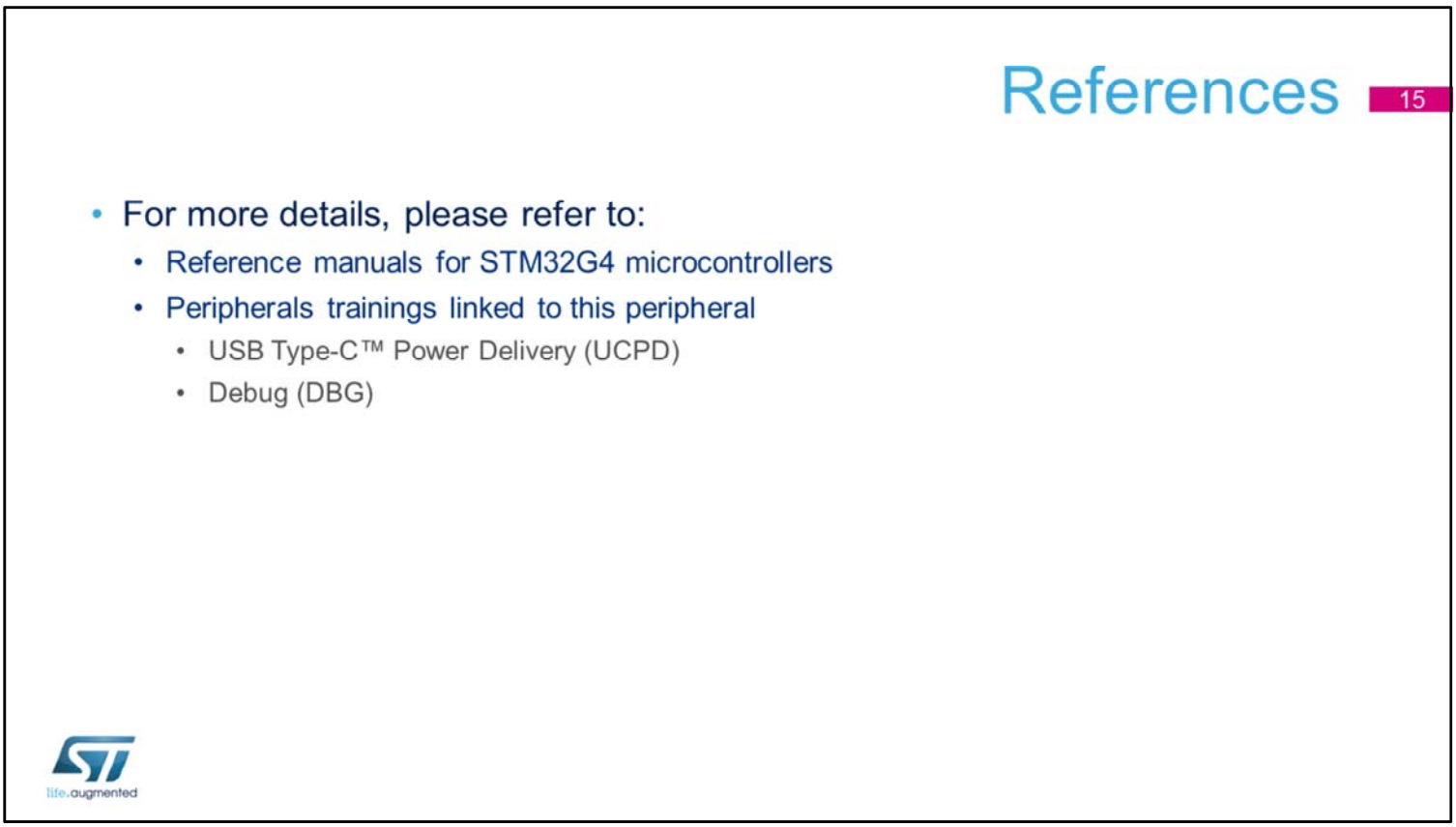
This table shows the differences with the STM32L4 microcontroller.
Analog with pull-down is a configuration which is supported the STM32G4, but not by the STM32L4.
Note that the STM32G4 also supports the analog mode without pull-down.
The purpose of this analog + pull-down capability is to force a low level on the pin when the external analog line is disconnected, in order to avoid a floating state.



For more details about the System Configuration module, refer to the reference manual for STM32G4 microcontrollers.
Refer also to these trainings for more information if needed:

- USB Type-C Power Delivery (UCPD)
- Debug (DBG)