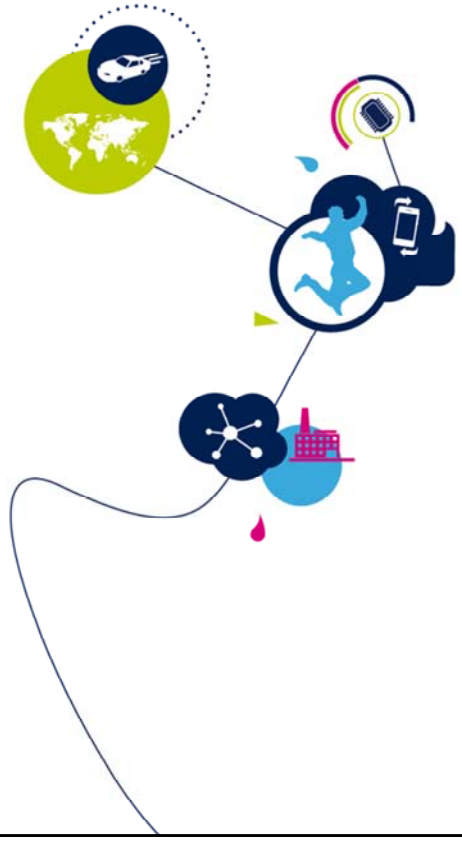
STM32MP1 - DAC

Digital-to-Analog Converter
Revision 0.1



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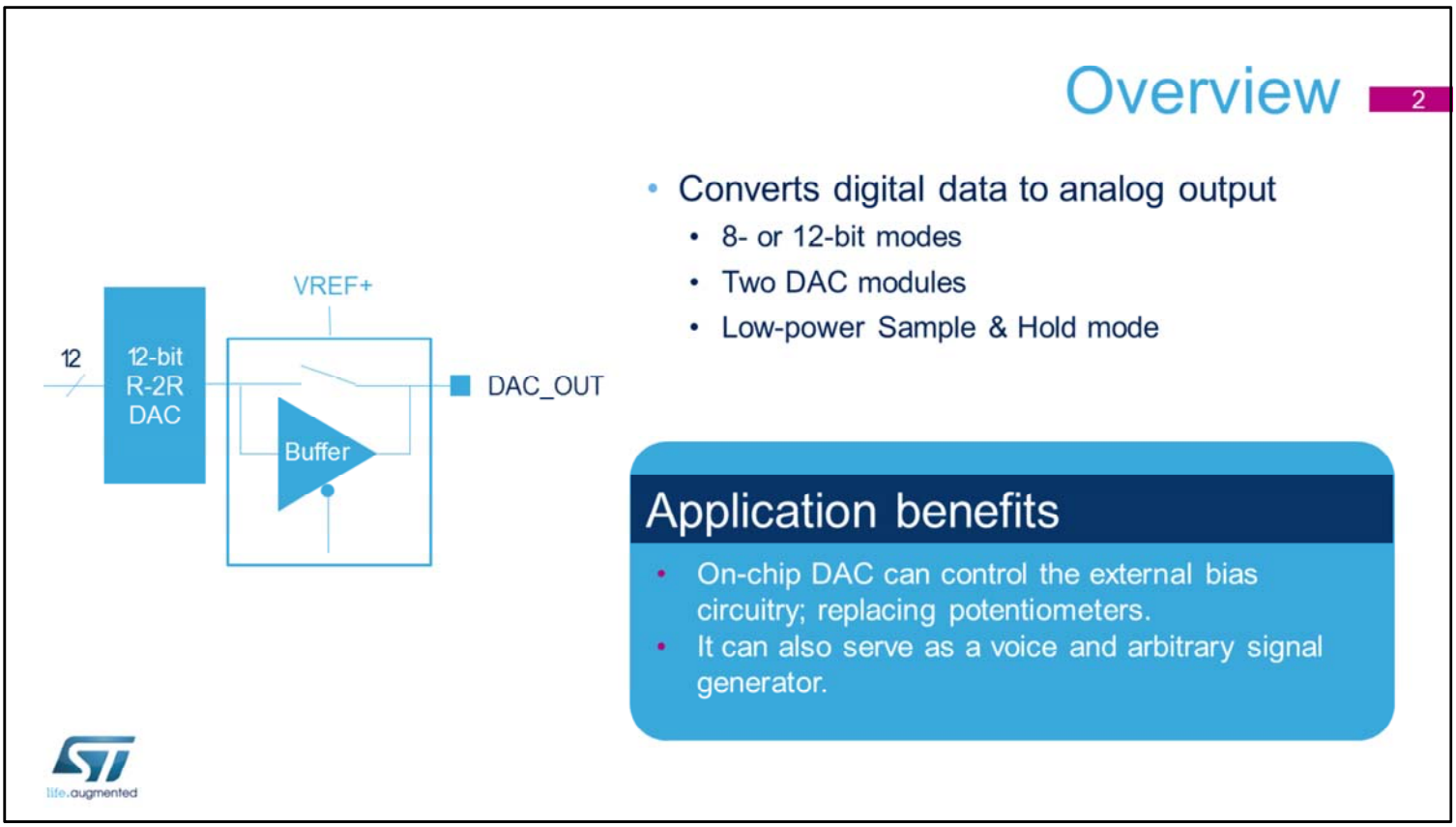
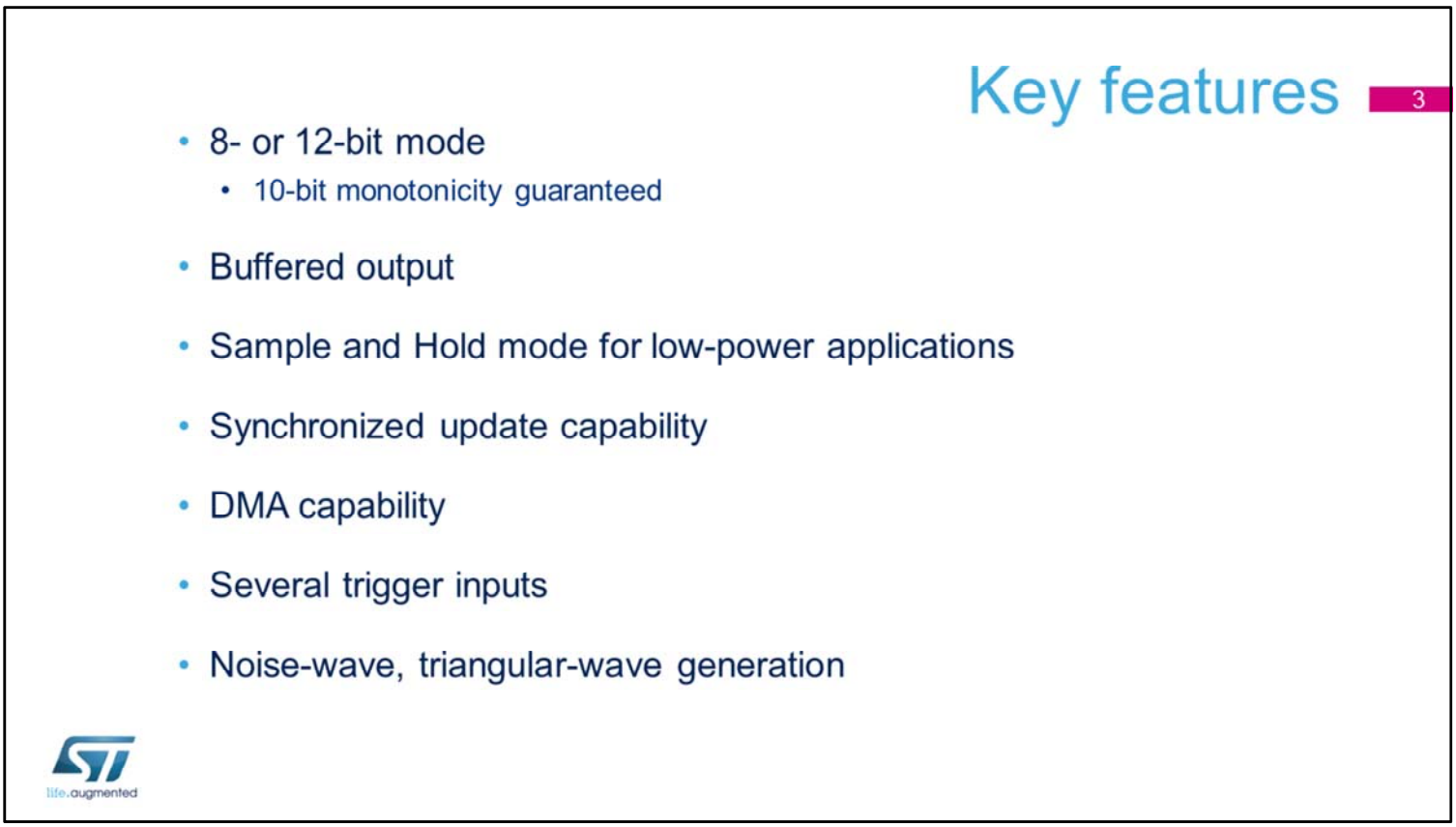
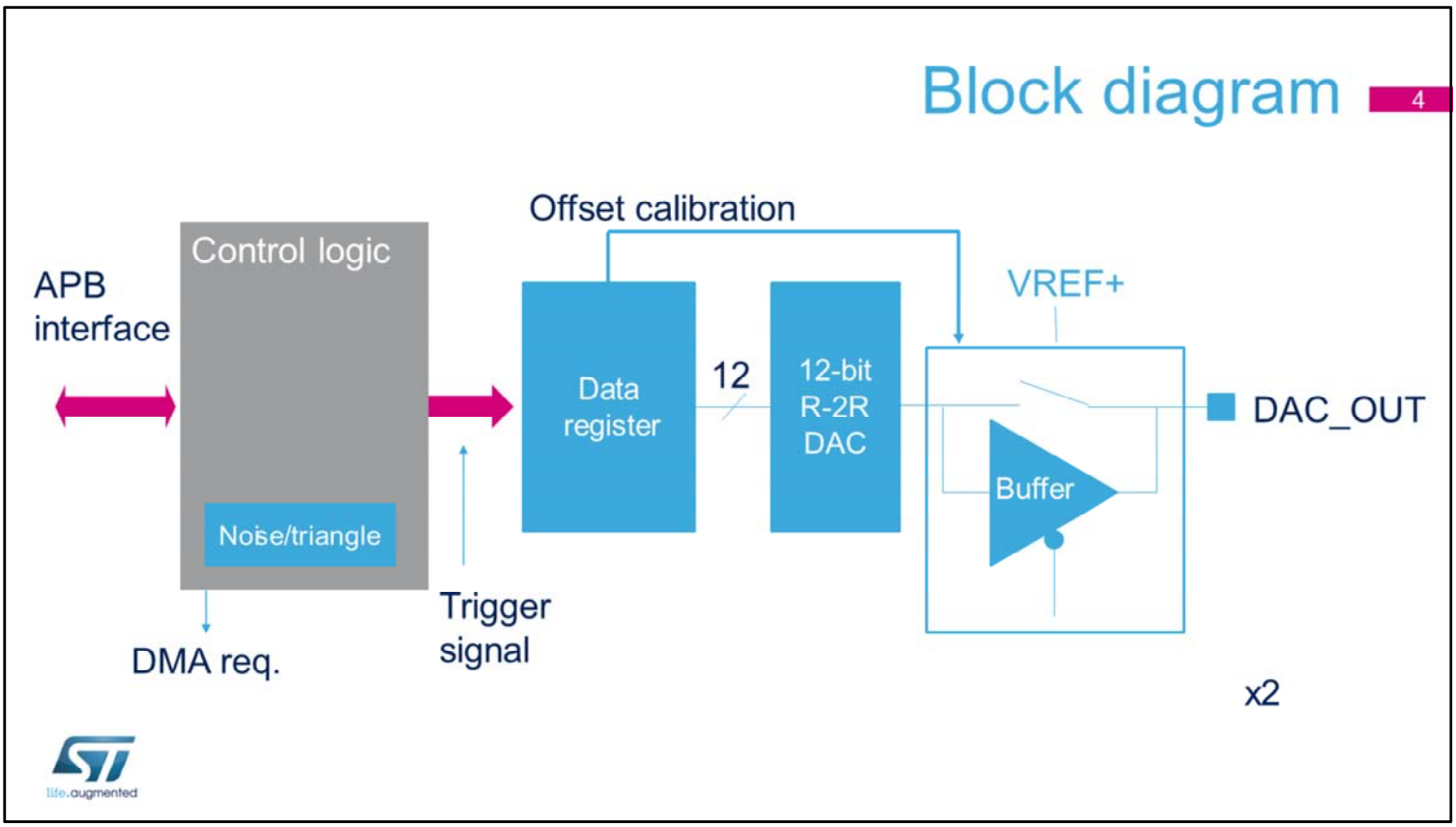
Hello, and welcome to this presentation of the **STM32MP1** digital-to-analog converter. This block is used to convert digital signals to analog voltages which can interface with the external world.



The STM32MP1 digital-to-analog converter converts 8- or 12-bit digital data to an analog voltage. Two DAC modules are embedded in the **STM32MP1 microprocessor.**
A low-power Sample and Hold mode is also integrated. The DAC can interface with external pots or bias circuitry. It can also create voice and arbitrary signals.



The digital-to-analog converter inside STM32MP1 products offers simple digital-to-analog conversion in an 8- or 12-bit mode; 10-bit monotonicity is guaranteed. The DAC output can have a low impedance buffer to drive external loads. Its Sample and Hold mode can reduce the power consumption significantly. Two DACs can be synchronized with each other. The input data can be transferred by DMA which offloads the CPU. The DAC output data can be updated by a timer or an external trigger as well as a software trigger. It also integrates small logic to generate noise waves as well as triangle waves.

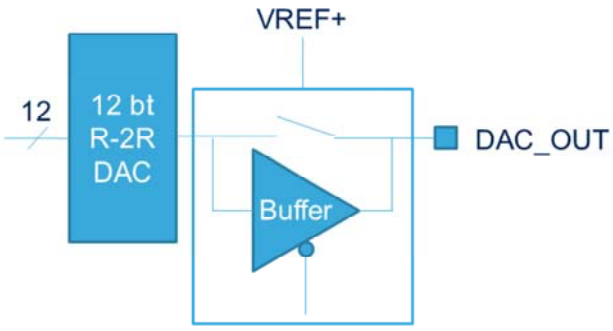


Here you can see the simplified block diagram of the digital-to-analog converter. The STM32MP1 integrates 2 of them. The block DAC is supplied by VDDA.

DAC with output buffer

Easy to interface with different configurations

- Output
  - Low impedance output using buffered mode
  - Raw output from the R-2R type resistor ladder DAC
    - Output impedance is ~13 kΩ



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The DAC output can be buffered for low impedance loads. When unbuffered, the output is directly connected to the R-2R resistor ladder network type of DAC.

DAC data formats (1/2)

Flexible data input formats

- 8-bit mode:
  - Right-aligned data input (on 16-bit data register)
  - 8-bit + 8-bit data input for Dual Channel mode

- 12-bit mode:
  - Right-aligned data input (on 16-bit data register)
  - Left-aligned data input (on 16-bit data register)

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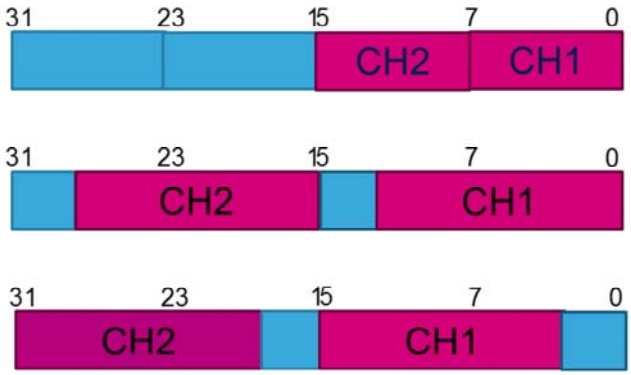
The DAC can support different input formats. In 8-bit mode, it’s a right-aligned 8-bit data format.

DAC data formats (2/2)

Dual channel mode

- 8-bit mode:
  - 8-bit + 8-bit data input for Dual Channel mode
- 12-bit mode:
  - 12-bits + 12-bits Right-aligned data input for Dual Channel mode
  - 12-bits + 12-bits Left-aligned data input for Dual Channel mode



In Dual channel mode , it's an 8-bit plus 8-bit data format, in order to provide input data for two DAC simultaneously. In 12-bits + 12-bits, either a right- or left-aligned mode can be used for input data.

DAC conversion triggers

Several triggers for starting the DAC

- Automatically by writing to the Data Hold register
- By a triggered conversion:
  - 12 different timer outputs
  - External I/O trigger
  - Setting the software trigger bt

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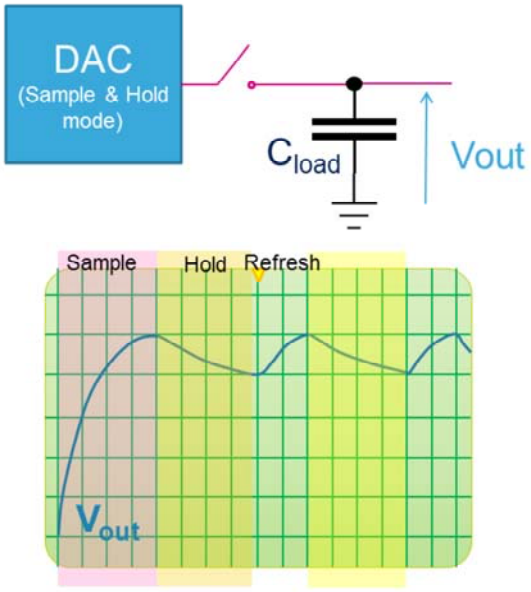
DAC output conversion is started by writing to the Data Hold register using software. 12 different timer outputs, an external I/O or software can trigger a DAC conversion.

Sample and Hold feature (1/2)

Low power mode

- "Sample & Hold" feature is available for extremely low power requirements.

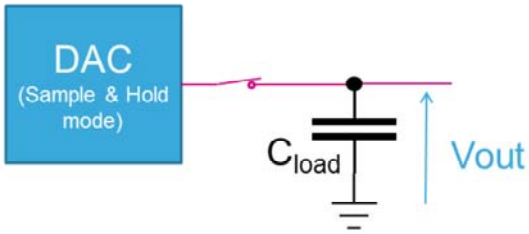


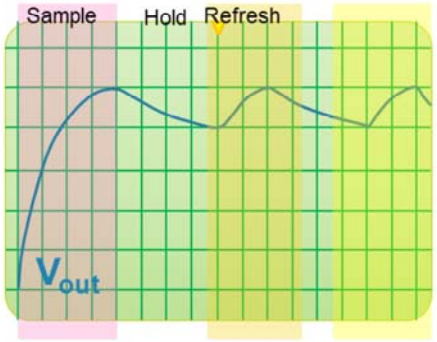
The digital-to-analog converter has a Sample & Hold mode feature. The DAC can work intermittently, charge the external or internal capacitor, and be powered down while the output voltage is kept on the hold capacitor. After a certain period, the DAC is powered back on again and recharges the hold capacitor.

Sample and Hold feature (1/2)

Low power mode

- "Sample & Hold" feature is available for extremely low power requirements.
- When the DAC is configured in "Sample & Hold" mode, it is able to generate its converted output voltage, and active circuitry can be turned off.



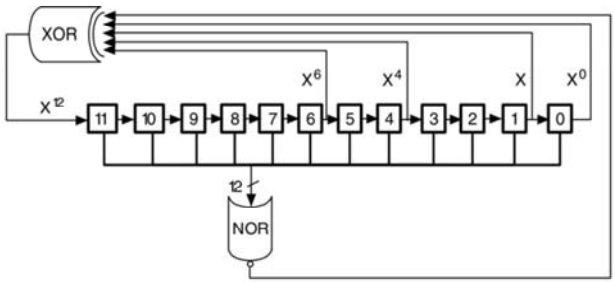


In doing so, the DAC is only active during very low duty cycles; resulting in very low power consumption. The duty cycle program is very flexible and autonomous.

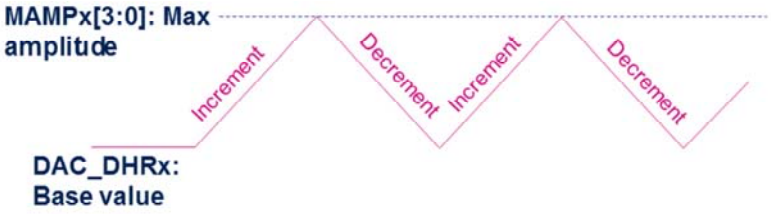
Noise and triangle wave generation

Several wave generation

- Noise generation
  - Based on the LFSR (linear feedback shift register)
    - Initial vale = 0xAAA
    - Calculated noise value is added to the Data Hold register without overflow using an external trigger



- Triangle generation
  - Based on the up-down counter, a triangle waveform can be generated (each trigger increments a +/- 1 step)

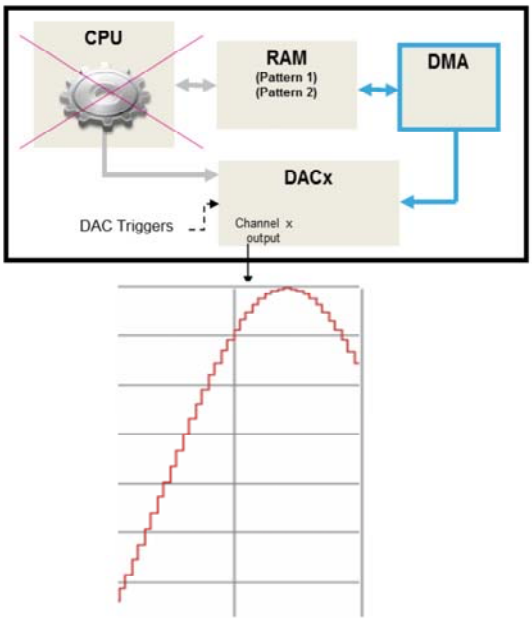


The DAC digital interface integrates two special signal generators. The Linear Feedback Shift register can create the noise signal for the DAC input. Each trigger updates the DAC output data by an LFSR block.
The up-down counter with a programmable count value can create triangle wave data which can update the DAC output data. The data can also be updated by a trigger signal.

DAC with DMA

Offloads the CPU

- The DAC DMA request is generated when an external trigger occurs:
  - The Data Hold register value is then transferred to the Data Output register.
  - DMA underrun with interrupt capability
  - Can generate a stable sampling time based output (timer controlled)



The DAC can also create DMA requests from the trigger signal. Once a trigger is detected, the Data Hold register value is then transferred to the Data Output register. Then the DMA request is generated to obtain the new data for the Data Hold register. As the update of the Output Data register is initiated directly by the trigger signal, the DAC output signal will not have jitter, so that it can create a stable sampling time signal output, making it easy to filter out the sampling frequency.

Interrupts and DMA

Interrupt event	Description
DMA underrun	When a DMA request is not processed by the next external trigger

DMA event	Description
DMA request	External trigger when the DMAENx bits are set

The DAC can generate a DMA underrun interrupt. To transfer data from memory, a DMA request can be generated.

Low-power modes

Mode	Description
CRun	Active.
CSleep	Active. The output data can be updated by DMA.
Stop + LP Stop	Active. The DAC remains active with a static output value or Sample and hold mode.
LPLV Stop	Active. The DAC remains active with a static output value or Sample and hold mode.
Standby	Powered down. The peripheral must be reinitialized after exiting Standby mode.

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The digital-to-analog converter is active in the following low-power modes: CRun, Csleep, Stop, LP Stop and LPLV Stop.
In Standby mode, the DAC is powered-down and it must be reinitialized afterwards.

Performance

	Condition	Value (typical)	Unit
VDDA		1.8 ~ 3.6	V
Monotonicity		10	bits
DNL		+/- 2	LSB
INL		+/- 4	LSB
ENOB	1 kHz output	10.9	bits
Consumption	Buffer on	TBD	µA
	Buffer off	TBD	µA
Settling time	+/-1 LSB, C = 10 pF	2.0	µs
Sampling rate		1.0	Msamples/s

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The following table shows some performance parameters for the digital-to-analog converter. The DAC can work between 1.8 and 3.6 volts. 10-bit monotonicity is guaranteed. By using Sample & Hold mode, the current consumption can be drastically reduced. Depending on the condition and the hold capacitor characteristics, less than 1 µA current consumption is possible for this mode. The DAC buffered output has a settling time of 2 µsec with 10 pF load. The DAC can handle a sampling rate of 1 mega sample per second; when using external components, it can support up to 10 mega samples per second. This is described in detail in application note AN4566.

Related peripherals

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- Refer to these peripherals trainings linked to this peripheral:
  - DMA – direct memory access
  - Interrupts
  - GPIO – general purpose inputs and outputs
  - TIM – timers
  - ADC – analog to digital converter
  - COMP – comparators
  - Op Amp – operational amplifiers

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This is a list of peripherals related to the DAC. Please refer to these peripheral trainings for more information if needed.

References

- For more details, please refer to following sources
  - AN3126: Audio and waveform generation using the DAC in STM32 microcontrollers
  - AN4566: Extending the DAC performance of STM32 microcontrollers

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Application notes dedicated to DAC topics are also available.