Hello, and welcome to this presentation of the STM32F7 System Configuration Controller.
STM32F7 microcontrollers feature a set of configuration registers. The main purposes of the system configuration controller are the following:

- Remap the memory areas
- Select the Ethernet PHY interface
- Managing the external interrupt line connection to the GPIOs
- Managing I/O compensation cell feature
- Managing Class B feature (*)
- Enabling /disabling I2C Fast-mode Plus 20 mA high-drive (*)

(*) Availability depends on STM32F7 device

STM32F7 microcontrollers feature a set of configuration registers. The System Configuration Controller gives access to the following features: Remapping memory areas, managing the external interrupt line connection to the GPIOs, certain robustness features, selecting Ethernet PHY interface and finally the configuration of the 20 mA high-drive I/Os used for I²C Fast-mode Plus. Certain features such as Flash bank swap, dual boot and Class B System configuration register are not available on all STM32F7 microcontrollers, please refer to the respective reference manuals.
The SWP_FB bit in the System Configuration Remap register allows swapping of Flash memory banks 1 and 2, which allows booting either to Bank 1 or to Bank 2. The MEM_BOOT bit in the same register allows software to identify the boot address, and in conjunction with BOOT_ADDx option bytes, it allows to identify the boot schema and the running firmware.
For STM32F7 microcontrollers with the dual-bank Flash feature, the FB_MODE bit determines the address mapping of Banks 1 and 2.
The SWP_FMC bit in the System Configuration Remap register allows remapping the FMC controller’s SDRAM banks 1 and 2 to the NOR/RAM bank base address, which allows changing the SDRAM memory’s attributes. When FMC bank swap is enabled, the NOR/RAM bank is remapped to the SDRAM bank 1 address.
The Class B System Configuration Register contains the control and status bits linked to safety and robustness. Two control bits direct certain error detection events to the timers’ break inputs. This allows timer outputs to be placed in a known state during an application crash. Once programmed, the connection is locked until the next system reset. These internal events are the power voltage detector event and the Cortex-M7 LOCKUP state.
The system configuration controller manages the selection of the GPIO to the external interrupt or event signal, which is used as asynchronous external interrupt or event with Wakeup from Stop capability. It also contains the I2C I/Os Fast-mode Plus 20 mA drive enable control bits. 4 I/Os can be configured in high-drive mode even if they are not used as I2C alternate functions. They can be used to drive LEDs for instance.
The values on the BOOT pin are latched on the 4th rising edge of the SYSCLK signal after a reset. It is up to the user to set the BOOT pin after a reset to select the required boot mode. The BOOT pin is also resampled when the device exits Standby mode. Consequently, they must be kept in the required Boot mode configuration when the device is in Standby mode.

After the startup delay, the boot space is selected before releasing the processor reset. The BOOT_ADD0 and BOOT_ADD1 address option bytes are used to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on the ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on the AXIM interface
• The System memory bootloader
The BOOT_ADD0 / BOOT_ADD1 option bytes can be modified after a reset in order to boot from any other boot address after the next reset.
If the programmed boot memory address is out of the memory mapped area or in a reserved area, the default boot fetch address is programmed as follows:
  • Boot address 0: ITCM-FLASH at 0x0020 0000
  • Boot address 1: ITCM-RAM at 0x0000 0000
When flash level 2 protection is enabled, only a boot from Flash (on ITCM or AXIM interface) or the system bootloader will be available. If the already programmed boot address in the BOOT_ADD0 and/or BOOT_ADD1 option bytes is out of the memory range or RAM address (on ITCM or AXIM), the default fetch will be forced from the Flash on ITCM interface at address 0x00200000.
When Dual-boot mode is enabled, the boot is forced to the System memory.
The system memory firmware will boot firmware in Bank 2 if it is valid, otherwise it will boot in Bank 1.
For more details on Dual-boot, please refer to application note AN2606.
BOOT_ADD0 and BOOT_ADD1 address option bytes allows to program any boot memory address from 0x0000 0000 to 0x2007 FFFF with a granularity of 16 Kbytes.
- BOOT_ADDx options bytes address corresponds to the to address [29:14]

If the programmed boot memory address is out of the memory mapped area or in a reserved area, the default boot fetch address is:
- BOOT_ADD0: FLASH on ITCM @0x0020 0000
- BOOT_ADD1: ITCM-RAM @0x0000 0000

The diagram shows the memory map and the default boot fetch addresses:
- BOOT_ADD0: ITCM-FLASH at 0x0020 0000
- BOOT_ADD1: ITCM-RAM at 0x0000 0000

The BOOT_ADD0 / BOOT_ADD1 option bytes can be modified after reset in order to boot from any other boot address after next reset.
If the programmed boot memory address is out of the memory mapped area or a reserved area, the default boot fetch address is:
- BOOT_ADD0: ITCM-FLASH at 0x0020 0000
- BOOT_ADD1: ITCM-RAM at 0x0000 0000
When the Dual Boot condition is respected, the STM32 boots from the system memory if the expected boot address is defined within the main Flash address. The STM32F7 boots from RAM if the boot address is defined in RAM. If none of the previous conditions is valid, the Boot is forced to the default memory location.

Dual-boot mode is supported even when the STM32F7 is protected with Readout Protection Level 2.
When STM32F7 readout protection Level 2 is enabled, the boot address is restricted to only addresses in Flash. When in Single-bank configuration, any programmed boot address out of the memory range or RAM or system memory address, the default fetch will be forced from Flash on the ITCM interface at address 0x0020 0000.

In Dual-bank configuration, the STM32F7 boots in Flash Bank 2 if it is valid, otherwise in Bank 1.
The on-chip bootloader allows the user to program the Flash memory through a serial communications peripheral. The supported protocols are USART, USB, CAN, SPI and I²C.

Note
The DFU/CAN may work with different values of the external quartz oscillator in the range of 4 to 26 MHz, and the USART uses the internal HIS.
Related peripherals

- Refer to these training modules linked to this peripheral:
  - Reset and clock control (RCC)
  - Power controller (PWR)
  - Interrupts (NVIC-EXTI)
  - Flash memory (I-flash)
  - System memory protections
  - Timers (TIM)
  - Inter-Integrated Circuit (I²C)

In addition to this training, you can refer to the Reset and Clock Control, Power Controller, Interrupts, Flash and System Memory Protections, Timers and I²C trainings.
For more details, please refer to application note AN2606
STM32 microcontroller system memory boot mode.