Hello, and welcome to this presentation of the STM32F7 power controller. It covers the efficient power management and all STM32F7 power modes.
The STM32F7 has several key features related to power management:
- Efficient dynamic consumption with free running clocks gating when needed. This allows to go down to 425 µA/MHz, executing from Flash memory,
- Independent power supplies, allowing to reduce MCU power consumption while some peripherals are supplied at higher voltages,
- A battery backup domain, called $V_{\text{BAT}}$, including the RTC and certain backup registers.
The STM32F7 has several power supplies. The main power supply is VDD, and supplies almost all the I/Os except those mapped on dedicated supplies. In addition, VDD supplies the Standby circuitry which includes the wakeup logic and independent watchdog. VDD supplies voltage regulators which provide the $V_{\text{CORE}}$ supply. $V_{\text{CORE}}$ supplies most of the digital peripherals and the SRAMs. The Flash memory is supplied by both $V_{\text{CORE}}$ and VDD. $V_{\text{CAP1}}$ and $V_{\text{CAP2}}$ pins have to be connected to external capacitors in Regulator-ON mode, the exact value is specified in the datasheet. In Regulator bypass mode the $V_{\text{CORE}}$ supply can be provided externally on $V_{\text{CAP1}}$ and $V_{\text{CAP2}}$ pins, the value for the $V_{\text{CORE}}$ specified in the datasheet $V_{\text{CAPDSI}}$ pin have to be connected to external capacitors when the DSI regulator is available, the exact value is
specified in the datasheet.

Internal regulators providing VCORE can also be BYPASSED and 1.2 V supply is provided by the VCAP pin in Regulator-OFF mode. Regulator ON/OFF mode is only available on packages with a BYPASS_REG pin.

STM32F7 microcontrollers feature several independent supplies for peripherals:
- VDDA for the analog peripherals, device PLLs and internal reset block. VDD and VDDA must be connected to the same source.
- VDDUSB for the USB transceiver.
- VDDSDMMC supplies 6 IOs used for SD card communication, SDMMC2 clock, command and 4 data pins.
- The VDDDSI pin provides the DSI peripheral voltage supply.

The VDDSDMMC and VDDDSI pins are available only on some STM32F7 devices. The $V_{REF}^{+}$ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters.

A backup battery can be connected to $V_{BAT}$ pin to supply the backup domain.
The main power supply VDD ensures full feature operation in all power modes from 1.7 up to 3.6 V, allowing the microcontroller to be supplied by an external 1.8 V regulator. Device functionality is guaranteed down to 1.7 V when the internal reset is OFF.

The analog power supply VDDA must be connected to VDD. When the analog-to-digital-converter is used, VDDA voltage has an impact on its performance. VDDA must be greater than 2.4 V for maximum ADC performance.

The USB power supply (VDDUSB) can be connected to any voltage other than VDD. When the USB is used, VDDUSB must be greater than 3V. GPIO pins PA11, PA12, PB14 and PB15 are supplied by VDDUSB. 6 I/Os corresponding to PF9 to PG12, PD6 and PD7 are supplied by VDDSDMMC independently from VDD.

Several functions are available on these I/Os: SDMMC2...
in 4-bit mode, SPI1, I2S1. VDDSDMMC is available starting with packages that have at least 144 pins. A backup domain is supplied by VBAT, which must be greater than 1.65 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the 128-byte backup registers.
VDDSDMMC is available only on some STM32F7 devices. It allows several IOs and functions (SDMMC2 in 4-bit mode, SPI1 or I2S1) to be used independently from VDD. 4 I/Os corresponding to PA11, PA12, PB14 and PB15 and also for USB transceiver from 3 to 3.6 V when USB is used.

VDDUSB is used mainly as a USB transceiver supply when VDD is below 3V. Several functions are available on these I/Os: USART1, USART4, SPI2 or I2S2.
VDDDSI is available only on some STM32F7 packages embedding the DSI Host peripheral. The VDDDSI pin provides the DSI Host peripheral with a voltage supply ranging from 1.7 up to 3.6V. VCAPDSI is the DSI voltage regulator external capacitor. VDD12DSI is for the MIPI DSI PHY supply, typical input voltage is 1.2V.
The STM32F7 has an integrated POR/PDR circuitry that allows proper operation starting from 1.8 V. The device remains in Reset mode when VDD/VDDA is below a specified threshold without the need for an external reset circuit. The hysteresis between Power-ON threshold and Power-OFF threshold is 40mV. After reaching Power-ON threshold for VDDA and VDD power supplies, the reset line is still kept low for a temporization time and then the reset line is released.
The embedded internal reset controller monitors the VDD supply to detect if the supply is present or not and releases the reset signal when the supplied power reaches the threshold of 1.8V.

The internal reset controller can be disabled by connecting PDR_ON pin to VSS. When disabled it allows STM32 microcontrollers to operate down to 1.7V.

On STM32F7 microcontrollers, no external VDD power supervisor is needed to manage resets when the internal reset is OFF.
In addition to Power-On reset functionality, there is also a user configurable Brownout reset (BOR) unit, which keeps the device under reset until the supply voltage reaches the specified VBOR threshold.

BOR levels are configurable by option bytes:
- **BOR OFF**: 2.1 V at power-on and 1.62 V at power-down
- **BOR LOW** (DEFAULT): 2.4 V at power-on and 2.1 V at power-down
- **BOR MEDIUM**: 2.7 V at power-on and 2.4 V at power-down
- **BOR HIGH**: 3.6 V at power-on and 2.7 V at power-down

VBOR is configured through device option bytes. By default, BOR is off. 3 programmable VBOR threshold levels can be selected:
- **BOR Level 3** (VBOR3). Brownout threshold level 3.
- **BOR Level 2** (VBOR2). Brownout threshold level 2.
- **BOR Level 1** (VBOR1). Brownout threshold level 1.
For full details about BOR characteristics, refer to the "Electrical characteristics" section in the device datasheet. This function is useful in applications where several devices have different operational voltage range. Depending on the BOR level, the F7 microcontroller will not start until VDD voltage reaches the operational range of all connected devices.
The programmable voltage detector (PVD) is used to monitor the VDD power supply by comparing it to a threshold selected by software. An interrupt can be generated when VDD drops below the PVD threshold and/or when VDD rises above the PVD threshold. PVD is internally connected to EXTI line 16.

Depending on STM32F7 device, PVD interrupt can be connected to Break input of Timer 1 or Timer 8 to put the timer’s output signals in a safe configuration.
This table describes the Regulator ON/OFF and internal reset ON/OFF availability per package. For a list of available package per STM32F7 line please refer to datasheet.
Two embedded linear voltage regulators supply all the digital circuitries except for the Standby circuitry and the Backup domain.

The regulator output voltage \( V_{\text{CORE}} \) can be programmed by software to three different values depending on the performance and the power consumption requirements. This is called Dynamic Voltage Scaling.

Depending on the application mode, \( V_{\text{CORE}} \) is provided either by the main voltage regulator for Run, Sleep and Stop modes, or by the low-power regulator for Stop mode to optimize power consumption. The regulators are OFF in Standby mode. SRAMs and peripheral are powered-down in Standby. They must be reinitialized after exiting from this mode.
The backup domain contains essentially the following blocks:
- The RTC unit and 128 bytes of RTC backup registers
- 4 Kbytes of backup SRAM
- The LSE oscillator
- PC13 to PC15 I/Os, plus PI8 I/O (when available)

To retain the content of these blocks when VDD is turned off, the \( V_{\text{BAT}} \) pin can be connected to an optional battery providing a standby voltage supply.

The switch to the \( V_{\text{BAT}} \) supply is controlled by the power-down reset embedded in the Reset block.

After reset, the backup domain (RTC registers, RTC backup register and backup SRAM) is protected against possible unwanted write accesses.
Voltage scaling and Over-drive mode offer flexibility between required performance and consumption. Over-drive mode allows the CPU and core logic to operate at higher frequencies than the normal mode for a given voltage scaling.

In Run mode, three voltage scaling modes are available:
- Voltage scale 1 is the high-performance range, allowing a system clock up to 180 MHz. 216 MHz is possible with Over-drive.
- Voltage scale 2 is the medium-performance range, allowing a system clock up to 168 MHz. 180 MHz is possible with Over-drive.
- Voltage scale 3 is low-performance and low-power range that allows a system clock up to 144 MHz.
Sleep mode allows all peripherals to be used and features the fastest wakeup time.
In this mode, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep mode.
This mode is entered by executing the assembler instruction Wait for Interrupt or Wait for Event.

Depending on the SLEEPONEXIT bit configuration in the Cortex-M7 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority interrupt sub-routine. This last configuration saves time and reduces consumption by eliminating the need to pop and push the stack.
STM32F7 devices feature Stop mode with different configurations to reduce leakage: Stop is the lowest power mode with full retention and only a 15µs wakeup time to Run mode on HSI clock. The contents of SRAMs and all peripheral registers are preserved in Stop mode. All high-speed clocks are stopped. The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled. Some peripherals can be active (RTC, LPTIM). All EXTI lines can wake up from Stop mode. Wakeup time depends on the power regulator and Flash memory configuration, it can be in the range of 15 up to 120 µs. The system clock on wake-up is the internal high-speed oscillator running at 16 MHz. Stop mode with under-drive mode enabled is the lowest

<table>
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<tr>
<th>Lowest power modes with full retention</th>
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<tr>
<td>• SRAM and all peripherals registers retention</td>
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<td>• Under-drive mode: the 1.2 V domain is preserved in reduced leakage mode</td>
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<tr>
<td>• All high-speed clocks are stopped</td>
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<td>• LSE (32 768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled</td>
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<tr>
<td>• EXTI peripheral can wake up from Stop mode</td>
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<td>• Wakeup time from 15 to 120 µs</td>
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<td>• System clock at wakeup is HSI</td>
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power mode with full retention.
Standby mode is the lowest power mode in which the 128-byte backup registers and 4 Kbytes backup SRAM are retained.

The voltage regulator is in Power down mode and the SRAMs and the peripherals registers are lost. As the V_{CORE} domain is powered off, the ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the VDD slope. I/O are in high-impedance state during Standby mode.

6 wakeup pins are available to wake up the device from Standby mode. The polarity of each wakeup pin is configurable.

The wakeup from Standby generates a system reset. Wakeup time is 313\mu s, but the software initialization and
configuration have to be taken into account as well.
The backup domain allows to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.

The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. 2 tamper pins are functional in VBAT mode, and erase the 128-byte backup registers also included in the VBAT domain, in case of intrusion detection.

The backup domain also contains the RTC configuration register.

In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
This slide illustrates typical power consumption figures for STM32F7 series.

**Typical values measurements conditions are room temperature (25°C) and VDD=3.3V**

Dynamic run mode consumption is in the range of 425 µA/MHz, while running CoreMark code from Flash memory at maximum frequency.

Stop low-power mode with full retention for peripheral configuration and SRAMs is in the range of 130 µA. For more details, you can refer to the datasheet.
2 bits are available in the Flash option bytes to prohibit entering a given low-power mode. When cleared, these option bits trigger a reset when entering either Standby or Stop modes. This is a security feature used to reduce the impact of unintentional entry into these low-power modes. In case these low-power modes are not used in user code, the option should be enabled.
3 bits are available in the Debug Control Register, in order to allow debugging in Sleep, Stop and Standby modes. When the related bit is set, the regulator is kept ON in Standby mode, and the HCLK and FCLK clocks remain ON to keep the debugger active. This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup. Remember to clear these bits when the MCU is not under debug, because the consumption is higher in those low-power modes when these bits are set, due to the fact they force the clocks and the regulators to remain enabled.