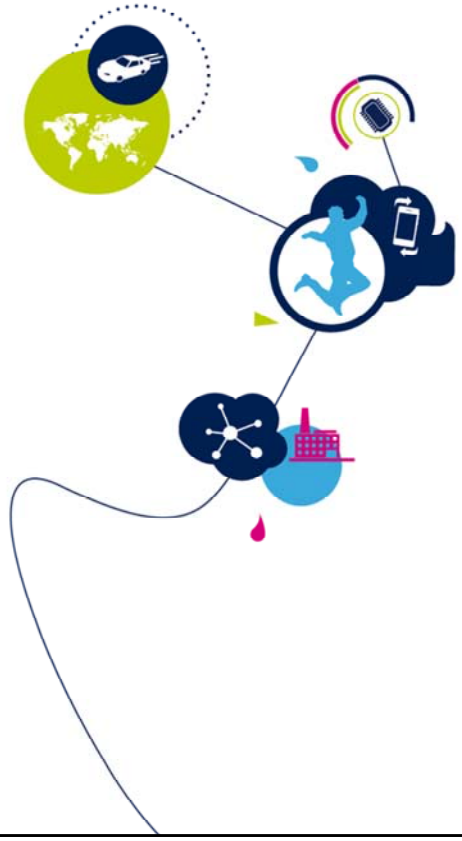
# STM32G4 - DAC

Digital-to-Analog Converter
Revision 1.0



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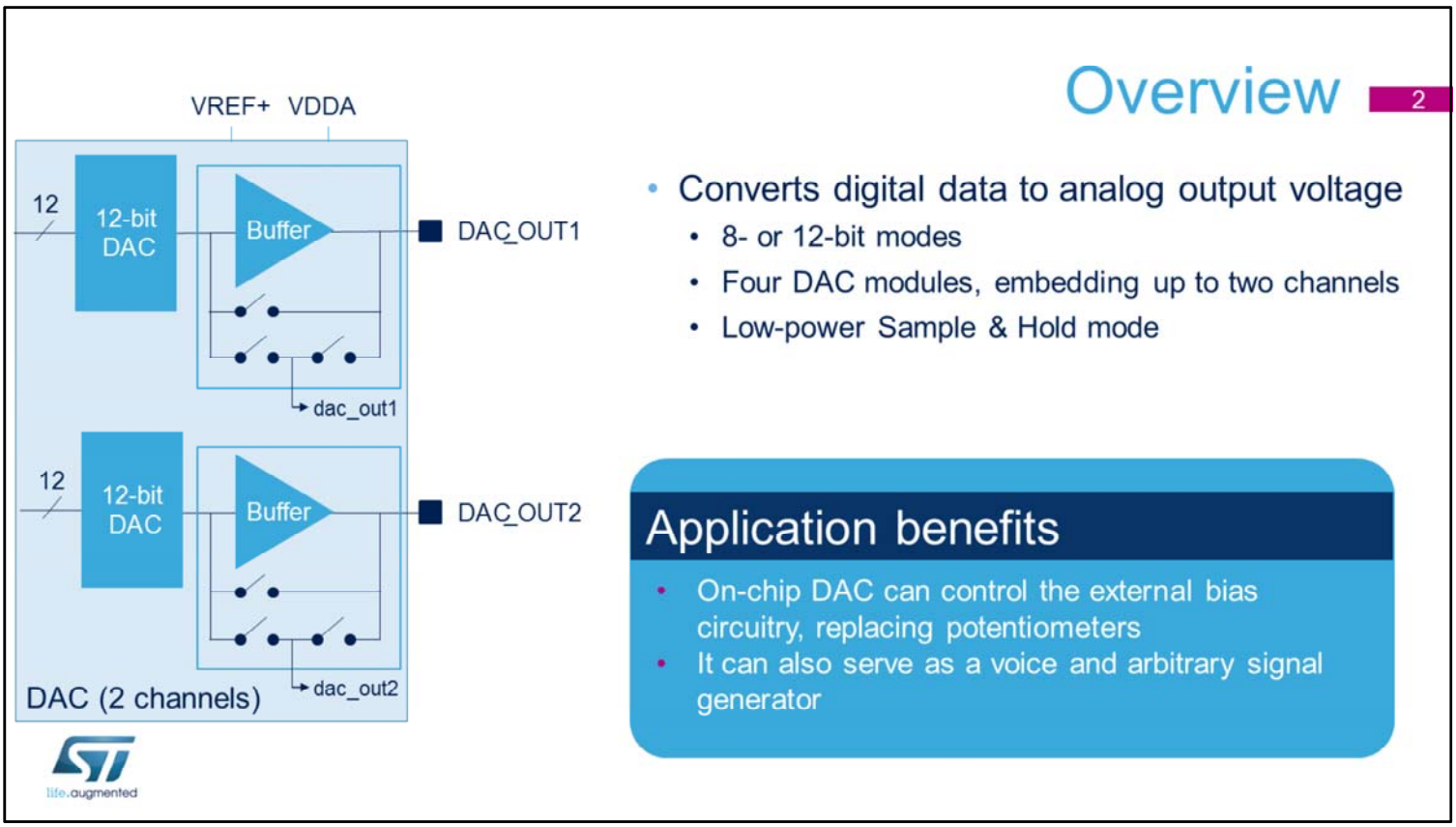
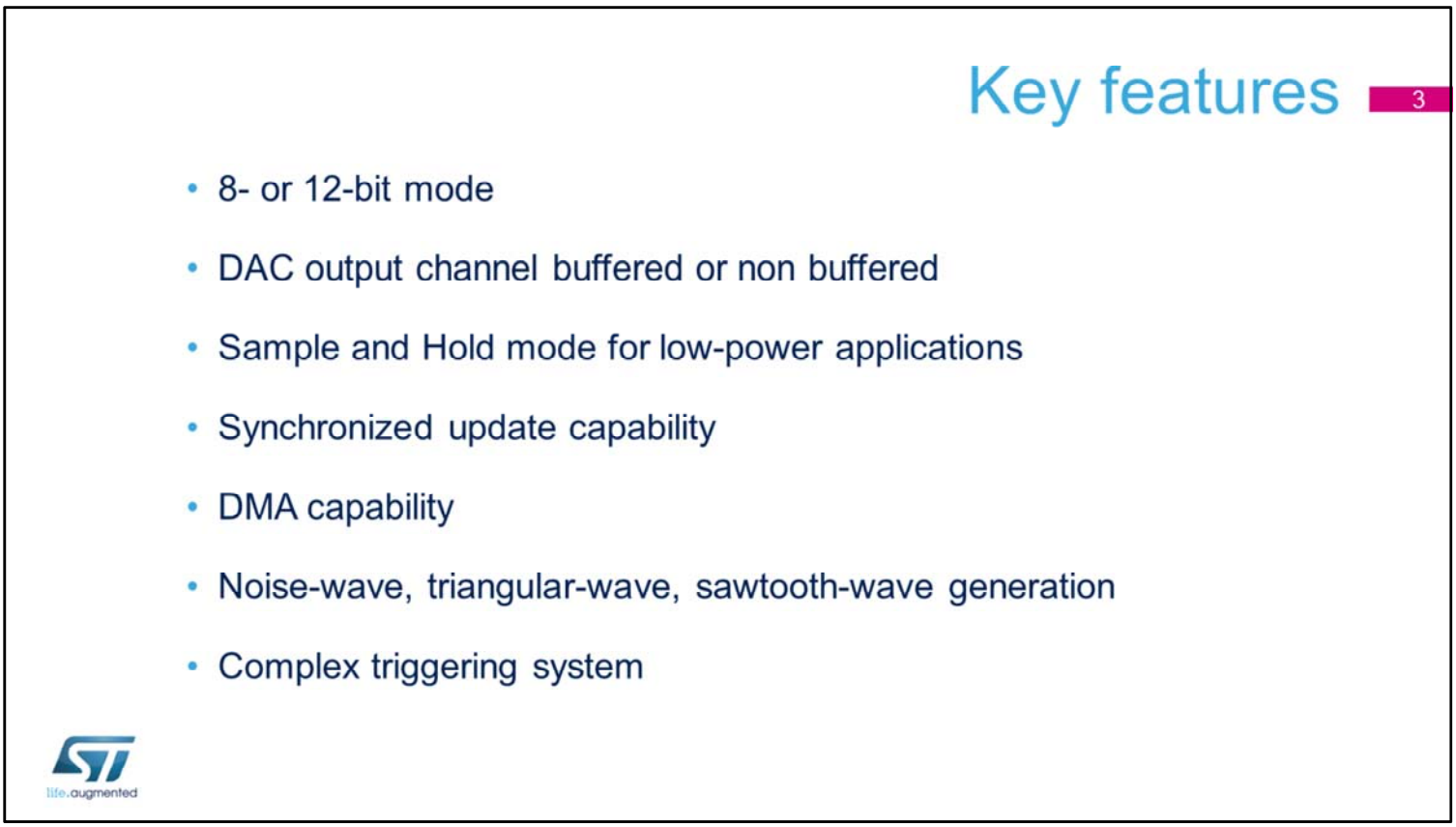
Hello, and welcome to this presentation of the STM32G4 digital-to-analog converter.
This block is used to convert digital signals to analog voltages which can interface with the external world and also with on-chip peripherals such as comparators and operational amplifiers.




The STM32G4 digital-to-analog converters converts 8- or 12-bit digital data to an analog voltage.
Each DAC module has two converters that can work synchronously or asynchronously.
A low-power Sample and Hold mode is also integrated.
The DAC can interface with external potentiometers or bias circuitry.
It can also create voice and arbitrary signals.




The digital-to-analog converter inside STM32G4 microcontrollers offers simple digital-to-analog conversion in an 8- or 12-bit mode.
The DAC outputs can have a low impedance buffer to drive external loads.
Its Sample and Hold mode can reduce the power consumption significantly.
The two converters within the same DAC can be synchronized with each other.
The input data can be transferred by DMA which offloads the CPU.
It also integrates small logic to generate noise, triangle and sawtooth waveforms.
The DAC output data is updated by a complex triggering system, based on software request, timers, HRTIM and EXTI.

## Advanced features



- VREF+ pin used as reference voltage
  - Can be driven by internal VREFBUF output: 2.048V, 2.5V, 2.9V
  - Or external reference connected to VREF+ pin
- Buffer calibration:
  - Offset calibration only
  - Factory calibration loaded at DAC reset
  - User trimming

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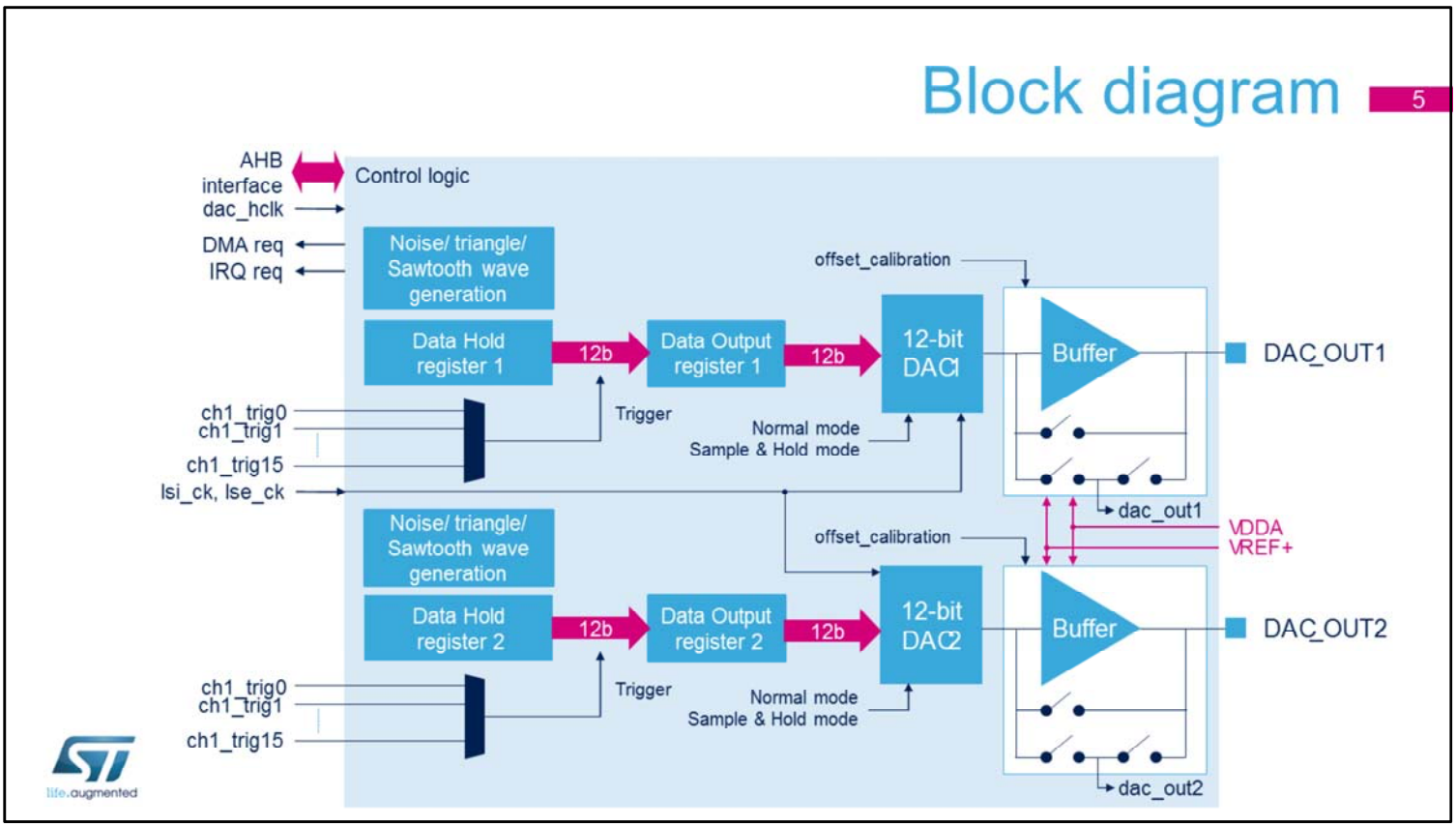
VREF+ is used as a positive voltage reference.
An input reference pin, VREF+ (shared with others analog peripherals) is available for better resolution.
An internal reference voltage buffer can generate the reference voltage on the same pad.
Output buffer's voltage offset is calibrated.
This calibration is performed at the factory, loaded after reset.
The user calibration can be done when the operating conditions differs from nominal factory calibration conditions and in particular when VDD/VDDA voltage, temperature, VREF+ values change and can be done at any point during application by software.




Here you can see the simplified block diagram of the digital-to-analog converter.
This DAC block is supplied by VDDA and uses VREF+ as a voltage reference.
The digital-to-analog converter is an AHB slave that supports DMA requests to fill the data hold register.
Either of the DAC_OUTx signals can be disconnected from the corresponding output pin which can be used as an ordinary GPIO.
DAC_OUTx signals can use an internal pin to connect to on-chip peripherals such as comparators and OPAMPs.
DAC output channels are buffered or non-buffered.
Sample and hold block use LSI (Low-Speed Internal oscillator) or LSE (Low-Speed External oscillator) clock source and are operational in Stop mode for static conversions.
The content of the Data Hold registers is transferred to

the corresponding Data Output register when a trigger condition is detected, this includes software triggers. Then the content of the Data Output register is transferred to the converter.
The output buffer has mechanism to calibrate the voltage offset.

# DAC channels configuration



| DAC features | DAC1 | DAC2 | DAC3 | DAC4 |
|---|---|---|---|---|
| Maximum sampling time | 1Msps | | 15Msps | |
| Output buffer | x | x | | |
| Number of channels | 2 (external) | 1 (external) | 2 (internal) | 2 (internal) |
| IO connection | CH1 on PA4<br>CH2 on PA5 | CH1 on PA6 | No connection to GPIO | |

- DAC speeds:
  - 15MHz:
    - Internal channels only (DAC3_OUTx, DAC4_OUTx)
    - Unbuffered mode only
  - 1MHz:
    - 3 external channels (DAC1_OUTx, DAC2_OUT1)
    - Buffered/unbuffered mode

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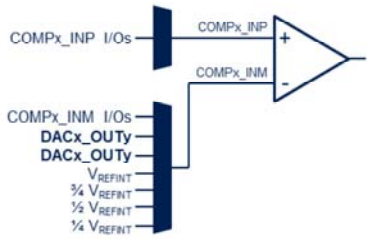
The STM32G4 implements four DAC units.
DAC1, 3, 4 support two channels while DAC2 supports only one channel.
DAC1 and DAC2 can be output to GPIOs while DAC3 and DAC4 only have internal channels, that can be connected to COMP and OPAMP units.
Consequently, DAC3 and DAC4 do not implement output buffers.
The utilization of output buffers is optional for DAC1 and DAC2.
DAC1 and DAC2 maximum speed is 1 Mega sample per second, while DAC3 and DAC4 maximum speed is 15 Mega sample per second.

# DAC internal outputs

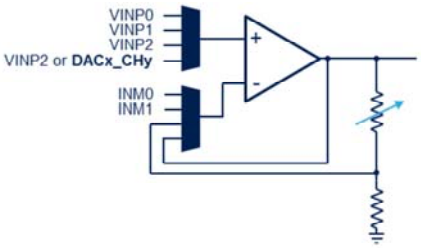


- DAC output as internal signal only:
  - The DAC output channel can be disconnected from the DAC_OUTx output pin and can be connected to on-chip peripherals only
  - Corresponding DAC_OUTx pin can be then used for another purpose

Using the output of DAC as a COMP INM input (COMP1-7)
➢ Reference voltage for comparator (DC, waveform generation)




Using the output of DAC as a OPAMP VINP input (OPAMP1-6 except OPAMP2)
➢ Way to get internal DAC channels to pin (OPAMPx_VOUT)

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The dac_outx can use an internal pin connection to on-chip peripherals such as comparator and operational amplifier.
Regarding DAC1 and DAC2, the corresponding DAC_OUTx GPIO can be used for another purpose.
Connecting the internal DAC output to a COMP INM input defines the reference voltage of the comparator.
Connecting the internal DAC output to an OPAMP VINP input can be used to bias the OPAMP DC point or amplify the analog voltage.
It is also a way to get internal DAC channels to pin, which can be useful for DAC3 and DAC4.

# DAC data formats



## Flexible data input formats

- 8-bit mode:
  - Right-aligned data input (on 16-bit data register)


- 12-bit mode:
  - Right-aligned data input (on 16-bit data register)
  - Left-aligned data input (on 16-bit data register)



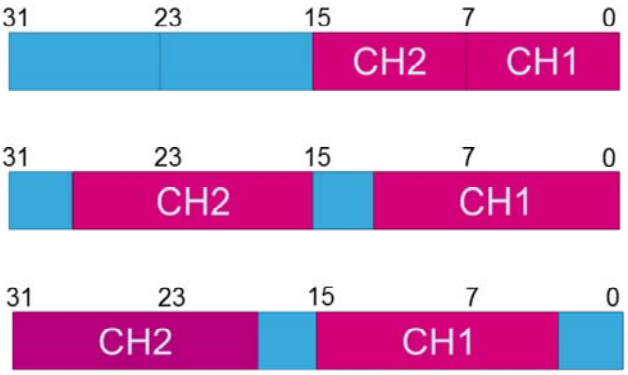
The DAC can support different input formats.
In 8-bit mode, it is a right-aligned 8-bit data format.
It also accepts the unsigned and signed data format.

# DAC data formats



## Dual-channel mode

- 8-bit mode:
  - 8-bit + 8-bit data input for Dual-channel mode
- 12-bit mode:
  - 12-bits + 12-bits Right-aligned data input for Dual-channel mode
  - 12-bits + 12-bits Left-aligned data input for Dual-channel mode




In Dual-channel mode, it is an 8-bit plus 8-bit data format, in order to provide input data for two DACs.
In 12-bits + 12-bits, either a right- or left-aligned mode can be used for input data.
Data held in these registers are transferred to the related converters either synchronously (for instance, for stereo audio) or asynchronously.
This means that the two channels can operate independently.

# DAC conversion triggers



## Several triggers for starting the DAC

- Conversions can be started:
  - Automatically by writing to the Data Hold register (software trigger)
    - The DAC_DHRx register to the DAC_DORx register takes only one AHB clock cycle
  - By a triggered conversion:
    - 7 different timer outputs
    - 7 HRTM outputs
    - External I/O trigger
    - Setting the software trigger bit
    - The following table indicates what is the delay between trigger and DAC_DOR update

| HFSEL | AHB frequency | Function |
|---|---|---|
| 00 | ≤ 80 MHz | DAC_DOR update rate up to 3 AHB clock cycles |
| 01 | ∈ ]80 MHz, 160 MHz] | DAC_DOR update rate up to 5 AHB clock cycles |
| 10 | > 160 MHz | DAC_DOR update rate up to 7 AHB clock cycles |
| 11 | Reserved | |

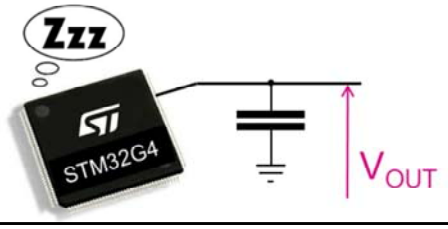
DAC output conversion is started by writing to the Data Hold register using software.
7 different timer outputs, 7 different HRTIM outputs, an external I/O or software can trigger a DAC conversion.
When a software trigger is used, the content of the Data Hold register is transferred to the corresponding Data Output register after 1 AHB clock cycle.
When a trigger occurs in Trigger mode, the content of the Data Hold register is transferred to the corresponding Data Output register after 3, 5 or 7 AHB clock cycles, depending on the AHB clock frequency.

# Sample and Hold feature



## Low power mode

- The main goal of the “Sample & Hold” feature is to maintain the DAC output voltage when the MCU is in low-power operation in Stop0/1 mode
  - LSI or LSE clock remains active while dac_hclk clock is gated
- When configured in “Sample & Hold” mode, the DAC is able to output the converted voltage when all its related Analog and Digital circuitries are turned OFF
- An Internal or External Hold capacitor can be connected to a DAC output

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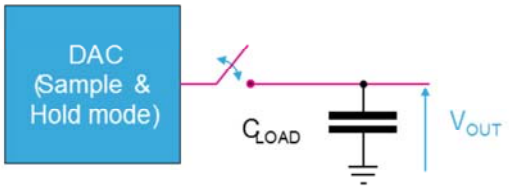
The Sample & Hold feature maintains the DAC output voltage while not actively driving continuously.
It relies on an internal or external capacitor that will hold the voltage level at the end of the sample period.
Then the DAC output can be set in high impedance.
Of course the capacitor will discharge over time. That is why a refresh period has been defined. Upon expiration of the refresh period, the DAC output will be actively driven again to recharge the capacitor.

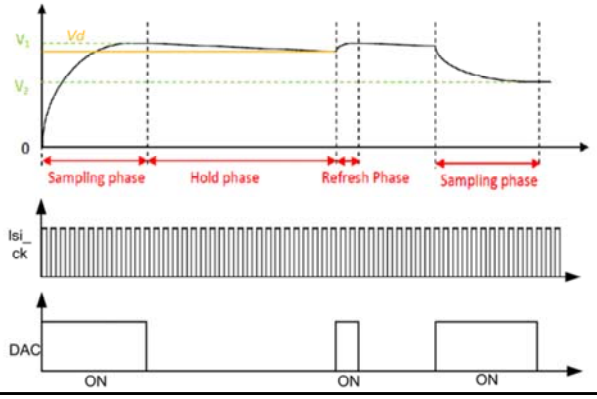
# Sample and Hold feature



## Low power mode

- The DAC conversions during “Sample & Hold” mode are made of three phases:
  - Sampling phase
    - During this phase, the “Sample & Hold” element is charged into the desired voltage
  - Holding phase
    - During which the DAC’s output is tri-stated (High-Z) to maintain the “Sample & Hold” element’s stored electrical charge
  - Refresh phase:
    - Due to leakage coming from several sources, a refresh phase is essential to keep the output voltage at the desired value (+/- LSb)



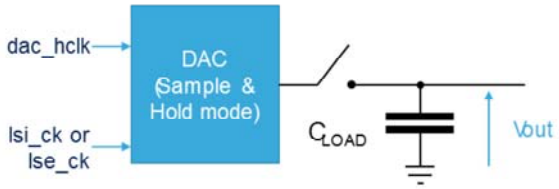

The digital-to-analog converter can work intermittently, charge the external or internal capacitor, and be powered down while the output voltage is kept on the hold capacitor. After the refresh period, the DAC is powered back on again and recharges the hold capacitor.

# Sample and Hold feature



## Low power mode

- "Sample & Hold" feature is available for extremely low power requirements
- Sample, Hold and Refresh timings are configurable
- In this mode, the DAC core and all corresponding logic and registers are driven by the Low Speed Internal oscillator clock (lsi_ck) or the Low Speed External oscillaror clock (lse_ck)

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When the DAC is configured in "Sample & Hold" mode, it is able to generate its converted output voltage, and active circuitry can be turned off.
In this mode, the DAC core and all corresponding logic and registers are driven by the LSI clock (lsi_ck) or LSE clock (lse_ck) in addition to the dac_hclk clock, allowing the usage of the DAC channels in Deep-low-power modes such as Stop mode.
The logic in charge of scheduling refreshes only requires the LSI or LSE clock.
In doing so, the DAC is only active during very low duty cycles: sample and refresh; resulting in very low power consumption.
The duty cycle program is very flexible and autonomous.

# Sample and Hold feature



## Low power mode

- "Sample & Hold" element (Internal or External)
  - When configured to be external: an external capacitor should be mounted on the DAC's external pin
    - Buffer can be enabled or disabled
    - DAC output can be routed or not to internal components (i.e. embedded comparators)
  - When configured to be internal: an embedded capacitor is used as "Sample & Hold" element
    - In this configuration, the DAC output is routed only to internal components (on-chip comparators, etc.)
- Conversion phase timing
  - All conversion phase timings are made in reference to LSI or LSE clock source
  - Sampling, Hold and Refresh timings are configurable

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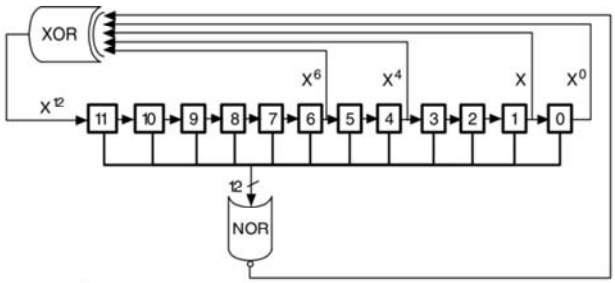
The capacitor can be external or internal.
When it is external, the buffer can be used and the DAC's output can also be routed to internal components, such as embedded comparators.
When it is internal, an embedded capacitor is used and the DAC's output is routed only to internal components.
The charging time depends on the capacitor value.
The timings for the three phases above are in units of lsi_ck or lse_ck clocks cycles.

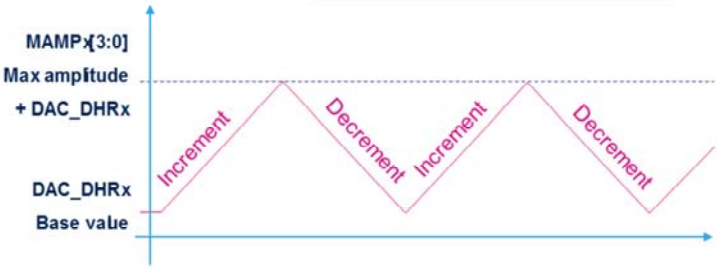
# Noise and triangle wave generation



## Wave generation

- Noise generation
  - Based on the LFSR (Linear Feedback Shift Register)
    - Calculated noise value is added to the Data Hold register without overflow using an external trigger
    - Configurable amplitude
- Triangle generation
  - Based on the up-down counter, a triangle waveform can be generated (each trigger increments a +/- 1 step)
  - Configurable base and amplitude



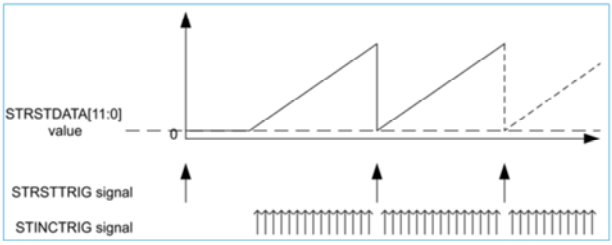

The DAC digital interface integrates three special signal generators: noise, triangle and seetooth.
The Linear Feedback Shift register can create the noise signal for the DAC input.
Each trigger updates the DAC output data by an LFSR block.
The up-down counter with a programmable count value can create triangle wave data which can update the DAC output data.
The data can also be updated by a trigger signal.

# Sawtooth wave generation



## Wave generation

- DAC autonomous waveform generation features
  - Sawtooth
    - Configurable increment/decrement value and amplitude and base




    - Complex triggering system
      - For increment/decrement
      - For reset

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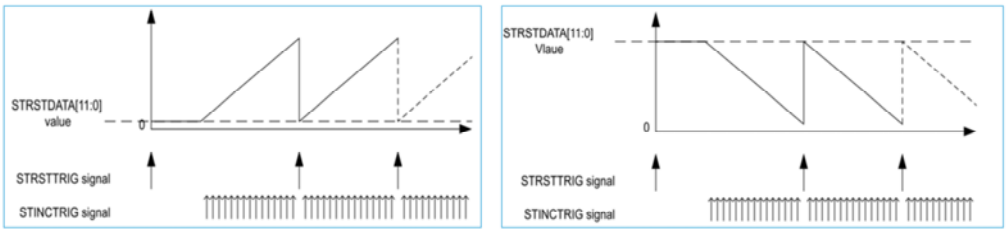
The DAC can generate a sawtooth waveform.
Specific register settings for the initial value, increment value and direction control are required.
The sawtooth counter starts from STRSTDATA, each increment trigger then increments (or decrements) STINCDATA value.
The increment trigger and reset trigger must be selected through the STINCTRIGSEL and the STRSTTRIGSEL bit fields.
This feature is useful to create the threshold voltage for the comparator to control the motor current.

# Sawtooth wave generation



## Wave generation

- Sawtooth generation properties




  - hcrement/Decrement counter:
    - 16-bit sawtooth counter (starts at base value: STRSTDATAx[11:0]<<4)
      - Reset trigger signal initializes the counter to base value STRSTDATAx[11:0]<<4
    - At each STINCTRIG trigger is incremented/decremented by STINCDATAx[15:0]
    - Only higher 12 bits are used as DAC output
      - When reached 0x0000 or 0xFFFF, the value is saturated
  - Trigger signals for increment/decrement (STINCTRIG) and reset (STRSTTRIG)
    - SWTRG bit, EXTI, TIMx_TRGO, HRTIM

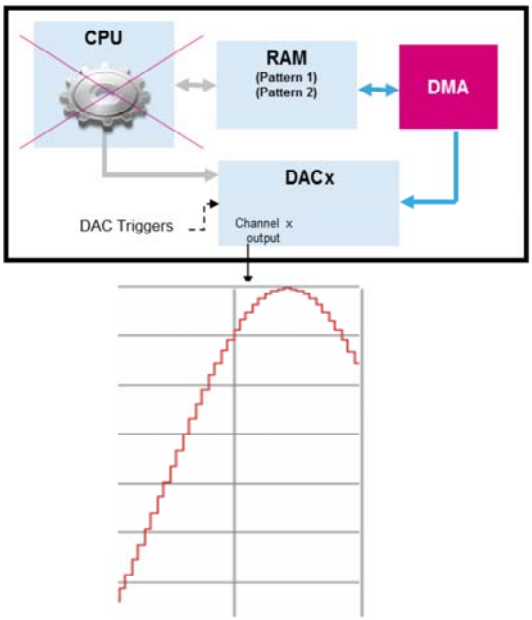
The increment value is defined by the STINCDATA bits in the DAC_STRx register.
The DAC output is used from 12 MSB of those counter value.
When the counter reaches 0x0000 or 0xFFFF, the value is saturated.
The sawtooth direction is defined by STDIR bit in the DAC_STRx register.

# DAC with DMA



## Offloads the CPU

- A DAC DMA request is generated when an external trigger occurs:
  - The Data Hold register value is then transferred to the Data Output register
  - Can generate a stable sampling time based output (timer controlled)
- DMA underrun with interrupt capability






The DAC can also issue DMA requests from the trigger signal.
Once a trigger is detected, the Data Hold register value is then transferred to the Data Output register.
Then the DMA request is generated to obtain the new data for the Data Hold register.
As the update of the Output Data register is initiated directly by the trigger signal, the DAC output signal will not have jitter, so that it can create a stable sampling time signal output, making it easy to filter out the sampling frequency.

# DMA double data capability



## Offloads the CPU

- DMA Double data mode (DMADOUBLEx bit = 1):
  - Allows transfer of 2 consecutive DAC samples in one DMA transfer
    - Consecutive samples for one DAC channel
  - DMA request is generated on each second DAC trigger
    - 2 samples are transferred in one 32-bit transaction
  - Implementation:
    - Two data hold registers (DAC_DHRx, DAC_DHRBx)
      Two output data registers (DAC_DORx, DAC_DORBx)
    - DMA transfer fills DAC_DHRx, DAC_DHRBx
    - Trigger switches between DAC_DORx, DAC_DORBx
      - DORSTATx bit indicates active registers pair

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The DAC supports a Double data DMA capability to reduce the bus activity.
A DAC DMA request is generated every two external triggers (except for software triggers) so that two samples are transferred in the same 32-bit AHB transaction.
In DMA double mode, DMA requests can only handle one DAC channel.
To use two channel outputs in DMA double mode, each DMA channel has to be configured separately.

# Interrupts and DMA



| Interrupt event | Description |
|---|---|
| DMA underrun | When a DMA request is not processed by the next external trigger |

| DMA event | Description |
|---|---|
| DMA request | External trigger when the DMAENx bits are set |

To transfer data from memory, a DMA request can be generated.
The DAC DMA request is not queued so that if a second external trigger arrives before the acknowledgment of the first external trigger is received (first request), then no new request is issued and an underrun flag is set that causes a maskable interrupt request.

# Low-power modes



| Mode | Description |
|---|---|
| Sleep | No effect, DAC used with DMA |
| Low power Run | No effect |
| Low power Sleep | No effect, DAC used with DMA |
| Stop 0/ Stop 1 | DAC remains active with a static value, if Sample & Hold mode is selected using the LSI/LSE clock |
| Standby | The DAC peripheral is powered down and must be reinitialized after exiting Standby or Shutdown mode |
| Shutdown | |



The digital-to-analog converter is active in the following low-power modes: Run and Sleep.
In Stop 0 and Stop1 modes, it remains active when Sample & Hold mode is selected.
In Standby and shutdown modes, the DAC is powered-down and it must be reinitialized afterwards.

## Performance



| | Condition | Value (typical) | Unit |
|---|---|---|---|
| VDDA | | 1.71 ~ 3.6 | V |
| Monotonicity | | 10 | bits |
| Differential Non Linearity (DNL) | | +/-2 | LSB |
| Integral Non Linearity (INL) | | +/-4 | LSB |
| Effective Number Of Bits (ENOB) 1 kHz output | Buffer on | 11.4 | bits |
| | Buffer off | 11.5 | bits |
| Consumption from VREF+ (1 Msps) | Buffer on | 185 | µA |
| | Buffer off | 155 | µA |
| Settling time (1 Msps) | +/-1 LSB, C = 50 pF | 1.6 | µs |
| Sampling rate | | 1.0 | Msample/s |
| | | 15.0 | Msample/s |

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The following table shows some performance parameters for the digital-to-analog converter. The DAC can work between 1.71 and 3.6 volts.
When DAC output buffer is ON or DAC_OUT pin is connected, the minimum VDDA voltage value is 1.8V.
10-bit monotonicity is guaranteed.
When operating at 1 Mega sample per second, Power consumption is 185 µA when the buffer is enabled and 155 µA when the buffer is disabled.
By using Sample & Hold mode, the current consumption can be drastically reduced. Depending on the condition and the hold capacitor characteristics, less than 1 µA current consumption is possible for this mode. The DAC buffered output has a settling time of 1.6 µsec with 50 pF load.
The DAC can handle a sampling rate of 1 mega sample per second or 15 mega samples per second.

# Related peripherals



- Refer to these peripherals trainings linked to this peripheral:
  - VREFBUF- Voltage Reference Buffer
  - RCC- Clock module
  - DMA – Direct memory access
  - Interrupts – Nested Vectored Interrupt Controller
  - GPIO – General-purpose inputs and outputs
  - TIM – Timers
  - OPAMP – Operational Amplifier
  - COMP – Comparators


This is a list of peripherals related to the DAC. Please refer to these peripheral trainings for more information if needed.

# References



- For more details, please refer to following resources
  - AN3126: Audio and waveform generation using the DAC in STM32 microcontrollers
  - AN4566: Extending the DAC performance of STM32 microcontrollers

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Application notes dedicated to DAC topics are also available.