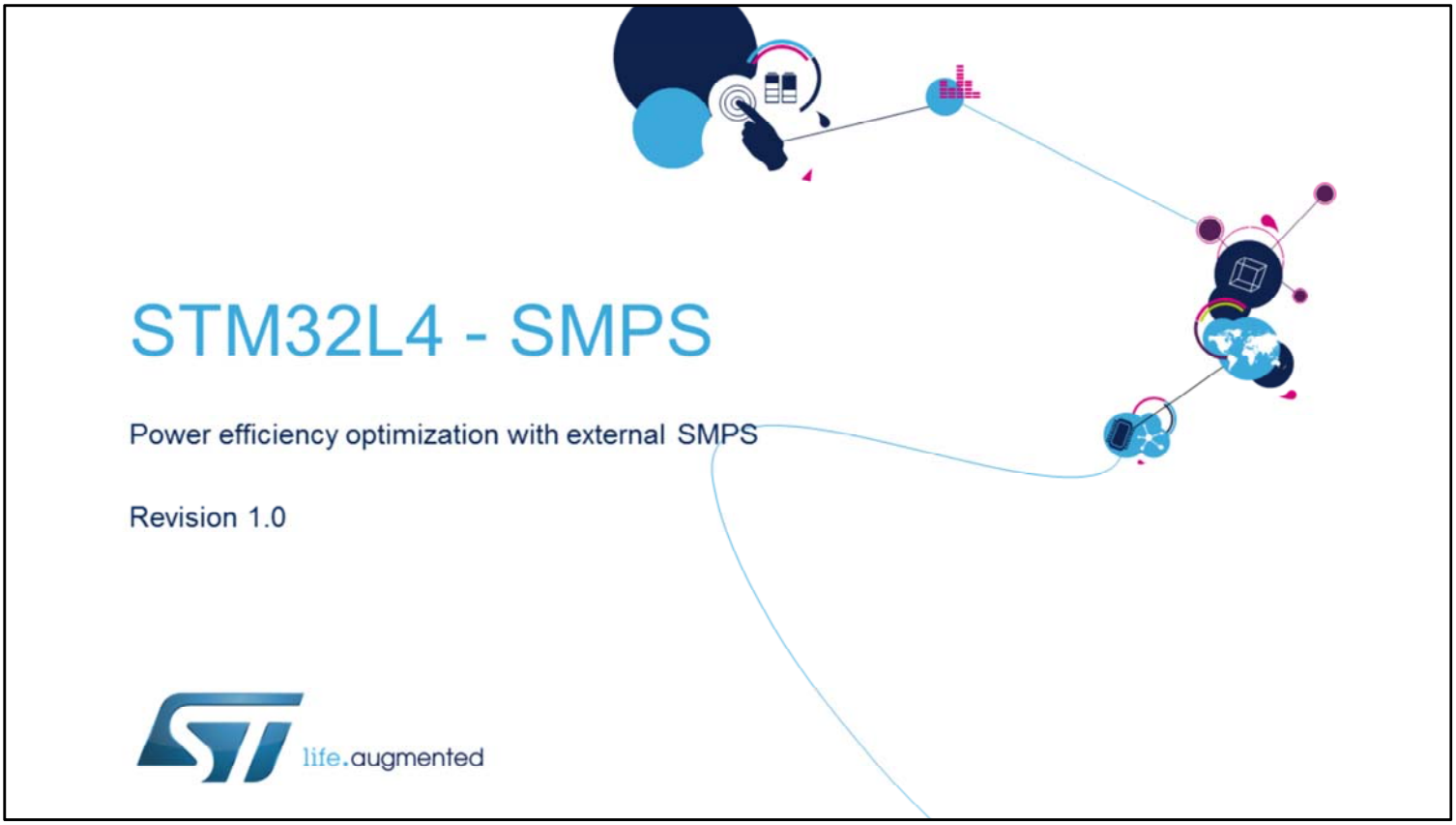
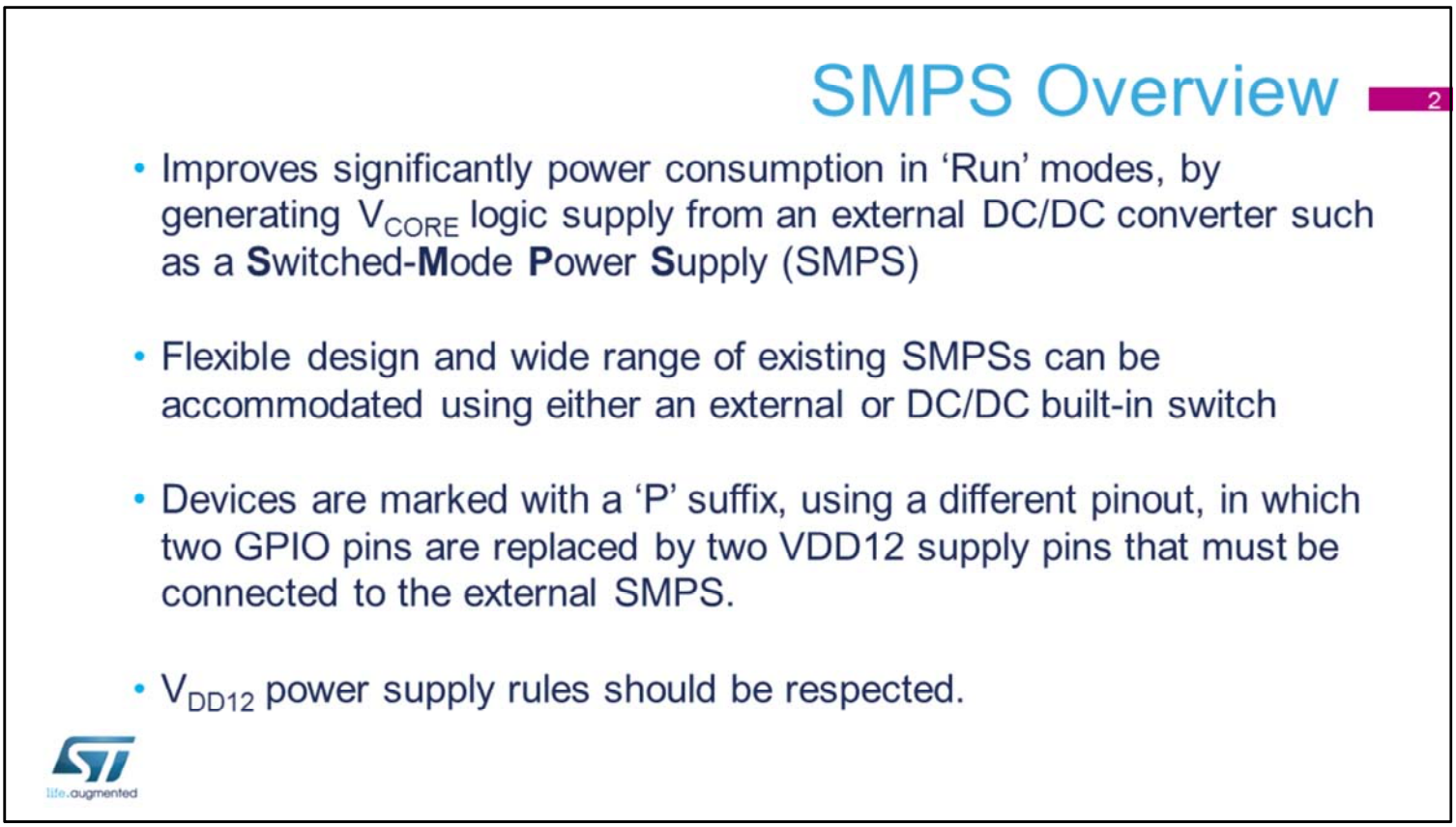
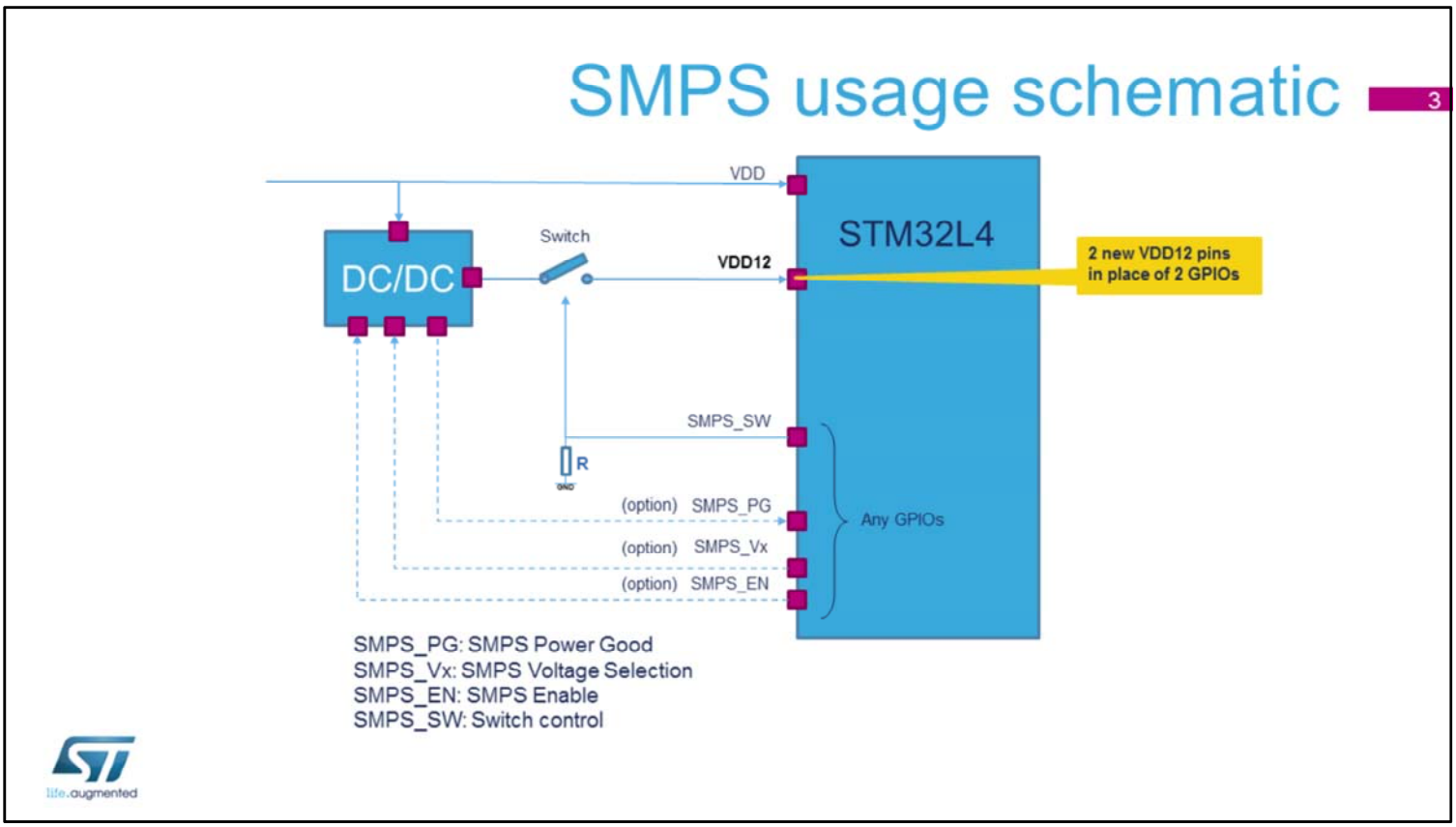


Hello, and welcome to this presentation of the STM32L4 power efficiency optimization with an external SMPS.



The use of an external switched-mode power supply (i.e. SMPS), with the STM32L4 series of ultra-low-power microcontrollers extends the power efficiency in 'Run' modes. By generating a V_{CORE} logic supply from an external DC/DC converter instead of the integrated LDO regulator. For example, it allows a power consumption gain up to 60% at V_{DD} = 3.3 V. This features is supported by devices marked with a trailing 'P' suffix, where two GPIO pins are replaced by a V_{DD12} logic supply connected to the external SMPS. A wide range of external SMPS can be accommodated, with the use of an external or built-in switch. For proper operating mode, the V_{DD12} power supply rules must be respected.

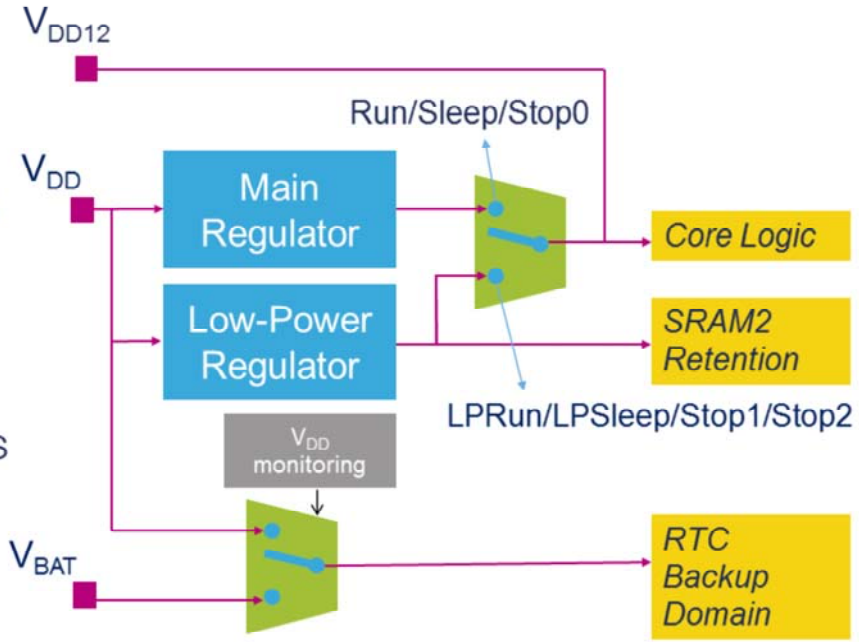


Here is a typical implementation of an external SMPS for an STL32L4 device with the use of two external components:
- the SMPS component, controlled by GPIOs if needed
- the Switch component, to isolate the VDD12 pins during low power modes or transitions phases, such as power-up or asynchronous reset.

The two GPIOs are chosen with the least impact in terms of functionalities and replaced by VDD12 pins. Please refer to the product datasheet for more details.

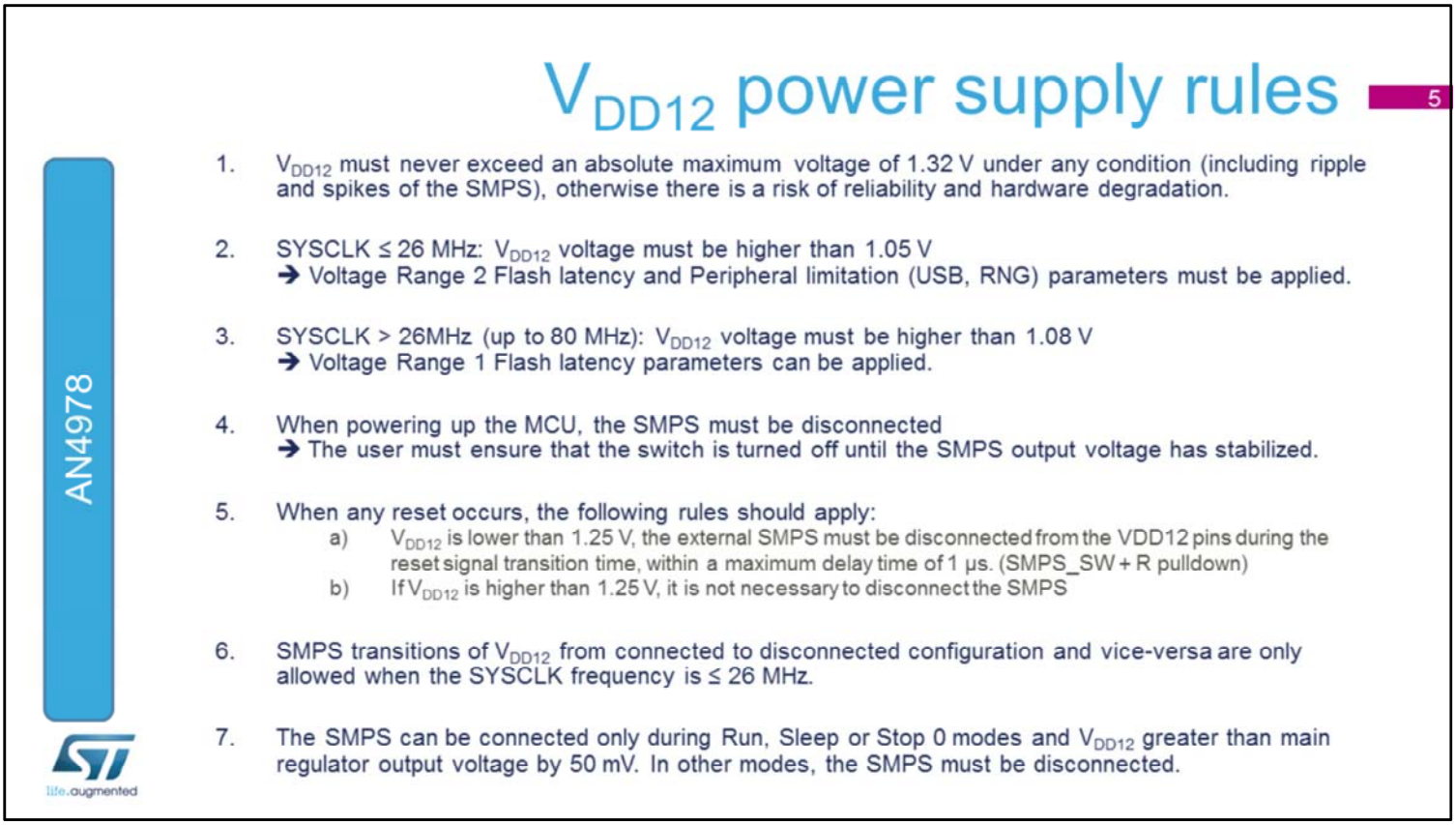
Voltage regulators and SMPS

- Two internal voltage regulators (LDO)
  - One Main regulator used in Run, Sleep and Stop 0 modes that **can be bypassed** by the SMPS via the VDD12 pins
  - One Low-power regulator for Low-power run, Low-power sleep, Stop , and Stop 2 modes in Standby that **must not be bypassed** by the SMPS via the VDD12 pins



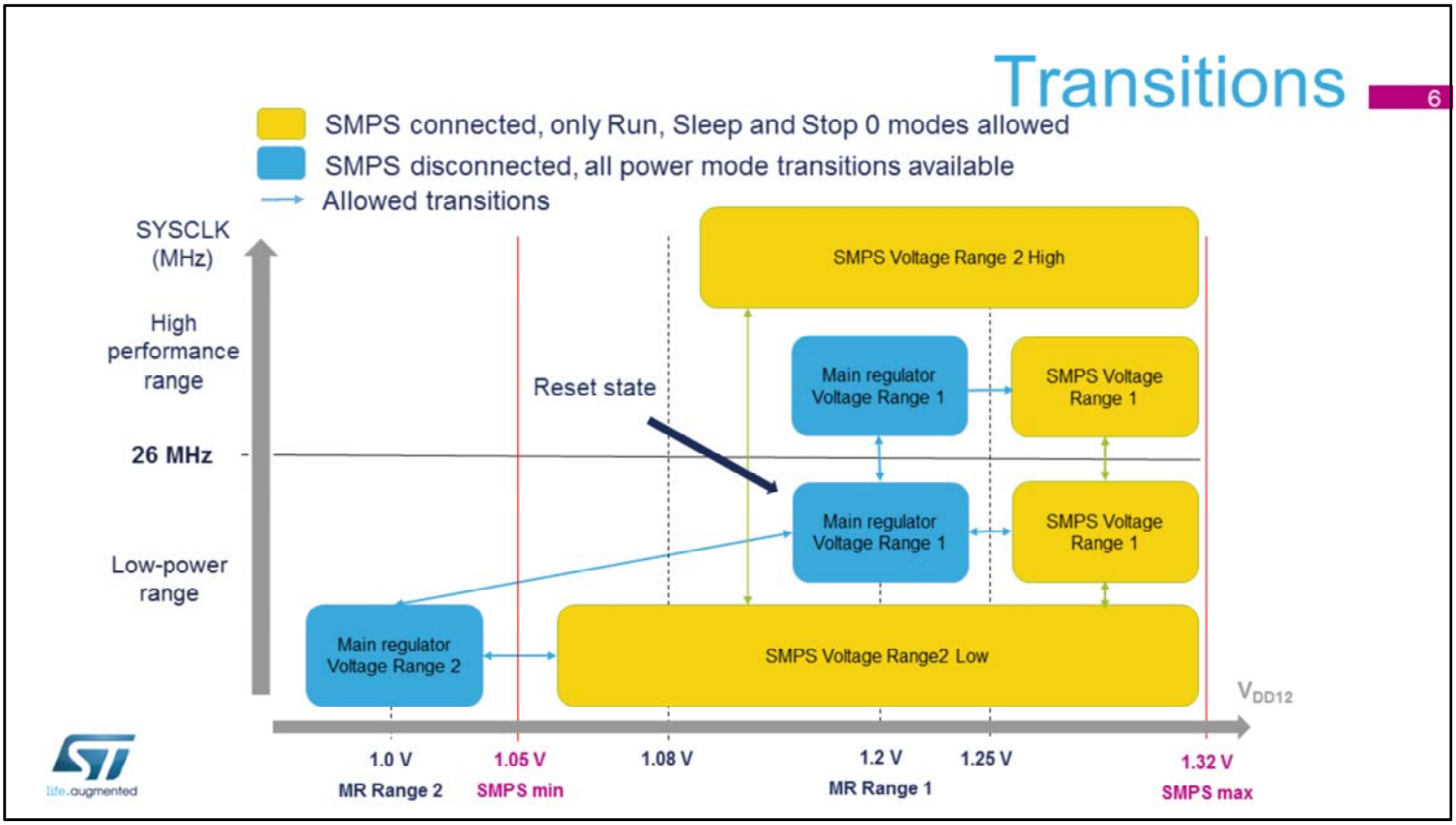
Two embedded linear voltage regulators, the Main and Low-Power regulators, supply all the digital circuitries except for the Standby circuitry and the Backup domain. When V_{CORE} is provided by the Main voltage regulator during Run, Sleep and Stop0 modes, the VDD12 can be supplied by the external SMPS by closing the external switch.

When V_{CORE} needs to be powered by the Low-power regulator during Low-power run, Low-power sleep, Stop 1 and Stop 2 modes or switched off during Standby and Shutdown modes, V_{DD12} must absolutely previously be disconnected from the external SMPS by opening the external switch to avoid any destructive impact on the regulator.



As the VDD12 voltage directly supplies the internal logic, the following rules should apply:
- VDD12 must never exceed 1.32 V
- VDD12 must be higher than 1.05 V when SYSCLK frequency is below or equal to 26 MHz
- VDD12 must be higher than 1.08 V when SYSCLK frequency is above 26 MHz
- During transition phase such as power-up or asynchronous reset, the VDD12 pins must be disconnected from the external SMPS
- Transitions from connected to disconnected configuration are only allowed when the SYSCLK frequency is below 26 MHz
- The SMPS can only be connected to the device during Run, Sleep or Stop 0 modes and when VDD12 is greater than the main regulator output voltage by 50 mV. In other power modes, the SMPS must be disconnected.

Please have a look at the application note AN4978 for more information.

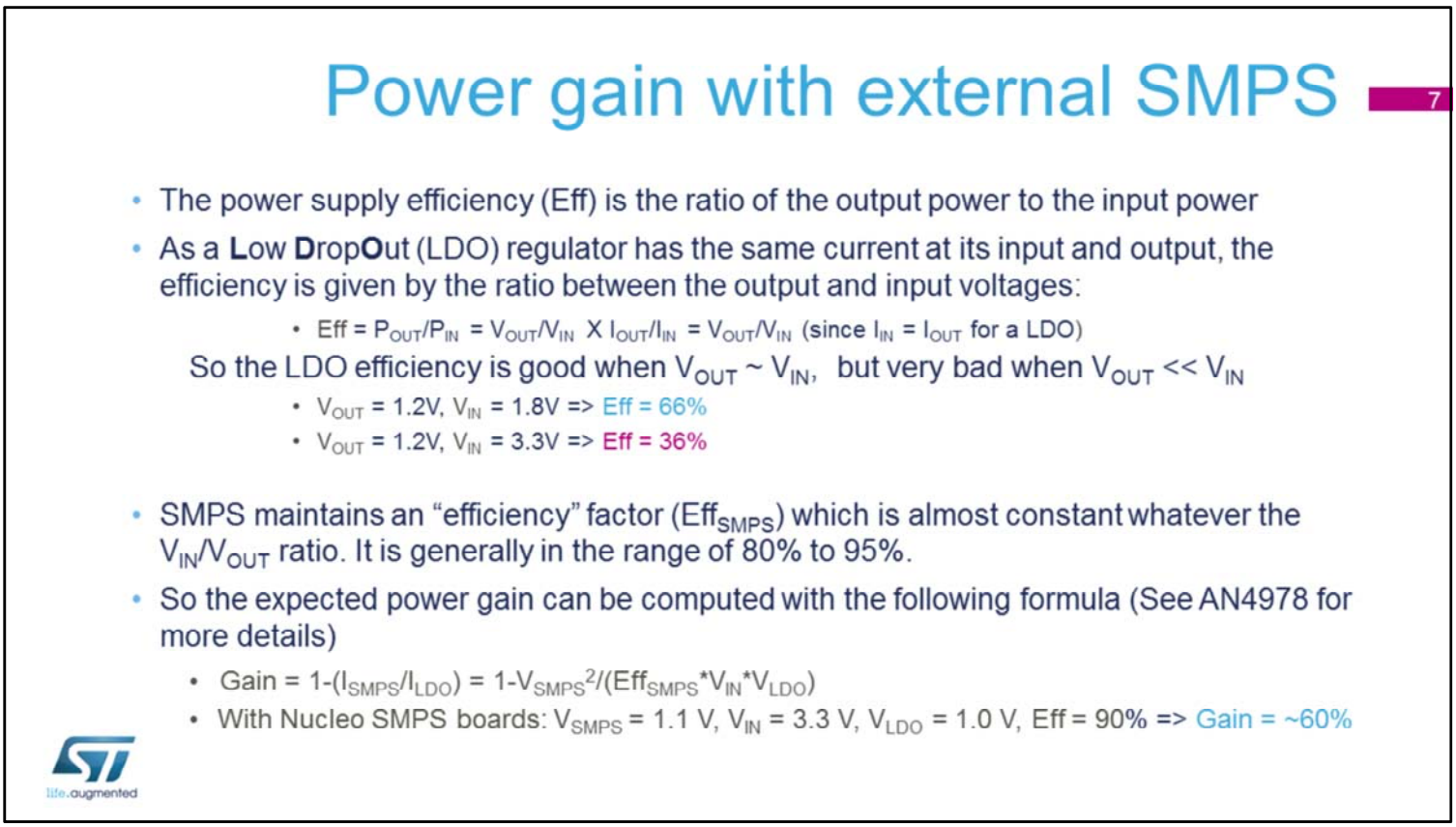


This graph summarizes the power supply rules allowing safe transitions.

After reset, the system clock frequency is 4 MHz and the main voltage regulator is in Voltage Range 1 supplying a V_{CORE} at 1.2 V.

If the SMPS supply voltage is greater than 1.25 V, the SMPS can be connected and then the system frequency increases to reach maximum performance possible in this low power range.

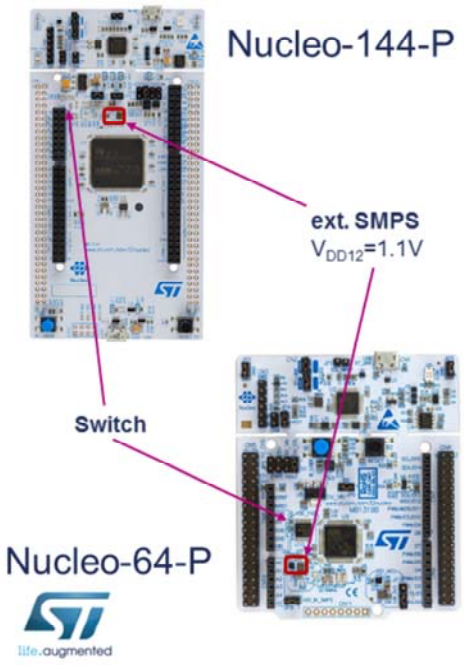
If the SMPS supply voltage is lower than 1.2 V, switch the Main regulator to Voltage Range 2 and then the SMPS can be connected. In this mode, the chip can run in high performance range when the SMPS voltage is greater than 1.08 V.

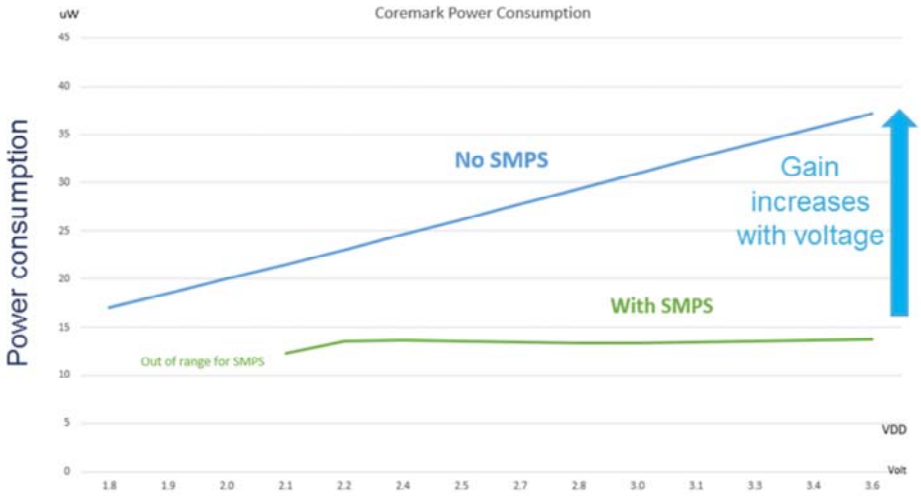


The expected power gain with the external SMPS is directly linked to the power efficiency of the regulator. The STM32L4 microcontroller embeds low dropout regulators whose power efficiency is given by the ratio of the output voltage to the input voltage. When the output voltage is close to the input, the power efficiency is good, but can get worse as soon as the input voltage increases.

On the contrary, the SMPS power efficiency remains almost constant whatever the voltage input ratio, generally between 80% to 95% depending on its input voltage and current load. We can compute the expected power gain with the provided formula (See AN4978 for more details). As an example, the Nucleo SMPS board has a gain of around 60% at input voltage 3.3 V.

Nucleo board power consumption





STM32L496 CoreMark power consumption
@ 80 MHz V_{DD12} = 1.1 V on Nucleo-144 SMPS board

Here is an example of the power consumption graph of a CoreMark™ at 80 MHz as a function of the VDD supply using a STM32L496ZG microcontroller on a Nucleo-144 SMPS board. We can clearly see the power gain increasing with the voltage.

References

9

- For more details, please refer to following resources:
  - AN4978: Design recommendations for STM32L4 with an external SMPS, for ultra-low-power applications with performance
  - Product datasheet for the available packages supporting the external SMPS feature.

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For more details, please refer to the application note “Design recommendations for STM32L4 with external SMPS”.
Please also refer to the product datasheet for the available packages supporting the external SMPS feature.