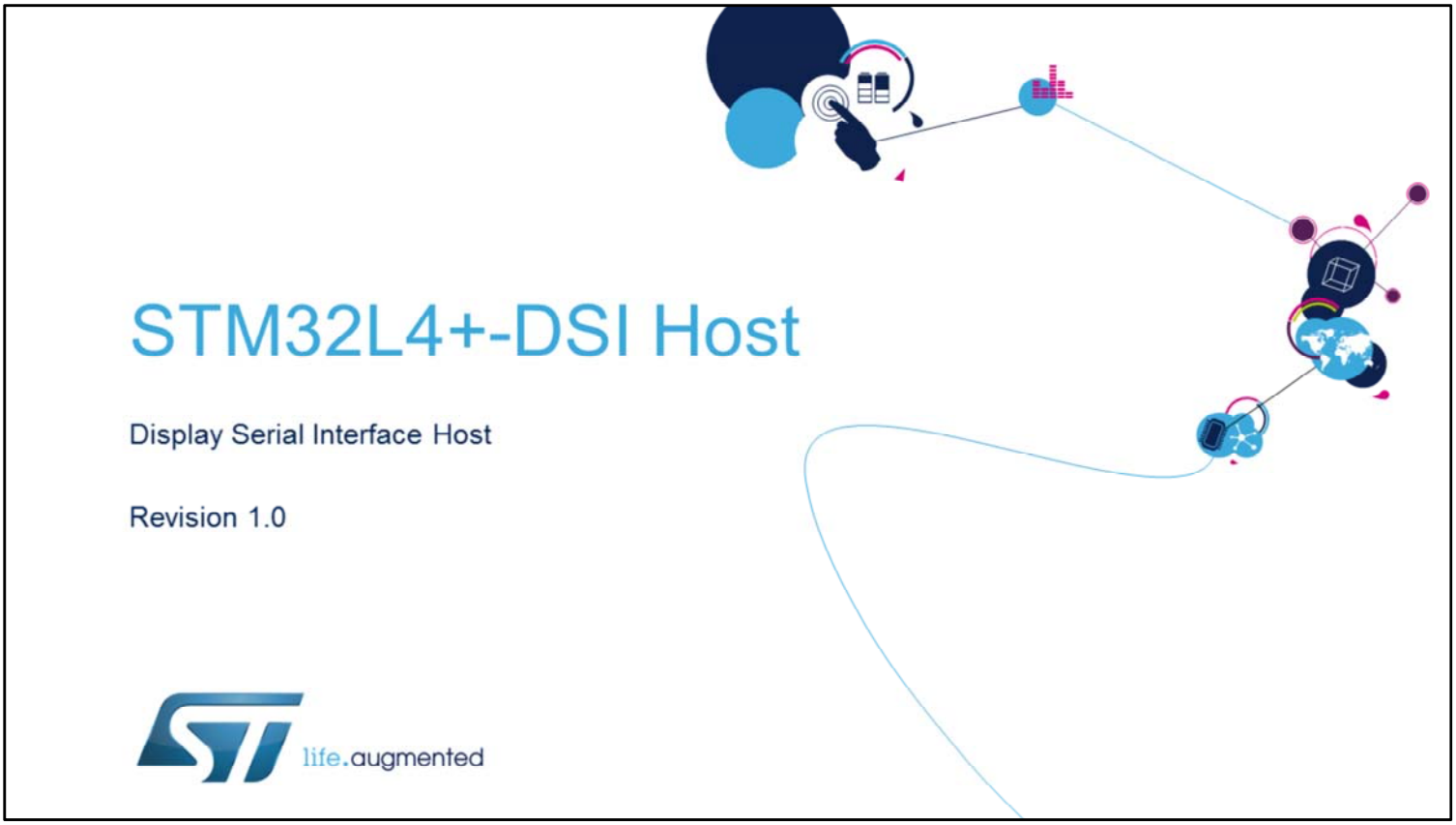
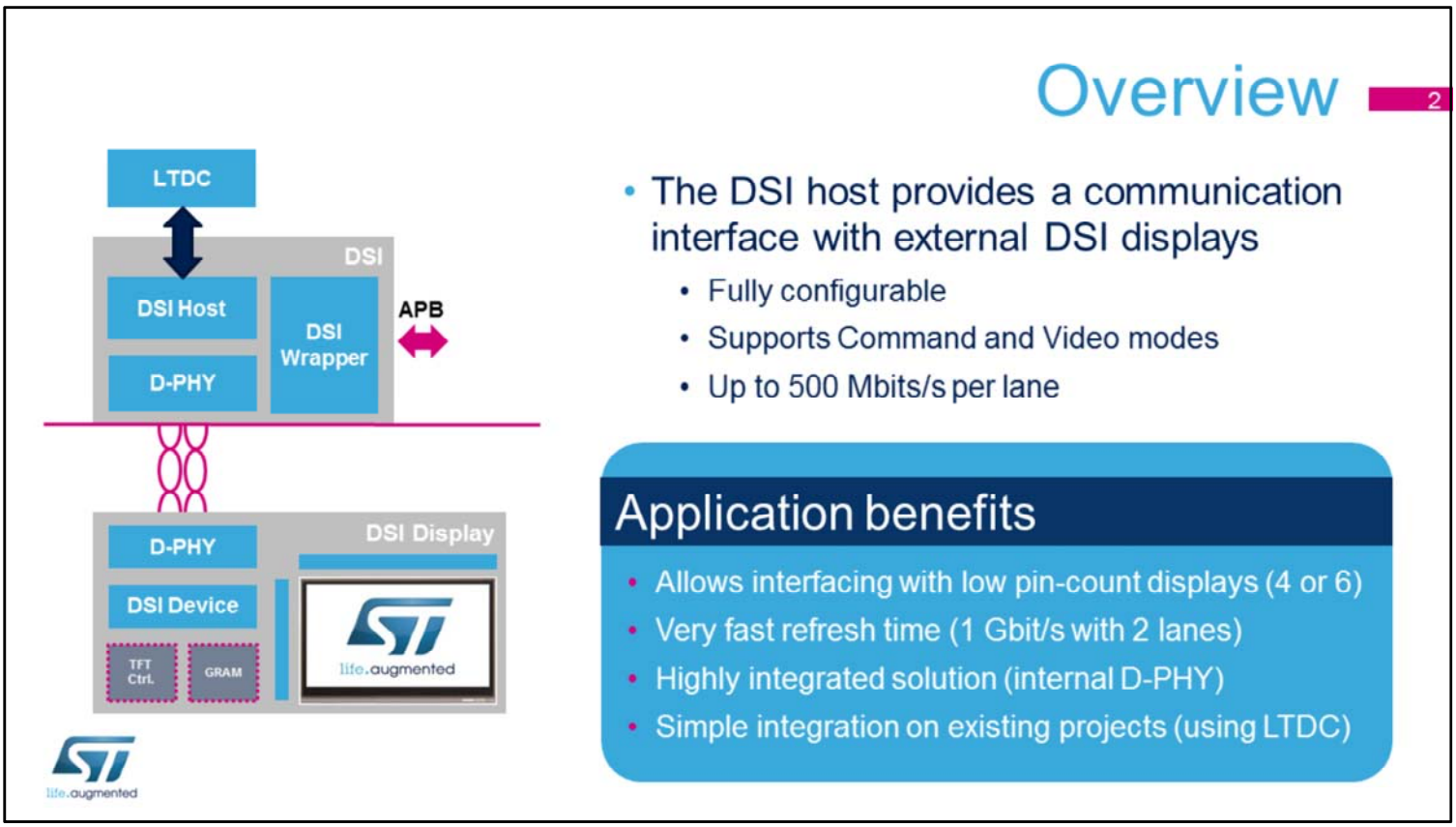
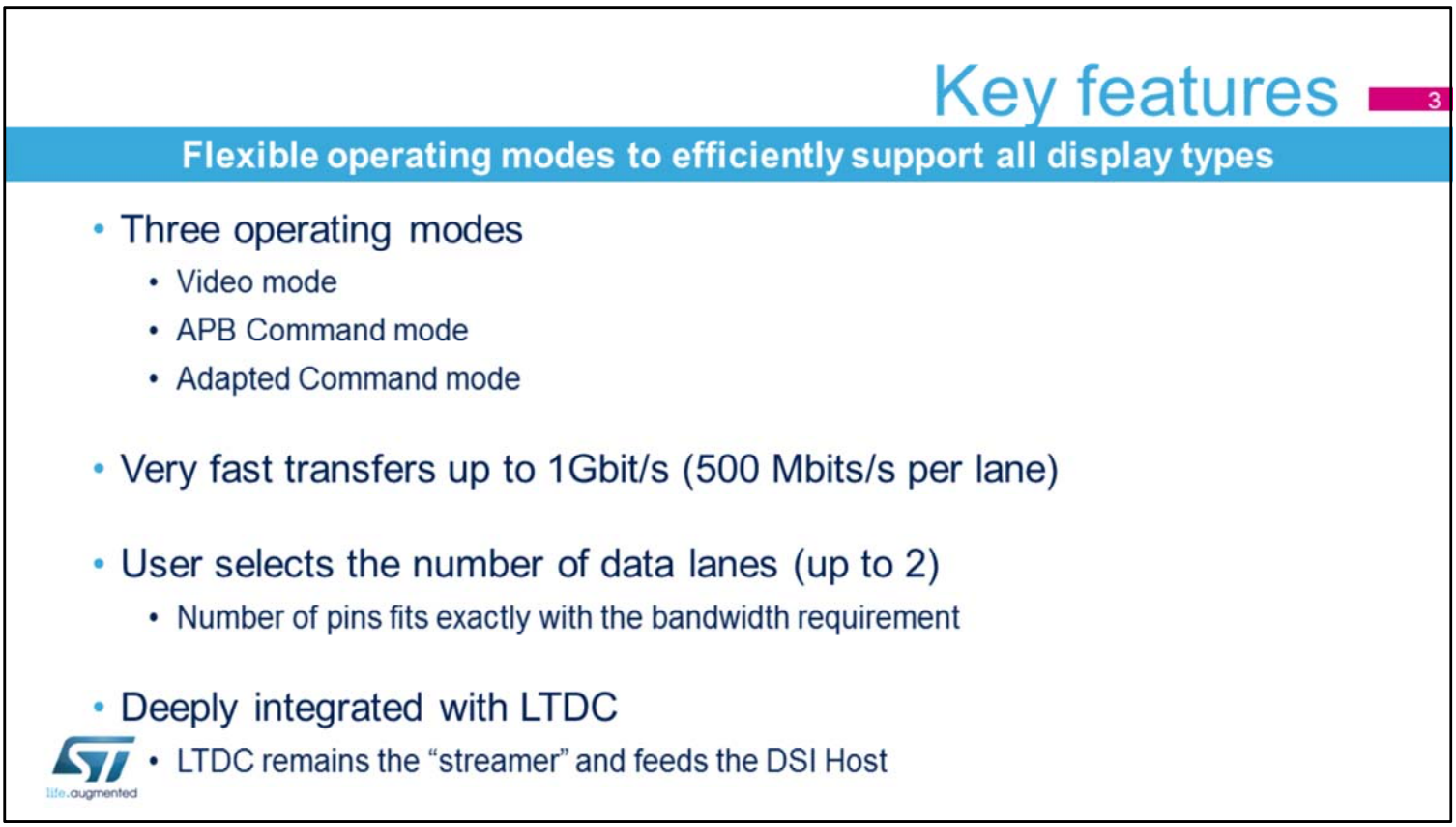


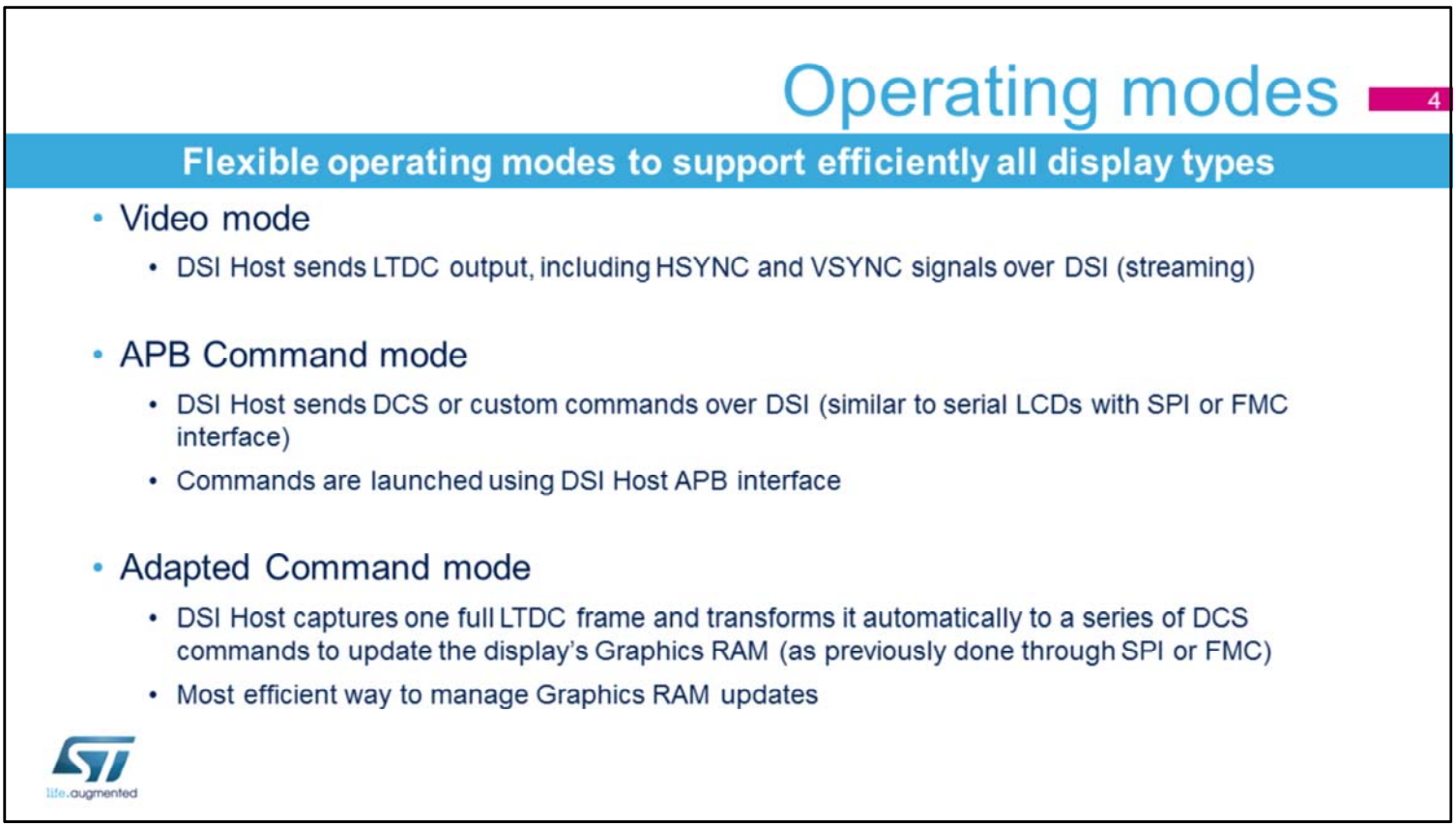
Hello, and welcome to this presentation of the STM32 Display Serial Interface (DSI) Host. It covers the features of this interface, which is used for connecting graphical displays to the microcontroller.



The DSI Host integrated inside STM32 microcontrollers provides a high-speed communication interface allowing the microcontroller to communicate with a display with a reduced pin count. This interface is fully configurable, making it easy to connect DSI displays available today on the market.
Applications benefit from the easy connection and reduced pin count.



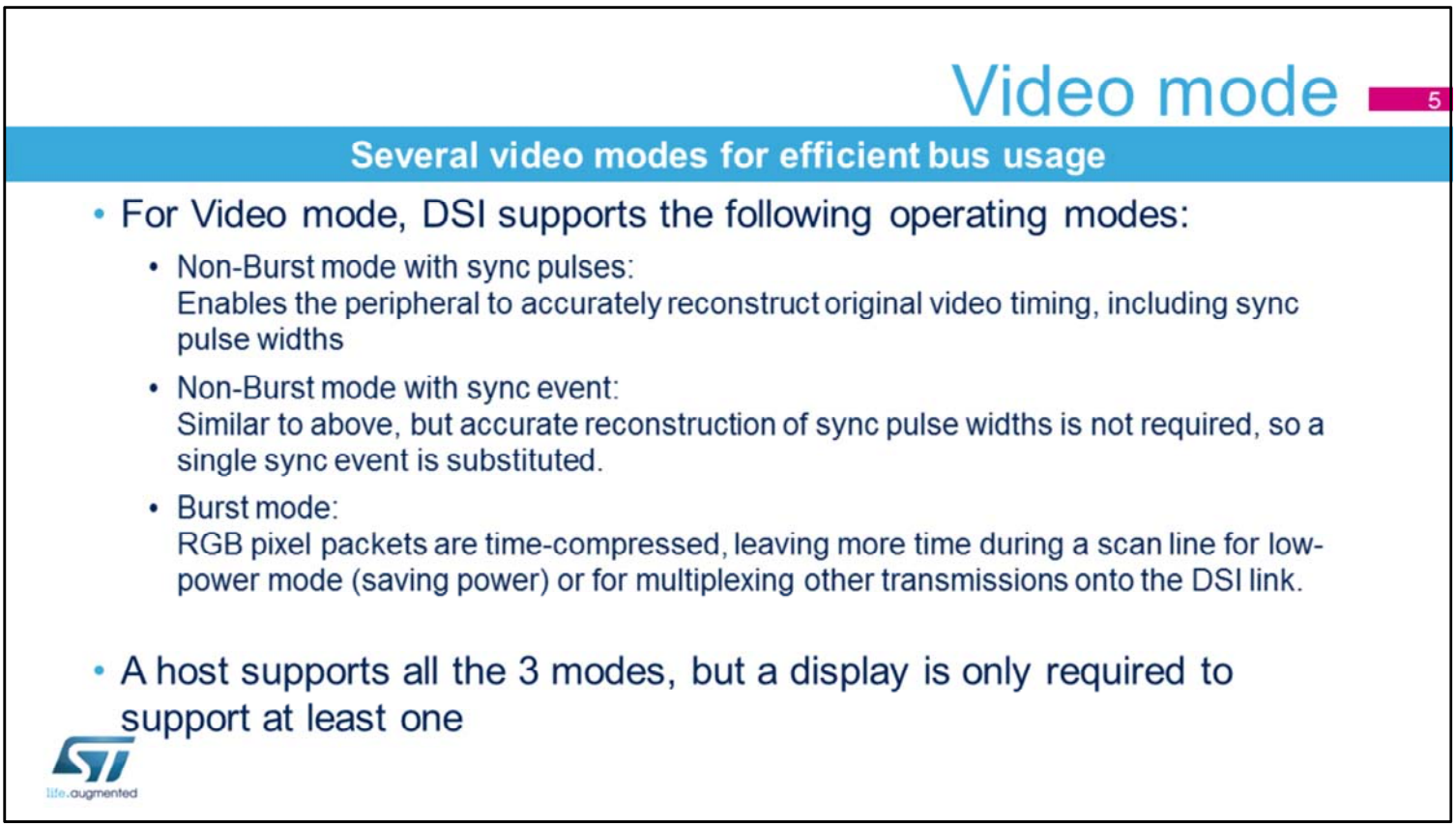
The DSI Host integrated inside STM32 microcontrollers offers three operating modes and is optimized for communication with graphical displays with a reduced pin count up to a 1Gbit/s. The number of data lanes is configurable to fit exactly with the application’s needs. The DSI Host is deeply integrated with the LCD-TFT display controller (LTDC) to ease application development and porting.



Three operating mode are available to convey the graphical data to the display:

- Video mode streams over the high-speed link the RGB data and the associated synchronization signals directly generated by the LTDC. The streaming starts as soon as the DSI Host and the LTDC are enabled. This continuous refresh is the best way to interface with a display without Graphics RAM (GRAM [“G” “RAM”]) .
- APB command mode sends commands over the high-speed link for configuration as it is done using a legacy serial interface (SPI, FMC). The commands are launched using the DSI Host APB interface.
- Adapted command mode is the best way to interface with a display having its own internal Graphics RAM. The DSI Host captures only one full frame coming from the LTDC and transforms it into a series of write

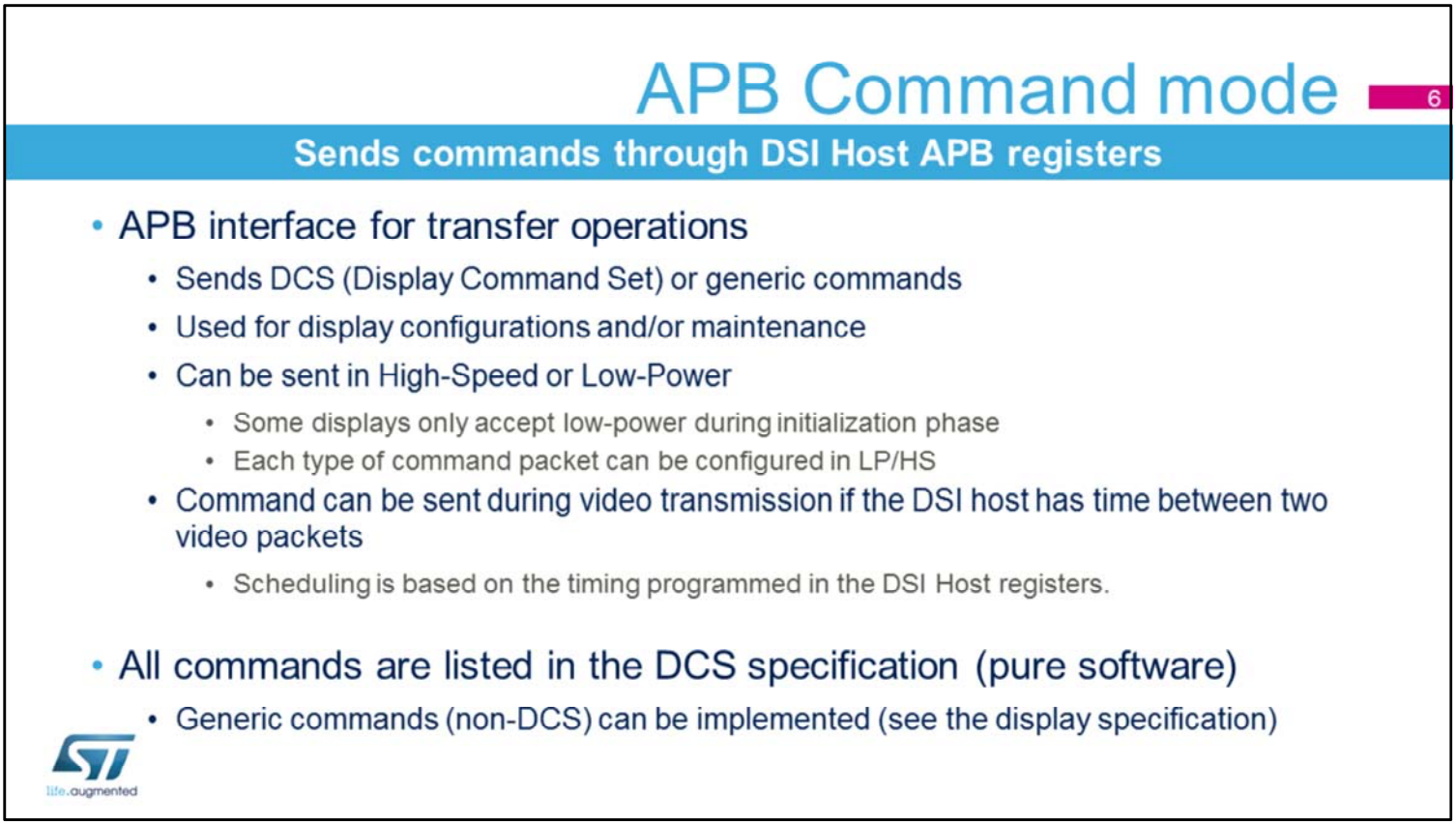
commands to update the display Graphics RAM. This one-shot refresh automatically sets a control bit in the DSI Host.



The DSI Host's Video mode supports the three operating modes defined by the Mobile Industry Processor Interface (MIPI) DSI specification:

- Non-Burst with sync pulse: where the synchronization signal and the data are sent accurately enabling the target display to reconstruct the original video timings, including synchronization pulse widths without any buffering.
- Non-Burst with sync event mode is similar to the previous mode but for displays not requiring synchronization pulse width information.
- Burst mode is the most energy-efficient mode. RGB pixel packets are time-compressed, leaving time during a line transmission to go into low-power mode or to transmit other commands.

The DSI Host must support all three modes. A display is only required to support at least one of these three modes.



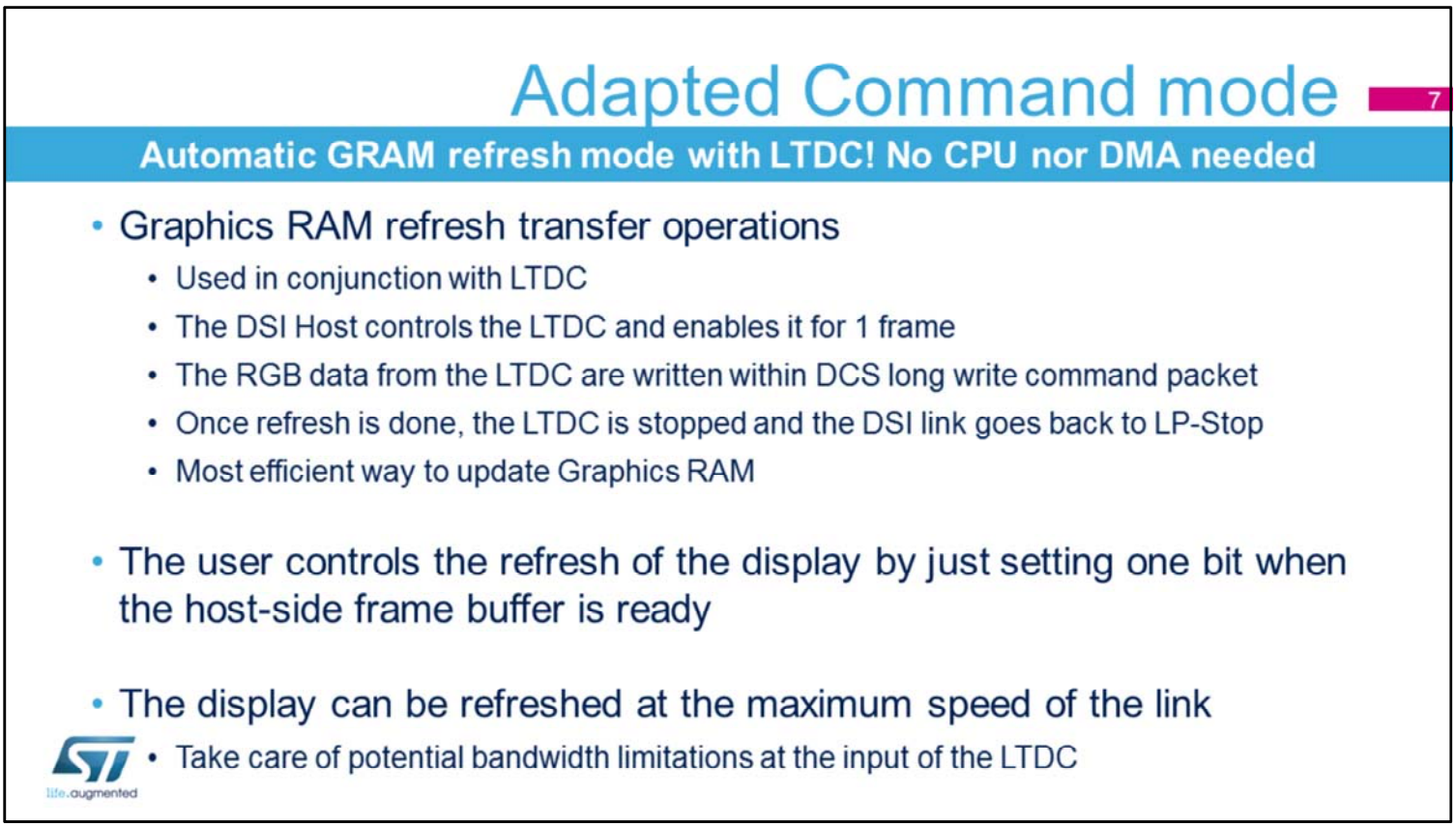
APB Command mode is used to send commands through the DSI Host APB register interface.

Generic or Display Command Set (DCS) commands can be sent for display configuration at startup or for maintenance operations when the application is running.

All the commands can be sent either in high-speed or in low-power modes as some displays only accept low-power communication at startup.

Commands can also be sent during video streaming: the DSI Host scheduler automatically evaluates if it has the sufficient time to insert a command during a video transmission according to the programmed timings.

All the commands are fully programmable by software, which means the DSI Host supports all the standard DCS commands and all the display-specific custom commands.

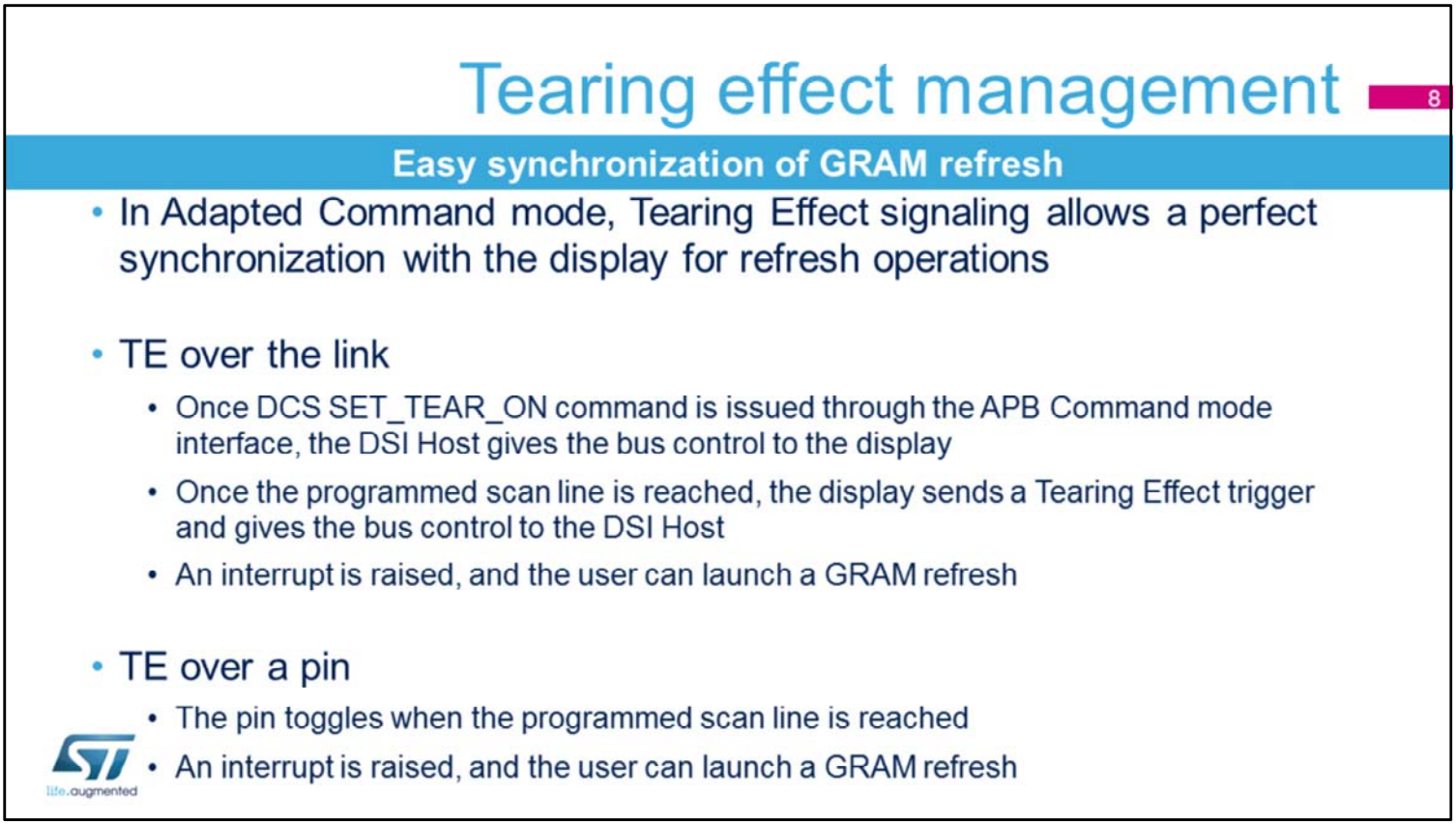


Adapted Command mode is a highly optimized operating mode to interface with displays having their own graphics RAM.
It automatically refreshes the display's Graphics RAM (GRAM) with the LTDC without any load on the CPU or DMA controller.
The Graphics RAM refresh operation works in conjunction with the LTDC:

- The DSI host controls the LTDC and enables it for 1 frame.
- The RGB data coming from the LTDC are captured and are sent into a series of DCS long write command packets to the display.
- Once the Graphics RAM is completely refreshed, the DSI Host automatically stops the LTDC and the DSI link goes into Low-power Stop mode.

The user controls the refresh operation of the display by

just setting one bit when the frame buffer is ready to be sent.
The display can be refreshed at the maximum speed of the link so special attention must be given on the bandwidth requirement on the LTDC side (e.g., memory bandwidth to read the frame buffer).



The tearing effect allows a perfect synchronization between the display and the DSI Host for refresh operations on displays having their own Graphics RAM.

The tearing effect can be signaled in two ways:

- Over the link without an additional pin,
- Or using an additional pin.

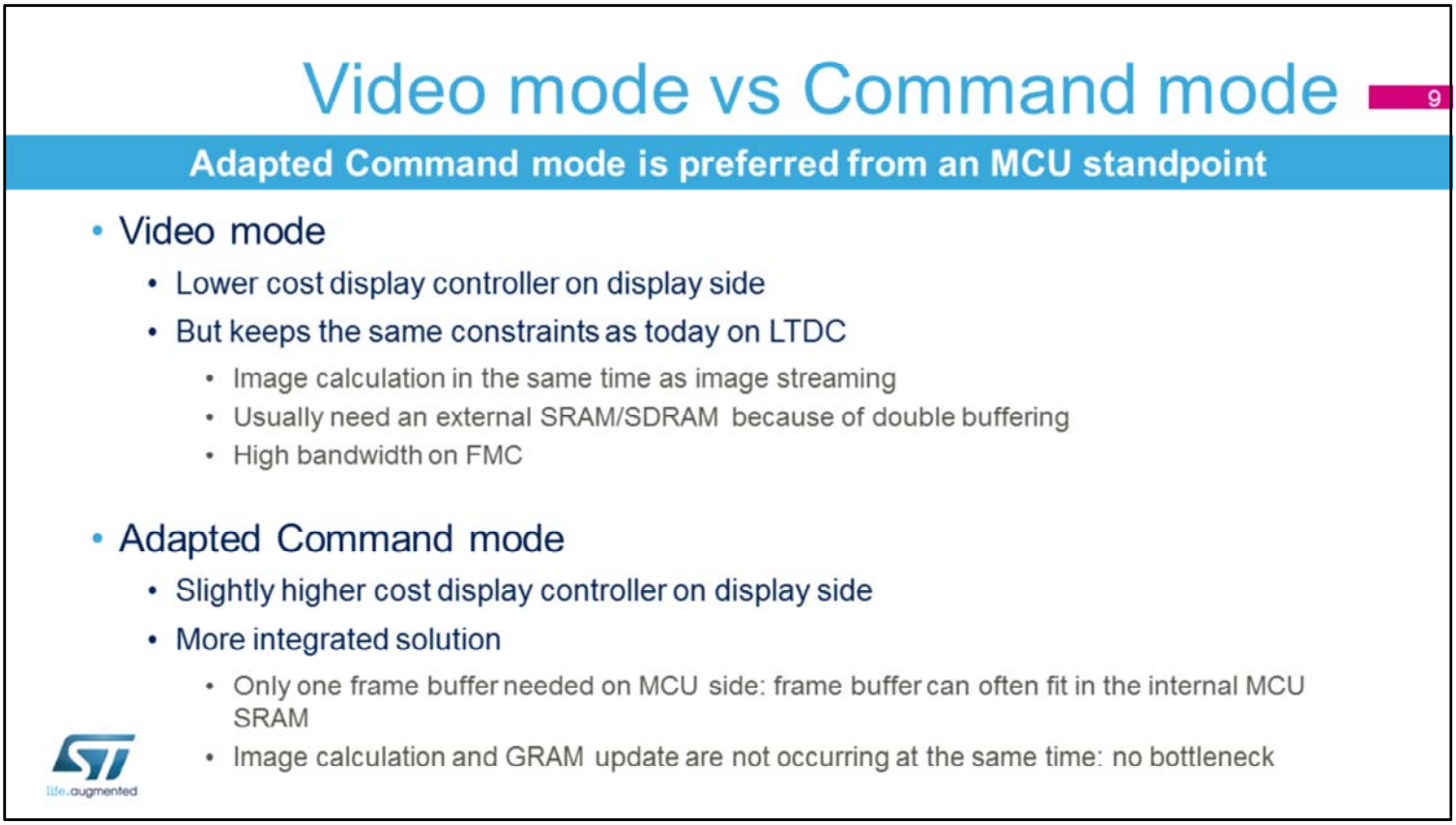
When the tearing effect is signaled over the link, the DSI host sends a SET_TEAR_ON command and gives the control of the bus to the display. Once the programmed scan line is reached by the display, it sends a trigger to the DSI Host and gives control of the bus back to the DSI Host.

An interrupt can be raised to launch the Graphics RAM refresh.

When the tearing effect is signaled over a pin, the

display toggles a dedicated GPIO to trigger the DSI Host when the programmed scan line is reached. Although an additional pin is required, this mechanism avoids having multiple exchanges over the link between the DSI Host and the display.

An interrupt can be raised on the pin toggling the launch the Graphics RAM refresh.



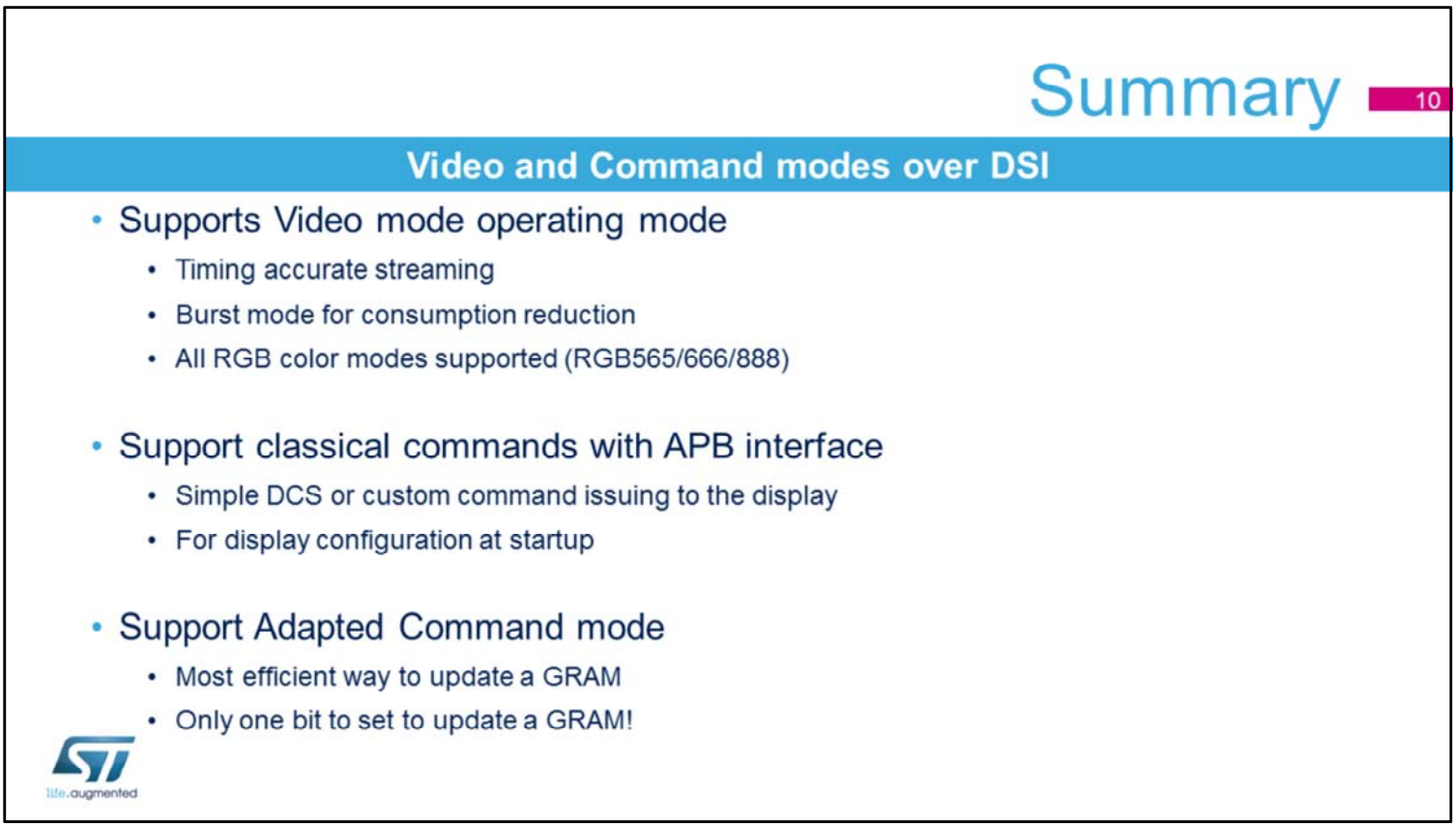
The choice between Video or Adapted Command mode has a big impact on the solution's architecture and cost.

From the MCU standpoint, Adapted Command mode is preferred for cost-optimized solutions.

As Video mode does not require Graphics RAM on the display side, this solution is often used for large displays which reduces cost. The constraints in term of bandwidth and memory usage on the MCU side remains the same as for today's LTDC-based solutions. Most of the time an external RAM is required for double-buffering of the frame buffer.

Adapted command mode requires a display with a Graphics RAM. The display may have a slightly higher cost, but most of the displays smaller than 480 by 480 pixels embed a Graphics RAM. As a consequence,

Adapted Command mode with a small display will not always require an external RAM as the frame buffer may fit in the internal MCU RAM. This highly reduces the bandwidth issues on the MCU and reduces the overall BOM cost and solution integration as no external RAM is required.



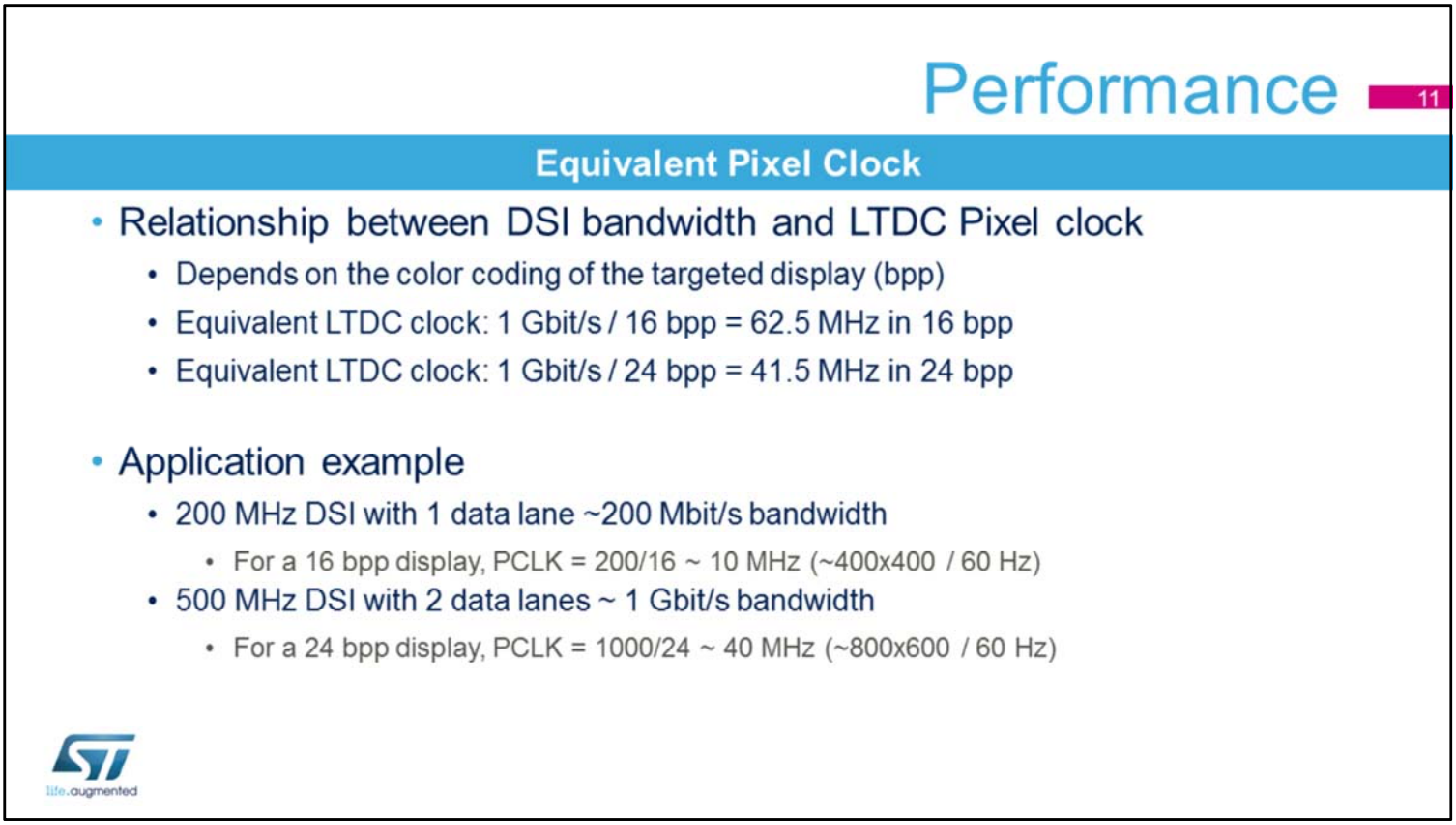
The DSI Host supports Video mode operation with:

- Timing accurate streaming
- Burst mode to reduce consumption during blanking periods
- Several RGB color encoding formats to optimize bandwidth usage

The DSI Host supports commands through its APB interface:

- DCS or generic commands can be issued to the display even when Video mode is working
- Commands are used for display configuration at startup and also for maintenance operations when the application is running

The DSI host can also use Adapted Command mode to update a display's Graphics RAM without having to use the CPU or DMA controller. This mode works using the LTDC to transmit write commands to the display.



In terms of performance, there is a relationship between the equivalent pixel clock and the DSI Host configuration.

Depending on the color coding, the number of data lanes used and the speed of the data lanes, we can evaluate the equivalent pixel clock.

As an example, when using two lanes at 500 Mbits/s (pronounced Mega bit per second) for a total of 1 Gbit/s (pronounced Giga bit per second), we have a maximum equivalent pixel clock of 62.5 MHz (pronounced Megahertz) for a 16 bits per pixel coding and 41.5 MHz for a 24 bits per pixel coding.

In terms of the application, we can have, for example, a small 400 by 400 pixel display running on a single 200 Mbits/s lane at 16 bits per pixel or a large 800 by 600 pixel display at 24 bits per pixel running on both data lanes at 500 Mbits/s each.

Equivalent Pixel Clock

- The DSI Host has interrupt sources for all the events which could occur on the link in the controller
  - Refer to the reference manual for a detailed description
- The DSI Host generates additional interrupts for
  - Regulator events
  - PLL events
  - Tearing Effect events
- No DMA request is necessary for the DSI Host as it works with the LTDC (which has its own DMA master)

life.augmented

The DSI Host has many interrupts to monitor all the timings and events of the communication. Please refer to the reference manual for a detailed description of all the interrupt sources.
In addition to protocol-related interrupts, the DSI Host also provides interrupts to manage:

- Regulator events,
- PLL events,
- Tearing effect events.

As the DSI Host uses the LTDC for data fetching, no DMA controller is necessary (the LTDC has its own DMA master).

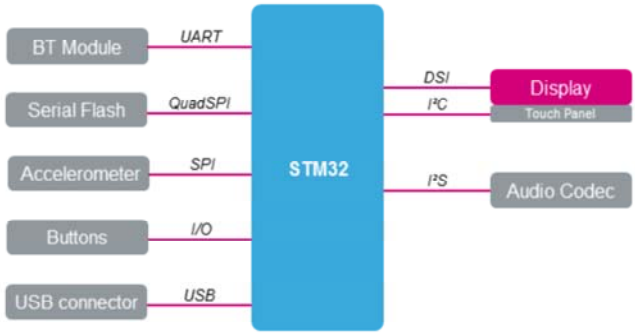
Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

The DSI Host is active in Run and Sleep modes. A DSI Host interrupt can cause the device to exit Sleep mode. In Stop mode, the DSI Host is frozen and its register content is kept. In Standby mode, the DSI Host is powered-down and it must be reinitialized afterwards.

Application examples

- Applications including connectivity and user interface:
  - 400x400 / 24 bpp display with embedded GRAM (no need for external RAM)
  - QSPI to store graphical primitives



Wearable applications require low-power management functions together with a high-quality user interface. This can be achieved using the DSI Host to interface with a display through only 4 or 6 pins. The low pin-count needed to drive such devices allows for a highly optimized system integration.

Related peripherals

- Refer to these peripheral training modules linked to this peripheral:
  - RCC (DSI clock control, DSI enable/reset)
  - Interrupts (DSI interrupt mapping)
  - GPIOs (DSI input for tearing effect)
  - LTDC (DSI pixel source, timing control)

You can refer to the training slides related to RCC, interrupts, LTDC, and GPIOs for additional information.