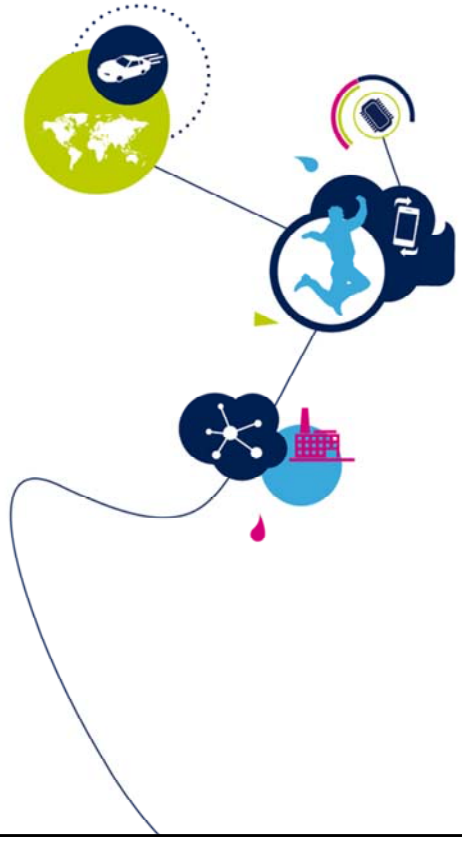
STM32G4 - COMP

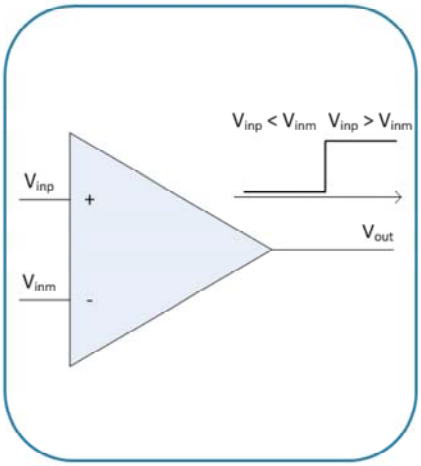
Analog Comparators
Revision 1.0



life.augmented

Hello, and welcome to this presentation of the STM32G4 analog comparators. It covers the main features of the ultra-low-power comparators and gives some application examples.

Overview



- Compares two analog signals and provides a digital output indicating which is larger
- Capability to wake up the CPU from Stop mode
- Motor control focus: cooperation with timers (TIMs, HRTIM), DACs, Vrefint

Application benefits

- Safety features such as the configuration lock or break event generator for timers
- Flexible I/O interconnections
- Hysteresis and speed vs. consumption configuration
- ~15 ns propagation delay

life.augmented

Up to seven analog comparators inside STM32 microcontrollers provide a binary output which indicates if the analog voltage on the plus input is larger than the voltage on the negative input.
It allows the MCU to react when the analog signal crosses a predefined threshold.
The comparator continuously monitors voltage in contrast to an analog-to-digital converter which operates in sampled mode.
The comparator can be used to wake up devices from Sleep and Stop modes.
Motor control loop is simplified by enabling a cooperation between the following units: comparators, timers, DACs and VREFINT.
Applications can benefit from the flexible configuration of comparator properties which can be locked for safety reasons.

Another safety feature of the comparator is its ability to generate a break signal for timers allowing to safely stop the generation of PWM driving signals.
Delay between analog threshold crossing and digital output assertion is less than 15 ns.

Key features

3

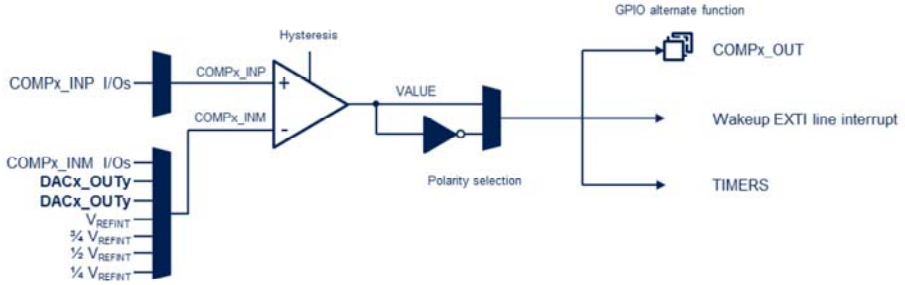
- Up to 7 independent comparators
- Programmable hysteresis
- Configurable plus and negative inputs
  - Multiplexed I/O pins, DAC channels 1 and 2, internal reference voltage and its three submultiple values
- Output redirection
  - Configurable I/Os
  - Timer – break event for fast PWM shutdown, cycle-by-cycle current control, and input capture for timing measurements
  - Output blanking source
- The comparator control and status registers can be write-protected

life.augmented

STM32G4 microcontrollers implement up to 7 comparators.
The comparator includes a programmable hysteresis to avoid spurious output transitions with noisy input signals
It offers flexible inter-connections of inputs and outputs allowing the selection of thresholds for several external and internal inputs such as DAC outputs or internal reference voltage outputs.
The comparator output can be connected to I/Os using the alternate function channels or internally redirected to a variety of timer inputs, enabling the break event for fast PWM shutdown.
It is also possible to create cycle-by-cycle current control or input captures for timing measurements.
The COMPx control registers can be locked until the next microcontroller reset.

COMP block diagram

	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7
STM32G43x	✓	✓	✓	✓			
STM32G44x	✓	✓	✓	✓			
STM32G47x	✓	✓	✓	✓	✓	✓	✓
STM32G48x	✓	✓	✓	✓	✓	✓	✓



The number of comparators depends on the exact reference of the STM32G4 microcontroller.
STM32G43x and STM32G44x series implement 4 comparators while STM32G47x and STM32G48x series implement 7 comparators.
The figure shows the general block diagram of the comparator integrated in STM32G4 microcontrollers.
The multiplexors on the left select the voltage sources to be compared: GPIOs, DAC outputs, VREFINT with four divide ratios.
The output of the comparator can be inverted.
The state of the comparator can be connected to:

- GPIOs
- EXTI module to generate a wakeup request or an event to the CPU
- Timer inputs.

It is possible to have the comparator output

simultaneously redirected internally and externally.

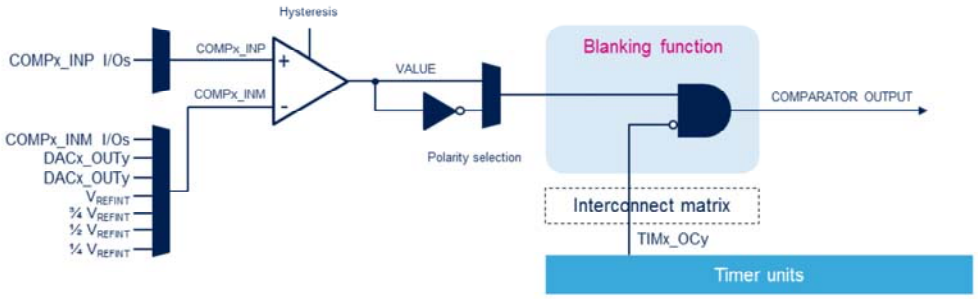
COMP inputs

COMP	NM			NP	OUT	
	External	Internal		External	External	Internal
COMP1	PA4, PA0	DAC3_CH1 DAC1_CH1	¼, ½, ¾, 1 Vrefint	PA1, PB1	PA0, PA6, PA11, PB8, PF4	TIMs, HRTIM, EXTI signals
COMP2	PA4, PA2	DAC3_CH2 DAC1_CH2		PA7, PA3	PA2, PA7, PA12, PB9	
COMP3	PF1, PC0	DAC3_CH1 DAC1_CH1		PA0, PC1	PB7, PB15, PC2	
COMP4	PE8, PB2	DAC3_CH2 DAC1_CH1		PB0, PE7	PB1, PB6, PB14	
COMP5	PB10, PD13	DAC4_CH1 DAC1_CH2		PB13, PD12	PA9, PC7	
COMP6	PD10, PB15	DAC4_CH2 DAC2_CH1		PB11, PD11	PA10, PC6,	
COMP7	PD15, PB12	DAC4_CH1 DAC1_CH2		PB14, PD14	PA8, PC8	

Each comparator has a non-inverting input and an inverting input.
The INMSEL field in the COMP1_CSR and COMP2_CSR registers is used to select the inverting input.
Note that VREFINT possibly divided can be selected as the INM input of any comparator.
The INPSEL field in the COMP1_CSR and COMP2_CSR registers is used to select the non-inverting input.
Note that the output of any comparator can be connected to timers and EXTI units.

Comparator output blanking function (1/3)

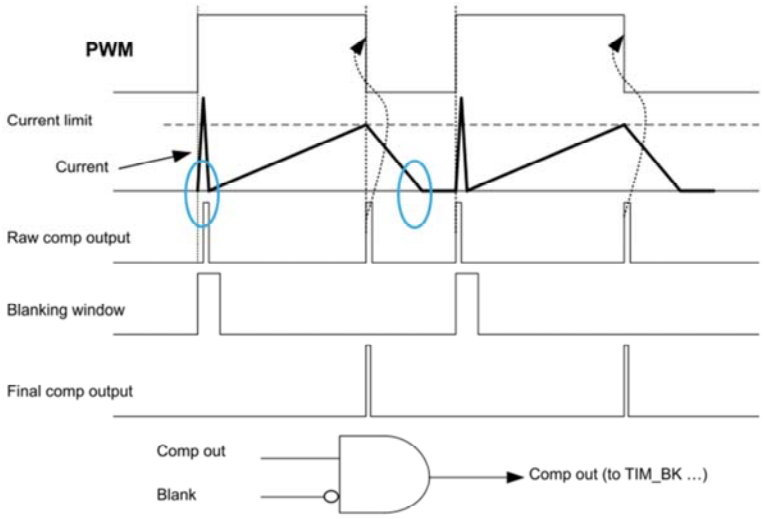
- For comparators, possibility to have blanking to mask spurious over-current during turn-on, or zero-crossing events during turn-off (for Predictive Functional Control)
  - 7 sources from TIM1, TIM2, TIM3, TIM4, TIM8, TIM15 and TIM20



The blanking function aims to mask the output of the comparator during period of times indicated by a timer. This is typically used in the PFC technique (Predictive Functional Control).
The output of the comparator called VALUE is ignored when the timer TIMx_OCy signal is asserted.

Comparator output blanking function (2/3)

- Prevents current regulation tripping due to short-duration current spikes at the beginning of the PWM period
- Masks the COMP output redirected to timer break input



The comparator can be used in the cycle-by-cycle regulation loop for monitoring the peak value of the current flowing into the load.
The purpose of the blanking function is to prevent incorrect current regulation tripping due to short duration current spikes at the beginning of the PWM period.
Short current spikes caused by activating the power switches can produce false pulses on the comparator output – marked by the blue color on the diagram.
These pulses need to be masked by a blanking window to avoid false fault detection.
The blanking window waveform can be generated by one of the timer output channels.

Comparator output blanking function (3/3)

BLANKSEL	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7
0b000	No blanking						
0b001	TIM1_OC5	TIM1_OC5	TIM1_OC5	TIM3_OC4	TIM2_OC3	TIM8_OC5	TIM1_OC5
0b010	TIM2_OC3	TIM2_OC3	TIM3_OC3	TIM8_OC5	TIM8_OC5	TIM2_OC4	TIM8_OC5
0b011	TIM3_OC3	TIM3_OC3	TIM2_OC4	TIM15_OC1	TIM3_OC3	TIM15_OC2	TIM3_OC3
0b100	TIM8_OC5	TIM8_OC5	TIM8_OC5	TIM1_OC5	TIM1_OC5	TIM1_OC5	TIM15_OC2
0b101	TIM20_OC5	TIM20_OC5	TIM20_OC5	TIM20_OC5	TIM20_OC5	TIM20_OC5	TIM20_OC5
0b110	TIM15_OC1	TIM15_OC1	TIM15_OC1	TIM15_OC1	TIM15_OC1	TIM15_OC1	TIM15_OC1
0b111	TIM4_OC3	TIM4_OC3	TIM4_OC3	TIM4_OC3	TIM4_OC3	TIM4_OC3	TIM4_OC3

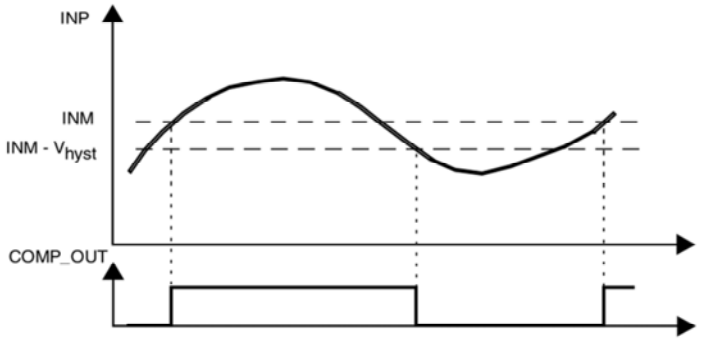
life.augmented

The comparator's output can be masked during a blanking time defined by the timer output compare value selected in the BLANKSEL field.
For each comparator, this table indicates which timer output signal is used to control the blanking.

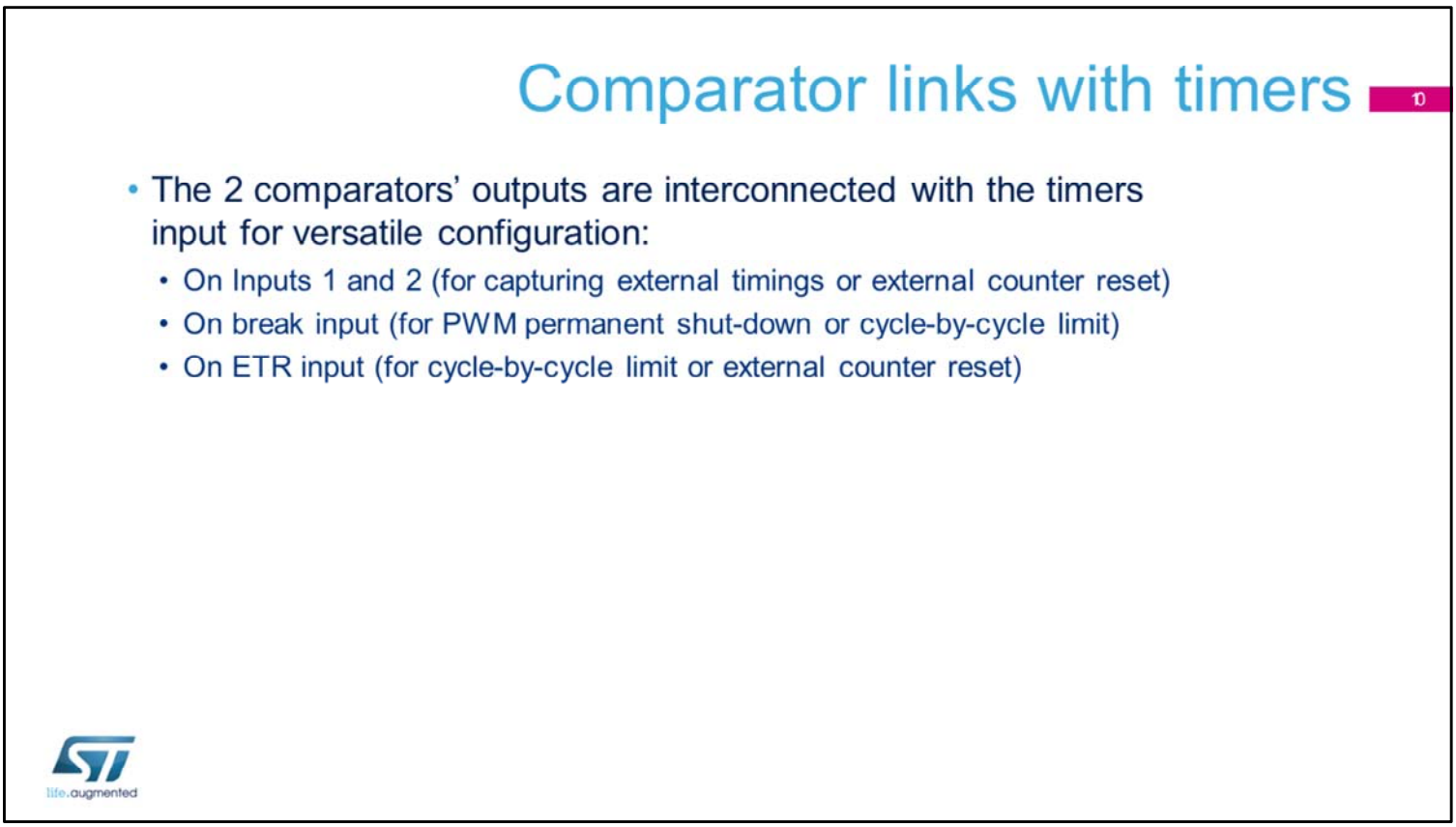
COMP hysteresis

9

- COMP programmable hysteresis:
  - 8 levels of hysteresis:
    - 0 – 70mV with 10mV step
    - Set by HYST[2:0] bits
  - Hysteresis influences output falling edge only:

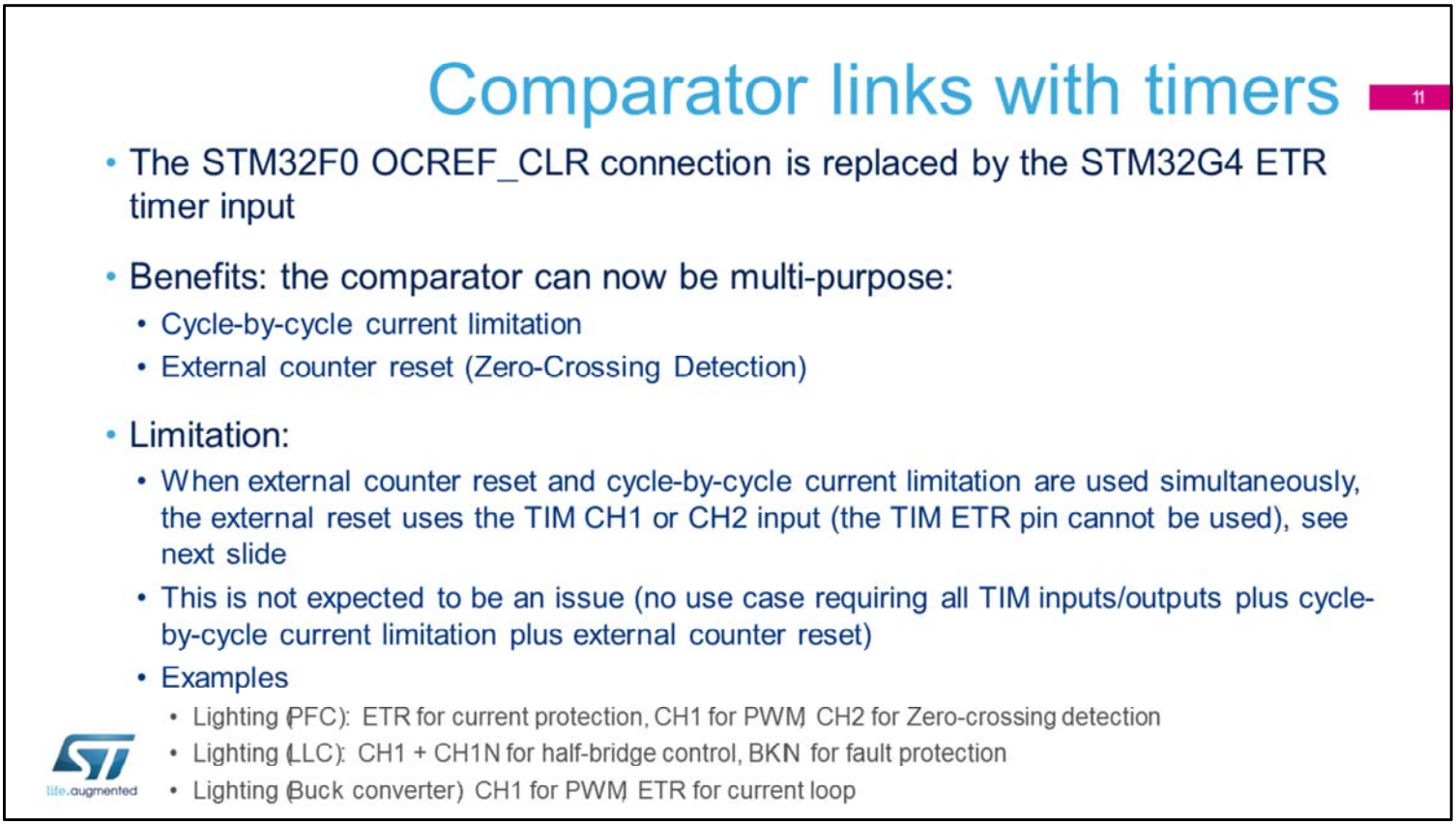


The comparator includes a programmable hysteresis to avoid spurious output transitions with noisy input signals. It is non-symmetrical and only acting to falling edge of the comparator output.
The internal hysteresis function can be disabled so as to set the amount of hysteresis with external components, which can be useful for example when exiting a low-power mode.



The comparators have internal connections with the timer units.
The output can be internally redirected to a wide range of timer inputs for the following purposes:

- Emergency shut-down of PWM signals, using BKIN and BKIN2 inputs
- Cycle-by-cycle current control, using Electronic Timing Relay (ETR) inputs
- Input capture for timing measures.



The connection between the comparators and the timer is generally used for two purposes:

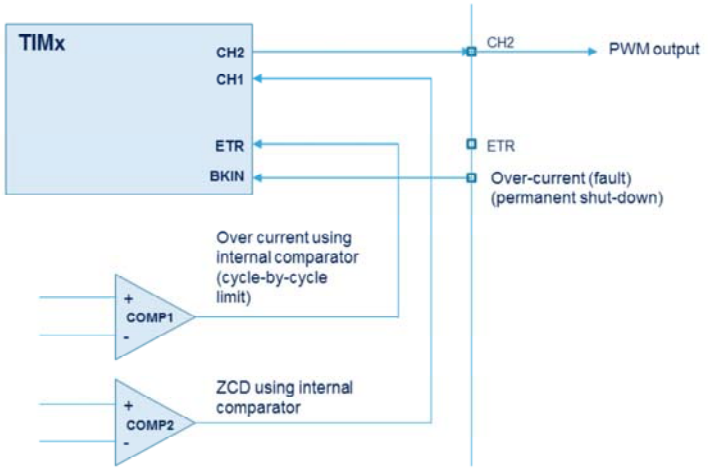
- Cycle-by-cycle current limitation based on the blanking mechanism
- External counter reset when the voltage drops below a threshold: zero-crossing detection.

When both are needed simultaneously, the current limitation is based on the ETR timer input and a counter reset is signaled through a timer channel input.

Comparator links with timers current control

12

- Current control using internal comparator resources



The figure represents an example of direct connection between Timer and COMP units.
Over-current limitation uses the ETR input and external reset uses the CH1 input.

Interrupts

Interrupt event	Description
Comparator output through EXTI	Configurable using rising or falling edges or both

- COMP output can trigger an interrupt through the EXTI line
  - COMP1: EXTI line 21; COMP2: EXTI line 22; COMP3: EXTI line 29,
  - COMP4: EXTI line 30; COMP5: EXTI line 31; COMP6: EXTI line 32;
  - COMP7: EXTI line 33

Interrupt event	Description
Comparator output to NVIC	Need AHB clock to generate the interrupt

- COMP output can trigger an interrupt on NVIC
  - COMP1, COMP2, COMP3: NVIC position 64
  - COMP4, COMP5, COMP6: NVIC position 65
  - COMP7: NVIC position 66

life.augmented

The comparator can trigger an interrupt on the rising, falling or both edges of the comparator output through the EXTI line.
This is required to exit the Stop modes.
The output can also be connected to the CPU's nested vectored interrupt controller (NVIC).

Low-power modes

Mode	Description
Run	Active
Sleep	No effect on the comparators. Comparator interrupts cause the device to exit the Sleep mode
Stop 0	No effect on comparators Comparator interrupts cause the device to exit the Stop mode
Stop 1	
Standby	The COMP registers are powered down and must be reinitialized after exiting standby or shutdown mode
Shutdown	

The on-chip comparator remains active in the following modes: Run, Sleep, and Stop modes.
In Standby and Shutdown modes, it is powered-down and must be reinitialized for use if returning to one of the higher powered modes.
The comparator supports interrupt generation with wake-up from Sleep and Stop modes, through the EXTI unit.

Related peripherals

- Refer to these peripherals trainings linked to this peripheral:
  - IMX- Interconnect matrix
  - TIM- Timers
  - HRTIM – High Resolution Timer
  - EXTI – Extended interrupts and events controller
  - GPIO – General-purpose inputs and outputs
  - DAC – Digital to Analog Converters

life.augmented

This is a list of peripherals related to the COMP unit. Please refer to these peripheral trainings for more information if needed.