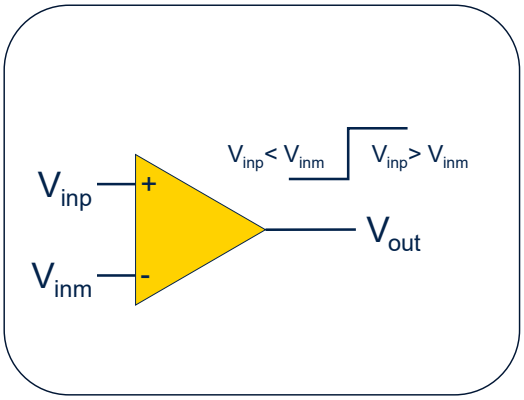
Hello, and welcome to this presentation of the STM32H5 comparator.
It covers the main features of the ultra-low-power comparator and gives some application examples.

Overview



- Compares two analog signals and provides a digital output indicating which is larger
- Capability to wake up the CPU from STOP mode

Application benefits

- One instance of COMP in STM32H503
- Safety features such as the configuration lock or break event generator for timers
- Flexible I/O interconnections
- Hysteresis and speed vs. consumption configuration

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The comparator inside STM32H503 microcontrollers provides a binary output, which indicates if the analog voltage on the plus input is larger than the voltage on the negative input. It allows the microcontroller to react when the analog signal crosses a predefined threshold.
The comparator continuously monitors voltage in contrast to an analog-to-digital converter which operates in sampled mode.
The comparator can be used to wake up devices from Sleep and Stop modes.
Note this is not possible when the internal reference voltage is switched off.
Applications can benefit from the flexible configuration of comparator properties, which can be locked for safety reasons.
Another safety feature of comparator is its ability to generate a break signal for timers allowing to safely stop the generation of PWM driving signals.

Key features

- One ultra-low-power comparator COMP1
- Programmable hysteresis and speed vs. consumption
- Configurable plus and negative inputs
  - Multiplexed I/O pins, DAC channels 1 outputs, internal reference voltage and its three submultiple values
- Output redirection
  - Configurable I/Os
  - Timer – break event for fast PWM shutdown, cycle-by-cycle current control, and input capture for timing measurements
  - Output blanking source

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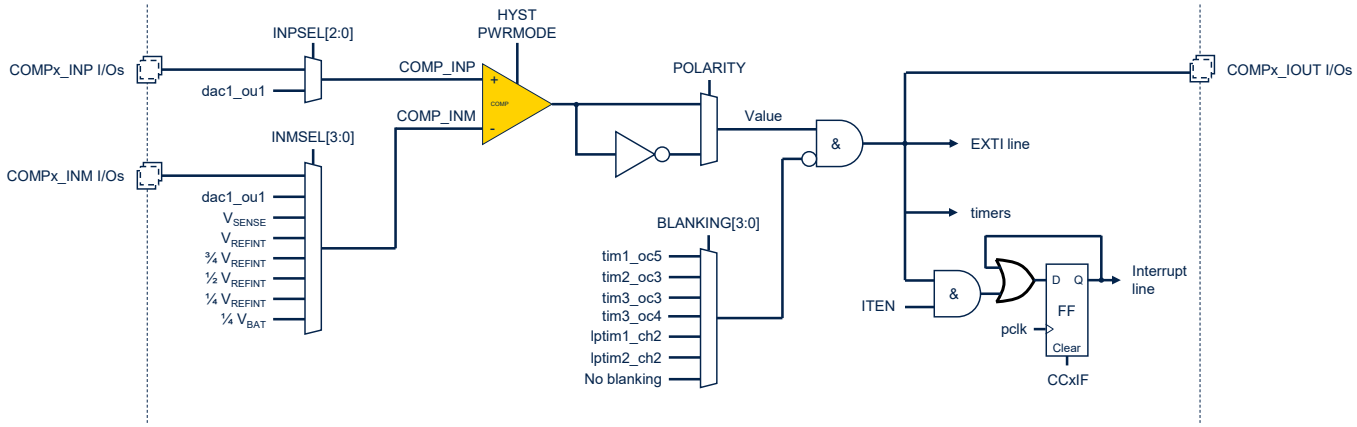
The analog properties of the comparator include hysteresis or a trade-off between speed and power consumption are configurable.
It offers flexible inter-connections of inputs and outputs allowing a threshold selection of several external and internal inputs such as DAC outputs or internal reference voltage outputs.
The comparator output can be connected to I/Os using the alternate function channels or internally redirected to a variety of timer inputs such as enabling the break event for fast PWM shutdown. The user can create cycle-by-cycle current control or input captures for timing measurements.

Block diagram



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This slide shows the general block diagram of the comparator integrated in the device.
Positive and negative inputs of the comparators are selectable through multiplexers.
The output of the comparator can be inverted, before being anded together with the input selected for blanking.
The resulting signal can be steered to general purpose input/output pads, EXTI module, timers and maskable interrupt line.

COMP low-power features

- COMP1 power consumption versus propagation delay can be adjusted for the optimum trade-off for a given application
- There are three power modes available
  - HIGH SPEED and full power
  - MEDIUM SPEED and medium power
  - LOW SPEED and ultra-low power

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The comparator power consumption can be adjusted to have the optimum trade-off between the speed and energy efficiency for a given application.
There are three modes available: high speed, medium speed and ultra-low-power.
The high-speed mode is preferred for power conversion applications - for example, a motor control design, while ultra-low power mode is the right choice for battery-powered applications where reaction times are not critical - for example in PIR sensor monitoring.
The comparator can stay active even if the rest of the system is suspended and the clock is switched off.

Interrupts

Interrupt event	Description
Comparator output through EXTI	Configurable using rising or falling edges or both

- COMP1 output can trigger an interrupt through the EXTI line
  - COMP1 → EXTI line 29

Interrupt event	Description
Comparator output to NVIC	Need AHB clock to generate the interrupt

- COMP1 output can trigger an interrupt on NVIC
  - COMP1 → NVIC position 133

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The comparator can trigger an interrupt on the rising, falling or both edges of the comparator output through the EXTI line, which can be used as a wakeup event to exit sleep and stop modes.
The output can also be directly connected to the CPU's Nested Vectored Interrupt Controller (NVIC).

Low-power modes

Mode	Description
Run	Active
Sleep	Active
Stop	Active
Standby	Powered-down ➢ The peripheral must be reinitialized after exiting Standby mode

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The on-chip comparator remains active in the following modes: Run, Sleep, and Stop modes.
In Standby mode, it is powered-down and must be reinitialized for use if returning to one of the higher-powered modes.

Performance & power consumption

- Comparator propagation delay

Conditions	Typical delay (µs)	Maximum delay (µs)
Ultra-low-power mode	2.5	7
Medium mode	0.5	0.9
High-speed mode	0.05	0.08

(1) Propagation delay for step > 200 mV with 100 mV overdrive on positive inputs

- Comparator consumption

Conditions	Static Typ. (µA)	Active (1) Typ. (µA)
Ultra-low-power mode	0.4	0.8
Medium mode	5	6
High-speed mode	70	75

(1) Toggling with frequency of 50 kHz, ±100 mV overdrive square signal

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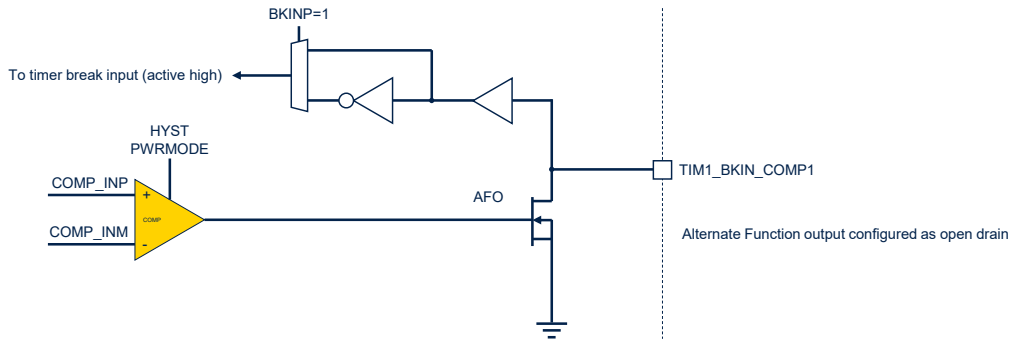
The on-chip comparator configuration capability allows the user to select the best performance point for the targeted application.
It replaces the external stand-alone comparator, thereby reducing the bill of materials.

COMP break signal generation

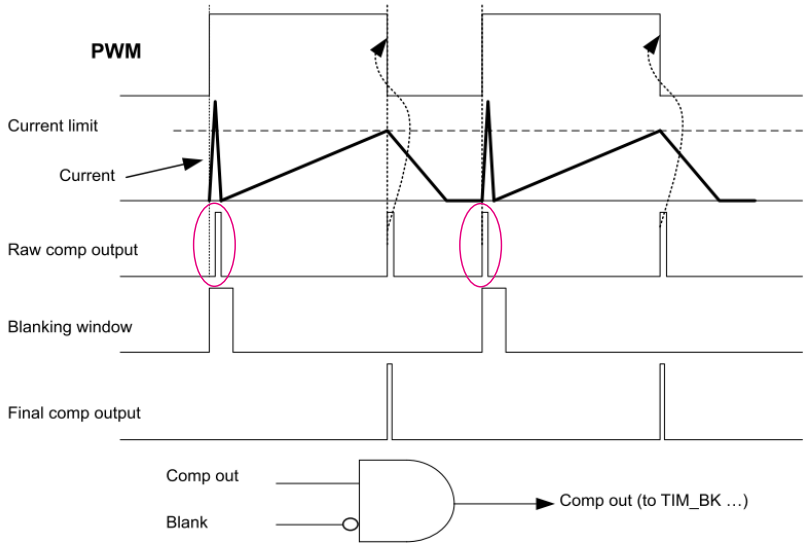
- Comparator COMP1 output value can generate break input signals for timers (TIM1) on input pins TIM1_BKIN or TIM1_BKIN2 by configuring the GPIO alternate function



Comparator output values can generate break input signals for the timers on input pins using GPIO alternate function selections incorporating the I/O open drain connection.
The purpose of the break function is to protect power switches driven by PWM signals generated by timers.
The two break inputs are usually connected to fault outputs of power stages and 3-phase inverters.
When activated, the break circuitry shuts down the PWM outputs and forces them to a predefined safe state.
Please see the timer training slides for more details.

COMP blanking

- Prevents current regulation tripping due to short-duration current spikes at the beginning of the PWM period
- Masks the COMP output redirected to timer break input



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The comparator can be used in the cycle-by-cycle regulation loop for monitoring the peak value of the current flowing into the load.
The purpose of the blanking function is to prevent incorrect current regulation tripping due to short duration current spikes at the beginning of the PWM period.
Short current spikes caused by activating the power switches can produce false pulses on the comparator output – marked by the blue color on the diagram.
These pulses need to be masked by a blanking window to avoid false fault detection.
The blanking window waveform can be generated by one of the timer output channels.

STM32H5 COMP IO assignment

External IO assignment	COMP1
Input inverting IO assignment COMP1_INMx	COMP1_INM1 = PC4 COMP1_INM2 = PB1 COMP1_INM3 = PA5
Input non-inverting IO assignment COMP1_INPx	COMP1_INP1 = PA0 COMP1_INP2 = PB0 COMP1_INP3 = PB2
Output IO assignment COMP1_OUT	PA13, PB1, PB15, PC5

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This table is showing comparator flexible IO assignment, for more information, please refer to product datasheet.

Related peripherals

- Refer to these peripheral trainings linked to this peripheral
  - Reset and clock control Reset and clock control (COMP clock control, COMP enable/reset)
  - Interrupts (COMP interrupt mapping)
  - Timers (COMP output redirection, break function)
  - General-purpose inputs/outputs General-purpose inputs/outputs (COMP input/output pins)
  - Digital-to-analog converter

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This is a list of peripherals related to the comparators.
Please refer to these peripheral trainings for more information if needed.

Thank you

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Thank you for attending this presentation.