Hello, and welcome to this presentation of the STM32MP13x power controller. The STM32MP13x's power management functions and all power modes will also be covered in this presentation.

Overview

- Provides power management and supply control functions
  - Different supply configurations
  - Voltage scaling
  - Wakeup from low-power modes
- 5 low-power modes with fast wakeup
- VBAT backup mode with RTC and backup registers
- Independent power supplies
- Trust zone security

Application benefits

- Optimizing power consumption:
  - Dynamic voltage scaling
  - Low power mode control per CPU
- Trust zone security on some system resources

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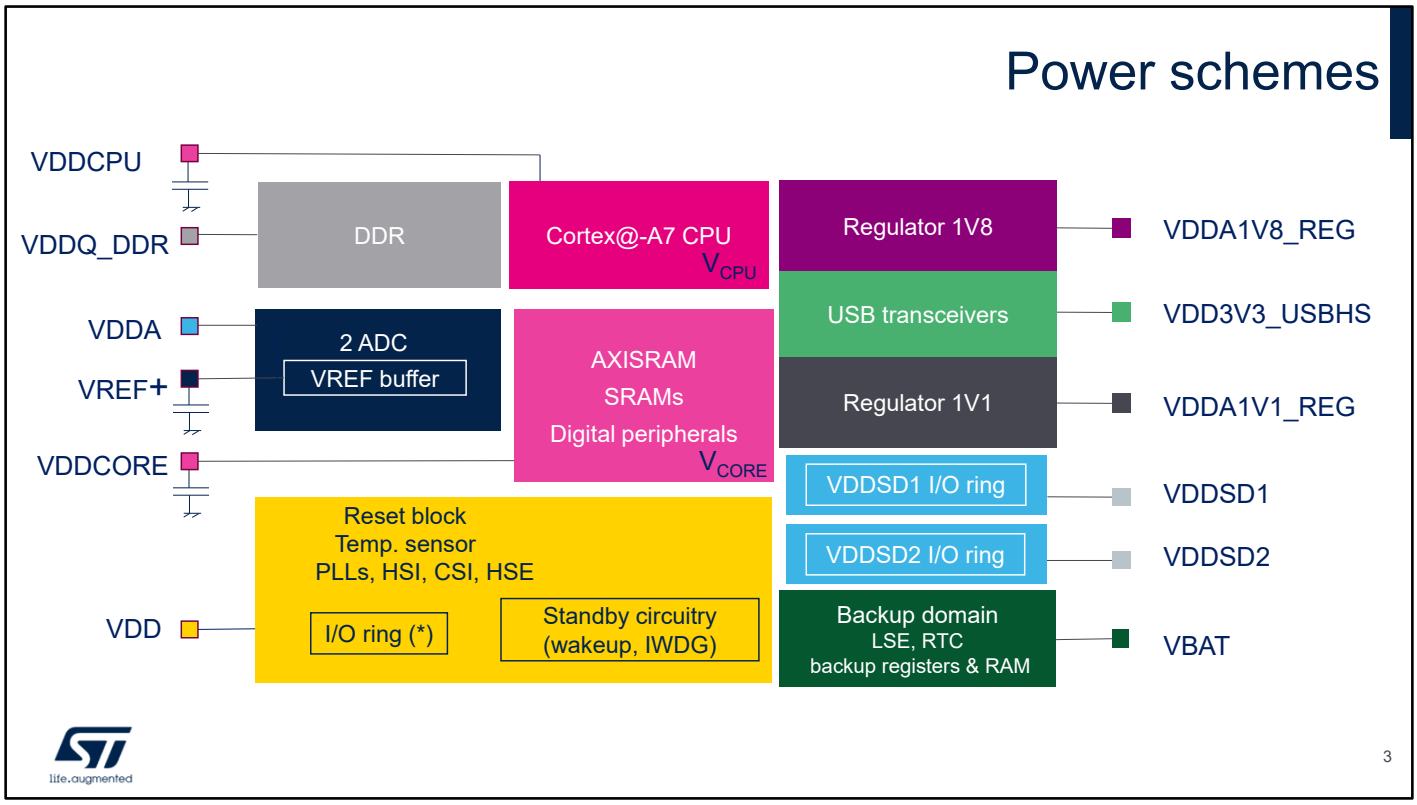
2

The STM32MP1 microcontroller has several key features related to power management, including several low-power modes, where it is still possible to wake up the CPUs individually with an event on an I/O, as well as a large number of peripherals that can wake up from the various low-power modes.
Several power supplies are independent, allowing reduction of the device power consumption while some peripherals are supplied at other voltages.
Thanks to the large number of power modes and independent power domains, STM32MP1 devices offer high flexibility to minimize power consumption and adjust it depending on active peripherals, required performance and necessary wake-up sources.
Some system resources can be secured.



STM32MP13x devices have several independent power supplies, which can be set at different voltages or tied together.
The main power supply is VDD. It supplies most of the I/Os. VDD also supplies the reset block, temperature sensor and all internal clock sources.
In addition, it supplies the Standby circuitry, which includes the wakeup logic and independent watchdog.
VDDSD1 and VDDSD2 supply two independent sets of I/Os which can be used to have a voltage supply level different from that of VDD, especially for the SDMMC1 and SDMMC2 interfaces when used in UHS-I mode.
The VDDCORE directly provides the VCORE supply. VCORE supplies most of the digital peripherals and the AXI RAMs and SRAMs.
The VDDCPU directly provides the VCPU supply. VCPU supplies the Cortex-A7 MPU. The DDR interface has its dedicated VDDQ_DDR supply.

The STM32MP13x features several independent supplies for peripherals: VDDA for the analog peripherals, VDD3V3_USBHS for the USB transceivers.
The VREF+ pin provides the reference voltage to the analog-to-digital and digital-to-analog converters and can be used as an external buffer reference for the application.
A backup battery can be connected to the VBAT pin to supply the backup domain.

Furthermore, the STM32MP13x microcontroller incorporates various regulators which provide the various voltage levels for the USB.

Power schemes

Optimized power and performance thanks to independent power supplies

- V_{DD} from 1.71 to 3.6 V
- V_{DDSD1} and V_{DDSD2} from 1.71 to 3.6 V
- V_{BAT} from 1.2 to 3.6V including the RTC, backup RAM
- V_{DDCORE} from 1.15 V to 1.29 V (min. 1.21 V in Run mode, 0.85 V in LPLV-Stop/LPLV-Stop2)
- V_{DDCPU} from 1.21 V to 1.38 V (min. 0.85 V in LPLV-Stop, min. 1.33 V when F_{MPU} > 650 MHz)
- V_{DDA} from 1.62 to 3.6 V
  - 1.62 V min. when ADCs are used
  - 1.95 V min. when V_{REFBUF} is used
- V_{DD3V3_USBHS} from 3 to 3.6 V for USB High Speed
- V_{DDQ_DDR} from 1.14 V to 1.575 V depending on DDR memory type.

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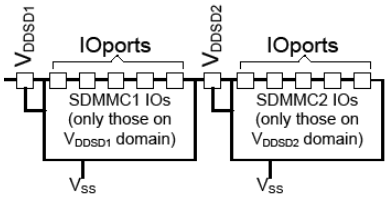
The main power supply VDD ensures full-featured operation in all power modes from 1.71 up to 3.6 V, allowing supply by an external 1.8 V regulator. Other independent supplies are provided for peripherals operating at a different voltage. VDDSD1 and VDDSD2 independent supplies for some I/Os have the same supply range as VDD.
A backup domain is supplied by VBAT, which must be greater than 1.2 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator, the backup registers, and the backup RAM.
The digital core logic (Cortex-A7) is supplied directly from VDDCPU at typical 1.25V in Run mode up to 650MHz, typical 1.35V in Run mode up to 900MHz, and typical 0.9 V in LPLV-Stop mode.
The analog power supply VDDA can be connected to any voltage other than VDD. When an analog-to-digital converter is used, the VDDA voltage must be greater than 1.62 V. When Vrefbuff is used, VDDA must be greater than 1.95 V.
The USB interface has its individual supply VDD3V3_USBHS.
The DDR interface is supplied from the individual VDDQ_DDR.

Power schemes

SDMMC, no need for external level shifters

- SDMMC UHS-I mode requires to dynamically switch the power supply level of the signals.

→ On STM32MP13x, V_{DDSD1} and V_{DDSD2} independent power supplies can be dynamically changed by external power regulator removing the need for external level shifters.



D[3:0], CMD, CK

D0DIR, D123DIR, CKIN, CDIR
D[7:4] (for eMMC)

eMMC 1.8V is not covered by those dedicated power supplies !! Only 4bit SDMMC is covered

Care must be taken to not enable HSLV option on the GPIOs when VDDSD1/2 are above 2.7V (chip can be damaged) SYSCFG_HSLVENxR registers shall be used (cf Ref manual)

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5

The VDDSD1 and VDDSD2 independent supplies can be used to eliminate the need for external level shifters when an SDMMC1 or SDMMC2 interface is used in UHS-I mode.
In UHS-I mode, the interface signals have to be dynamically changed from a 3.3V to a 1.8V supply.
VDDSD1 or VDDSD2 can be dynamically changed by software by programming the external regulator.
Care must be taken to enable the HSLV option only once the supply level has been set below 2.7V or else the chip can be damaged.
The eMMC at 1.8V is not covered by these independent supplies since some eMMC signals are not part of the GPIO's supplied by VDDSD1 or VDDSD2.
eMMC 1.8V will require the VDD and VDDSD1 or VDDSD2 to be at 1.8V.

Power schemes

Independent voltage reference supplies for analog performance

- V_{REF+} : reference voltage for ADCs
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.

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6

The ADC voltage reference can be provided either by an external supply voltage or by the internal reference buffer. This allows converter performance to be improved by providing an isolated and independent reference voltage.

Backup domain regulators

- Used to regulate the V_{SW} supply to the Backup RAM supply level.
- The Backup RAM has its own regulator.
  - When V_{DDCORE} is present
    - Backup domain regulators are off. (Allows to reduce backup battery consumption)
    - Backup RAM is supplied from V_{DDCORE}.
  - When V_{DDCORE} is absent (Standby or V_{BAT} mode) and backup regulators are enabled
    - Backup domain regulator are on.
    - Backup RAM is supplied from V_{BKUP}.
  - When V_{DDCORE} is absent (Standby or V_{BAT} mode) and backup regulator are disabled
    - Backup domain regulators are off.
    - Backup RAM is powered down. (data lost)

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The Backup regulator is used to keep the context of the Backup RAM in Standby and VBAT modes. The backup RAM regulator is enabled by the BREN bit in the PWR register CR2.
When the regulator is enabled, its supply level is checked to ensure that it is ready, before the system enters Standby mode.

Other regulators

- USB regulators
  - Used to supply the USB interfaces. Can’t supply external logic.
  - See USB training

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8

Independent USB regulators generate the V_{DDA1V8_REG} and V_{DDA1V1_REG} supplies from VDD.

Voltage supply supervision

Supply supervision enabling dynamic power management

- Supply voltage monitoring is provided on:
  - V_{DD} via POR/PDR, BOR (reset), and PVD (threshold interrupt on EXTI).
  - $V_{DDSD1,}$ V_{DDSD2} via level detector (ready register bit VDDSD1RDY, VDDSD2RDY)
  - V_{DDA} via AVD (threshold interrupt on EXTI)
  - V_{BAT} via V_{BAT} threshold (interrupt via Tamper)
  - V_{DDCORE} Core domain supply, via level detector (reset).
  - V_{DDCPU} CPU domain supply, via level detector (reset).
  - V_{SW} Backup domain supply, via level detector (reset).
  - V_{BKP} Backup domain backup RAM supply, via level detector (ready register bit BRRDY)
  - V_{DD3V3_USB} 3.3V USB I/O regulated supply, via level detector (ready register bit USB33RDY)
  - V_{DDA1V8_REG} 1.8V USB regulated supply, via level detector (ready register bit REG18RDY)
  - V_{DDA1V1_REG} 1.1V USB regulated supply, via level detector (ready register bit REG11RDY)

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9

The power supply supervisor ensures dynamic power supply management. STM32MP13x devices embed power management on the main VDD, VDDSD1, VDDSD2, analog VDDA, VBAT supply input, VDDCORE domain, VDDCPU domain, Backup VSW domain, Backup regulator VBKP, USB interface VDD3V3_USB supply, and regulator supplies VDDA1V8_REG, VDDA1V1_REG.
The main VDD supervisor handles reset management and voltage detection via the programmable voltage detector (PVD) when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby modes. 7 thresholds can be selected by software. In addition, comparisons can be made with an external pin.
The VDDSD1 and VDDSD2 supply supervisors verify that the VDDSD1 or VDDSD2 interface supply is present. VDDSD1 and VDDSD21 supervision can be enabled in all modes except Standby modes.
The analog VDDA supervisor handles voltage detection via the analog voltage detector (AVD) when VDDA crosses the selected threshold. The AVD can be enabled in all modes except Standby mode. 4 thresholds can be selected by software.
The VBAT supply voltage is monitored to detect when VBAT crosses the minimum and maximum thresholds. The VBAT voltage detection function can be enabled in all modes.
The VDDCORE and VDDCPU supervisors handle reset management detection. They keep the VDDCORE or VDDCPU domain in reset as long as the supply level is not OK.
The Backup domain VSW supervisor handles reset management when the

supply drops below the operating level.
The Backup RAM regulator VBKP supply supervisor verifies that the regulator is ready to supply the backup RAM, before entering Standby mode.
The USB interface VDD33USB supply supervisor verifies that the USB interface supply is present. USB supervision can be enabled in all modes except Standby modes.
The USB regulators VDDA1V8_REG and VDD1V1_REG supply supervisors verify that the regulator is ready to supply the interface.

POR/PDR & BOR

Safe and ultra-low-power reset management

- POR (Power On Reset)
  - Supervises V_{DD}.
  - Fixed level to disable reset when V_{DD} level rises above threshold.
- PDR
  - Supervises V_{DD}.
  - Fixed level to generate reset when V_{DD} level drops below threshold.
  - Can be enabled/disabled with PDR_ON input pin.
- BOR
  - Supervises V_{DD}.
  - Provides 4 selectable levels from V_{BOR0} = 1.63 V to V_{BOR3} = 2.6 V through option bits **BOR_LEV[2:0]**, generates reset when V_{DD} level drops below threshold.
  - Can be disabled with system option bits.

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10

The V_{DD} power supply supervisor guarantees safe and ultra-low power reset management.
STM32MP1 devices embed an ultra-low-power brown-out reset (BOR) which is always enabled in all power modes. The BOR ensures reset generation as soon as the MCU drops below the selected threshold, regardless of the V_{DD} slope.
Four thresholds from typical 1.63 V to 2.6 V are selected by option byte programmed in Flash memory.

Temperature supervision

- Temperature threshold
  - Supervises junction temperature.
  - Can be enabled/disabled with register bit MONEN.
  - Provides TEMPH and TEMPL register flags, connected to Tamper wakeup interrupt.

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The temperature supervisor detects when the junction temperature crosses the minimum and maximum thresholds. The temperature detection function can be enabled in all modes.

VBAT supervision

- Backup battery threshold
  - Supervises backup battery supply level.
  - Can be enabled/disabled with register bit MONEN.
  - Provides VBATH and VBATL register flags, connected to Tamper wakeup interrupt.

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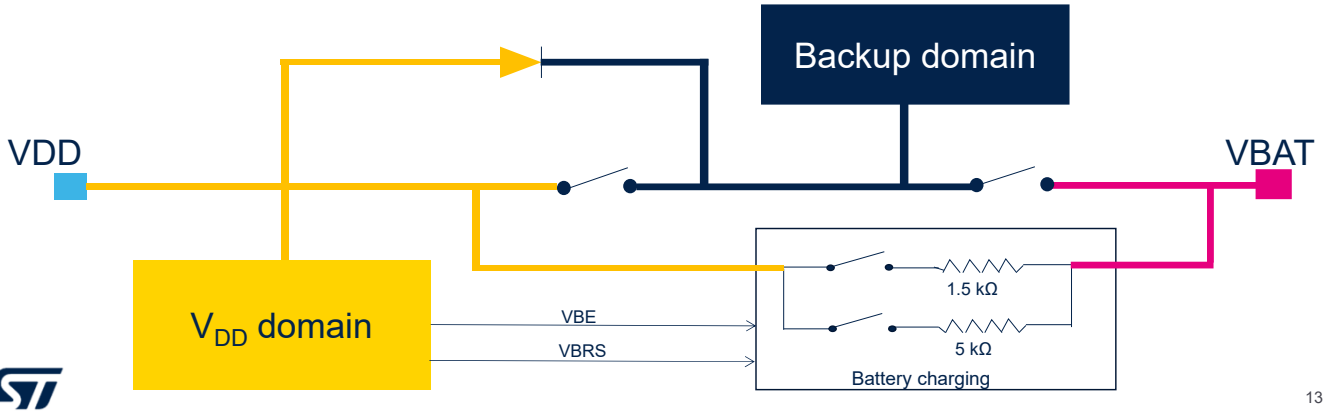
The backup battery supervisor detects when the backup battery supply level crosses the minimum and maximum thresholds. The backup battery detection function can be enabled in all modes.

V_{BAT} battery charging

- A backup battery connected to V_{BAT} can be charged from V_{DD}.
  - Enabled by application Software
  - Selection between 2 charging resistor values (5 kOhm or 1.5 kOhm)
  - Automatically disabled when entering V_{BAT} mode.



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13

The battery charging feature can charge a super-cap connected to the VBAT pin through an internal resistor when the V_{DD} supply is present. Charging is enabled by software and is done either through a 5kOhm or 1.5 kOhm resistor depending on software. Battery charging is automatically disabled in VBAT mode.

TrustZone security

- TrustZone security in the Power controller allows to secure some system functions:
  - VBAT, Temperature, PVD and AVD monitoring.
  - Backup domain protection, and backup RAM settings.
  - USB regulators control
  - DDR self-refresh and retention control.
  - Battery charging settings
  - MPU system low-power mode configuration
  - LP-Stop modes configuration
  - Wakeup pin configuration

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14

The following features can be made TrustZone-secure. They are either all secure or all non-secure.

- Backup battery voltage monitoring, temperature monitoring, Programmable voltage detector, analog peripheral voltage detector.
- Backup domain protection, and backup RAM settings.
- USB regulators control
- DDR self-refresh and retention settings
- Backup battery charging settings
- MPU system low-power mode configuration
- LP-Stop, LPLV-Stop and LPLV-Stop2 mode configuration
- Individual per wakeup pin configuration

CPU (Cortex-A7) operating modes

CPU operating modes controlled from WFI/WFE and ctrl bits

Mode	Description	control
CRun	CPU, CPU-sub system bus matrix(s), CPU enabled peripheral clock(s) active.	
CSleep	CPU clock stopped, CPU-sub system bus matrix(s), CPU sleep enabled peripheral clock(s) active.	WFE or WFI, STPREQ_P0=0 MPU GIC interrupts and events cleared
CStop	CPU, CPU-sub system bus matrix(s), CPU peripheral clock(s) stopped.	WFI, STPREQ_P0=1, PDDS=0, STOP2=0 MPU GIC interrupts and events cleared all wakeup sources are cleared
CStandby	CPU subsystem power supply (VDDCPU) is OFF.	WFI, STPREQ_P0=1, PDDS=0, STOP2=1 (System LPLV-Stop2) or PDDS=1, STOP2=x (System Standby) MPU GIC interrupts and events cleared all wakeup sources are cleared

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The CPU entering low-power mode is controlled by the WFI and WFE instruction and some control bits.

System operating modes

- System operating modes controlled from wakeup sources, CPU state, ctrl bits

Mode	Description	control
Run	System clock is active and forwarded to the system.	CPU in CRun or CSleep or wakeup source active
Stop	System clock is stopped.	CPU in CStop, all wakeup sources are cleared (STPREQ_P0=1, STOP2=0, PDDS=0, LPDS=0)
LP-Stop	System clock is stopped, Low-power mode signaled to external regulator	CPU in CStop, all wakeup sources are cleared (STOP2=0, PDDS=0, LPDS=1, LVDS=0)
LPLV-Stop	System clock is stopped, Low-power mode signaled to external regulator VDDCORE and VDDCPU can be lowered (0.85 V)	CPU in CStop, all wakeup sources are cleared (STOP2=0, PDDS=0, LPDS=1, LVDS=1)
LPLV-Stop2	System clock is stopped, Low-power mode signaled to external regulator VDDCORE can be lowered (0.85 V), VDDCPU OFF	CPU in CStandby, all wakeup sources are cleared (STOP2=1, PDDS=0, LPDS=1, LVDS=x)
Standby	System is powered down. VDD ON (Backup domain may be kept active)	CPU in CStandby, all wakeup sources are cleared (STOP2=x, PDDS=1, LPDS=x, LVDS=x)
VBAT	System is powered down. VDD OFF, Backup domain kept active if supplied by VBAT pin	

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The STM32MP13x system operating mode is controlled from the CPU state, wakeup sources state and some control bits.

CPU CSleep mode

All peripherals available and fastest wakeup time

- CPU is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing **WFI** (Wait For Interrupt) or **WFE** (Wait For Event)

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CPU CSleep mode enables all peripherals to be used and features the fastest wakeup time.
In this mode, the CPU is stopped, and each peripheral clock can be configured by software to be gated ON or OFF during CPU CSleep mode.
This mode is entered by executing the assembler instruction Wait for Interrupt or Wait for Event.

Stop, LP-Stop, LPLV-Stop modes

Lowest power modes with full retention

- All memory and all peripheral register data is retained
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock to the MPU is restored at wakeup.

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STM32MP13x devices feature three Stop modes: Stop, LP-Stop and LPLV-Stop, which are the lowest power modes with full retention and fast wakeup time to Run mode.
The contents of SRAMs and all peripheral registers are preserved in all Stop modes.
All high-speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop modes.
The MPU system clock on wake-up is restored.

LPLV-Stop2 modes

Lowest power modes

- MPU sub-system power supply (VDDCPU) is OFF
- LPLV-Stop2 mode has the lowest Stop mode power consumption (no leakage on MPU sub-system). But it has the longest wakeup time.
- Same peripherals as LPLV-Stop can be active and wake up from LPLV-Stop2
- All memory and all peripheral register data is retained except on VDDCPU domain.
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- System clock to the MPU is restored at wakeup.

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STM32MP13x devices feature a very low power LPLV-Stop2 mode, which has the lowest Stop mode power consumption since it powers off the MPU sub-system.
LPLV-Stop2 however has the longest wakeup time to Run mode, and MPU sub-system memory content is lost.
The same peripherals as on LPLV-Stop mode can be active and wake up from LPLV-Stop2 mode.
All high-speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
The MPU system clock on wake-up is restored.

Stop modes comparison

	Stop	LP-Stop	LPLV-Stop	LPLV-Stop2
Consumption	high	medium	low	lowest
Wakeup time	short	medium	long	longest
Regulator	Main mode	Low Power mode		
	Normal supply level		Low-voltage level	VDDCORE: Low-voltage level VDDCPU: OFF
Wakeup sources	DBG, USBH, OTG, CEC, ETH			
	USARTx, I2Cx, SPIx, DTS, LPTIMx, GPIOs, PVD, AVD, BOR, VBATH/VBATL, TEMPH/TEMPL, LSE CSS, RTC/auto wakeup, tamper pins, IWDGx			

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20

When comparing Stop modes:
The lower the low power mode consumption, the longer the wakeup time.
Stop and LP-Stop modes keep the V_{CORE} domain at the same supply level as Run mode, allowing a very short wake-up time at the expense of higher consumption..
LP-Stop mode allows control of the external power supply unit to be placed in low-power mode, reducing overall system power consumption as compared to that in Stop mode.
LPLV-Stop mode allows the external power supply unit to be placed in low-power mode and supplies a lower Vddcore level, reducing STM32MP1 and overall system power consumption.
LPLV-Stop2 sets the VDDCPU in power-off mode, further decreasing consumption.
Stop and LP-Stop modes support the same number of active wake-up peripherals, whereas LPLV-Stop and LPLV-Stop2 modes support a reduced sub-set.

Standby mode

Lowest power mode with Backup RAM retention, switch to V_{BAT} and I/O control

- By default: no RAM nor registers retention (voltage regulators in power down). backup registers always retained.
- Possibility to retain 8 Kbytes of Backup RAM
- Ultra Low Power BOR always ON: safe reset regardless of V_{DD} slope.
- 6 wakeup pins: the polarity of each of the 6 wakeup pins is configurable
- MPU clock restored on wakeup.

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Standby mode is the lowest power mode in which 8 Kbytes of Backup RAM can be retained, and the automatic switch from VDD to VBAT is supported.
By default, the voltage regulators are in Power-down mode and the SRAMs and peripheral registers are lost. The backup registers are always retained.
Thanks to software, it is possible to retain the Backup RAM.
The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.
6 wakeup pins are available to wake up the device from Standby mode. The polarity of each of them is configurable.
The MPU system clock is restored upon wakeup.

VBAT mode

RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including **12 tamper pins** (5 OUT, 7 IN)
  - **Backup registers**
  - RCC_BDCR register
  - 8 Kbyte Backup memory, when backup regulator is enabled.
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered on.
- Internal connection to ADC for voltage monitoring ($V_{BAT}/4$)
- V_{BAT} charging

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The backup domain allows us to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. 12 tamper pins (5 tamper_OUT, 7 tamper_IN) are functional in VBAT mode and, in case of intrusion detection, will erase the backup registers also included in the VBAT domain.
The backup domain also contains the RTC clock control logic.
Should VDD drop below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery level.
When VDD is present, the battery connected to VBAT can be charged from the VDD supply.

CPU wakes up from CStop mode

- To know from which system low-power mode the CPU wakes up, flags are provided.
  - STOPF - System has been in Stop, LP-Stop, LPLV-Stop or LPLV-Stop2 mode
    - Wakeup interrupt to the CPU will be pending in EXTI or peripheral.
  - SBF – System has been in Standby mode
    - CPU starts from reset, there is no wakeup interrupt pending in the EXTI.
  - SBFMPU- MPU exit CStandby mode (System has been in Standby or LPLV-Stop2 mode)
    - CPU starts from reset, there is no wakeup interrupt pending in the EXTI.
- The CPU flags are supposed to be cleared by firmware when the CPU wakes up.

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When the CPU wakes up from its low-power mode, it needs to know from which mode the system has woken up. Dedicated flag bits STOPF, SBF and SBFMPU are provided for this purpose. These bits inform the CPU about the state of the system, and which parts may need to be reinitialized.

Wakeup

- The CPU wakeup state depends on the system state

System Mode	CPU mode	SBF	SBFMPU	STOPF	Comment	MPU wakeup
Run	**CRun / CSleep**	**0**	**0**	**0**	System contents retained	ISR/Event
Stop, LP-Stop, LPLV-Stop	**CStop**	**0**	**0**	**1**	System contents retained, system clock stopped	ISR/Event
LPLV-Stop2	**CStandby**	**0**	**1**	**1**	MPU sub-system content lost	Reset
Standby	**CStandby**	**1**	**1**	**0**	System contents lost	Reset
VBAT	**n.a.**	**0**	**0**	**0**		

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24

This table gives an overview of the CPU wake-up state versus the System operating mode and how they are signaled by the wake-up flag bits. It also shows how the CPU was awakened, through an interrupt or an event, or a CPU reset.

PWR interrupts

Interrupt event	Description	Availability
WKUP[6:1]	Wakeup from Standby mode. Wakeup from Stop mode via event signal to EXTI	Run, Stop and Standby
PVDO	Wakeup from Stop mode via event signal to EXTI	Run and Stop
AVDO	Wakeup from Stop mode via event signal to EXTI	Run and Stop
VBATH, VBATL	Wakeup from Standby mode & STOP mode via RTC Tamper Interrupt	Run, Stop and Standby
TEMPH, TEMPL	Wakeup from Standby mode & STOP mode via RTC Tamper Interrupt	Run, Stop and Standby

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Here is a summary of the PWR control-related interrupts.

Debug information

- The DBGMCU_CR register enables debugging in Stop and Standby mode:
  - DBGSTOP: when set, the processor clock and associated bus matrix clocks are kept active in Stop mode.
  - DBGSTANDBY: When set, the digital part is not powered down in LPLV-Stop2 and Standby mode, and the processor clock and associated bus matrix clocks are kept active.
    When exiting from LPLV-Stop2 or Standby mode, a reset is generated.
- When DBGSTOP or DBGSTANDBY is enabled, the connection with the debugger is kept during the related Stop or Standby mode.
  After wakeup, debugging is still possible.

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The Debug Control Register is used to enable debugging in Stop and Standby modes. When the related bit is set, the CPU clock and bus matrix clock are kept active, and the regulator is kept ON in normal mode to supply the core logic. This maintains the connection with the debugger during low-power modes, and keeps debugging alive during and after wake-up. Remember to clear these bits when the device is not under debug, since consumption is higher in all low-power modes when these bits are set, due to the fact that they force the regulator to remain enabled and keep clocks active.

Related peripherals

- Refer to the following list of peripheral trainings for more details about their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Interrupts (NVIC and EXTI)
  - Low-power timer (LPTIM)
  - Independent watchdog (IWDG)
  - Real-time clock (RTC)
  - Inter-integrated circuit (I2C) interface
  - Universal synchronous asynchronous receiver transmitter (USART)
  - Low-power universal asynchronous receiver transmitter (LPUART)
  - USB-HS interface

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In addition to this training, you can refer to the Reset and Clock Control and Interrupts trainings as well as those for all the peripherals with wake-up from Stop and Standby capability.

Thank you

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