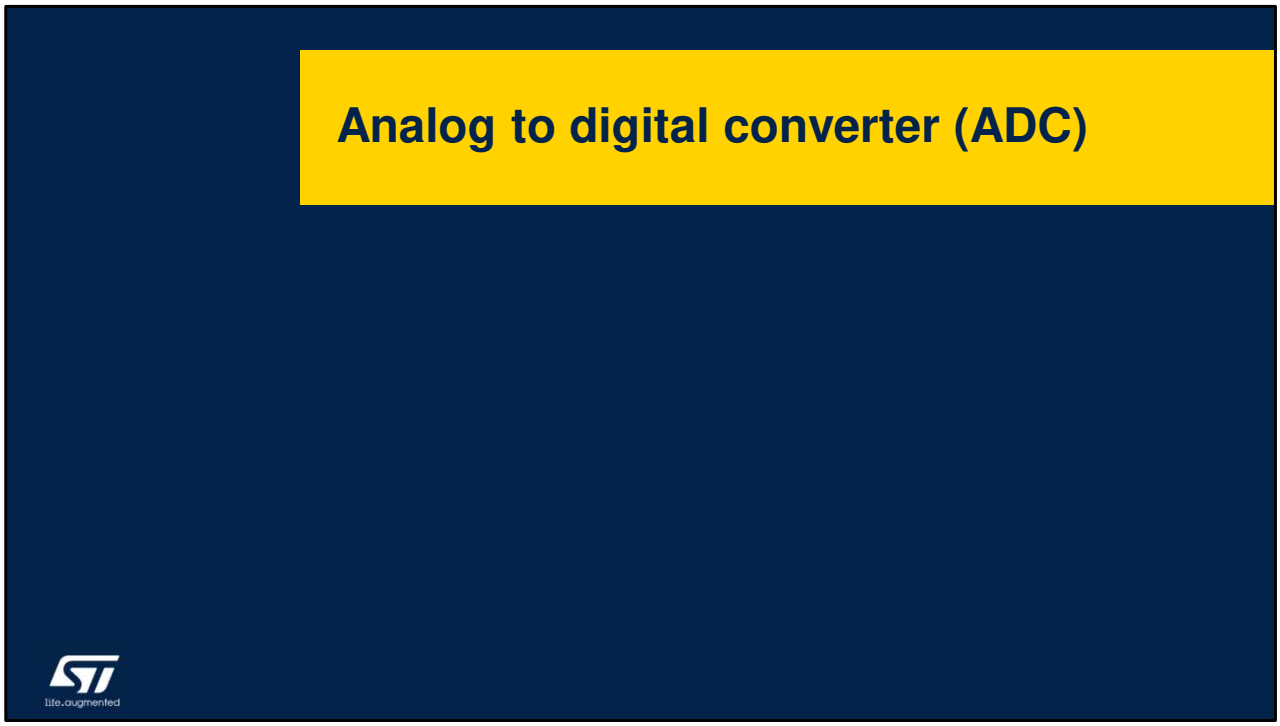
Hello and welcome to this presentation of the STM32U5 Analog-to-Digital Converter or ADC and Digital-to-Analog Converter or DAC.
It will cover the main features of ADC1 and ADC4, which are used to convert analog voltages, like sensor outputs, to digital values for further processing in the digital domain.
The DAC is used to convert digital signals to analog voltages which can interface with the external world and also with on-chip peripherals such as comparators and operational amplifiers.



Let’s start with a description of the features of the ADCs.

ADC Overview

	ADC1	ADC4
Resolution	14 bits	12 bits
Data register	32 bits	16 bits
Maximum sampling speed	2.5Msps	2.5Msps
Hardware linearity calibration	Yes	No
Differential Inputs	Yes	No
Injected channel conversion	Yes	No
Autonomous mode	No	Yes
Concurrent mode protection	-	Yes
Flexible sampling time	Yes	No
Oversampling	Up to x1024	Up to x256
Offset compensation	Yes	No
Gain compensation	Yes	No

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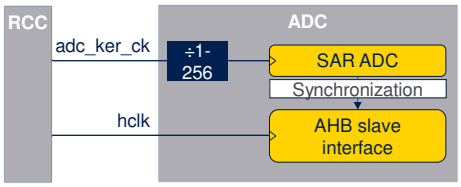
STM32U 575 and 585 products integrate two ADCs: the 14-bit ADC1 and the 12-bit ADC4.
ADC1 is a high-performance converter belonging to the CPU domain, while ADC4 is a low power converter belonging to the SmartRun domain.
The table on this slide highlights the differences between these two ADCs.
First the resolution of ADC1 is 14 bits and the converted data are stored in 32-bit registers, while the resolution of ADC4 is 12 bits and the converted data are stored in 16-bit registers.
The maximum sampling rate is the same for both ADCs: 2.5 megasamples per second.
ADC1 supports a hardware linearity calibration, which is

required for a 14-bit resolution.
ADC4 only converts analog voltage provided by single-ended inputs, while ADC1 also supports differential analog inputs.
For ADC1, conversions are organized in two groups: regular and injected group. The injected group can pre-empt the execution of the regular group sampling sequence.
ADC4 only supports the regular group.
ADC4 supports low-power background autonomous mode (LPBAM), that allows it to be functional and autonomous in Stop 0, Stop 1 and Stop 2 modes (without any software running).
When ADC4 is used simultaneously with ADC1, ADC1 operation might generate noise on the VREF+ voltage. Since VREF+ is also the ADC4 reference voltage, this might cause conversion errors.
To prevent this issue from happening, ADC4 implements a control bit that activates concurrent mode protection.
Each channel of ADC4 can choose one of two sampling times, while each channel of ADC1 can be sampled with a different sampling time.
Raw samples acquired by ADC1 maybe processed by the oversampler, gain and offset compensation units before being provided to the software. The maximum oversampling ratio is 1024.
Raw samples acquired by ADC4 maybe processed by the oversampler before being provided to the software. The maximum oversampling ratio is 256.

ADC1 and ADC4 clocking

- The ADC clock can be selected by RCC
  - No longer directly selectable from the AHB clock
  - Different clock sources can be selected by RCC for adc_ker_ck:
    - Synchronous clock SYSCLK or HCLK
    - pll2_r_ck
    - HSE
    - HSI16
    - MSIK (MSI kernel clock)
  - Both ADCs will work from the same kernel clock



Both ADCs feature a dual clock-domain architecture, which means that the ADC kernel clock is independent from the AHB bus clock that is used to access ADC registers.
ADC1 and ADC4 use the same kernel clock source from RCC.
This synchronizes the ADC1 and ADC4 activity and helps to manage the interference with each other.
Compared to previous generation, there is no option to select the AHB clock, HCLK, as the sampling and conversion clock source,
However, it is possible to choose the kernel clock from SYSCLK or HCLK in the RCC.

ADC input channels

	ADC internal channels	ADC external channels connected to dedicated GPIO pads
ADC1	VREFINT (bandgap voltage =~1.2V) VBAT/4 VSENSE (temperature sensor voltage)	17
ADC4	V_{REFINT} $V_{BAT/4}$ V_{SENSE} V_{CORE} (Digital Core voltage) DAC1_OUT1, DAC1_OUT2	19

- IO booster
  - When VDDA voltage is lower than 2.4V, it is necessary to enable the IO booster circuit, that controls the gate voltage of the analog switch in the GPIOs
  - This is activated by SYSCFG_CFGR1[BOOSTEN,ANASWVDD]

VDD	VDDA	BOOSTEN	ANASWVDD	Gate Voltage
-	> 2.4 V	0	0	VDDA
> 2.4 V	< 2.4 V		1	VDD
< 2.4 V		1	0	Boost Voltage (~3.0V supplied by VDD)

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ADC1 has the following analog input channels:
- 17 external channels
- 3 internal dedicated channels
- One channel for internal reference voltage (VREFINT)
- One channel for internal temperature sensor (VSENSE)
- One channel for VBAT monitoring channel (VBAT/4)

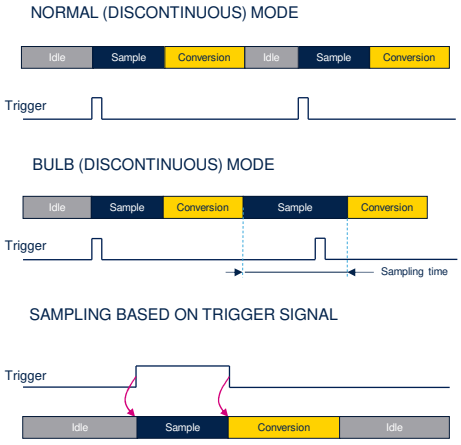
ADC4 has the following analog input channels:
- 19 external channels
- 4 internal dedicated channels
- One channel for the internal reference voltage (VREFINT)
- One channel for the internal temperature sensor (VSENSE)
- One channel for VBAT monitoring channel (VBAT/4)

- One channel for the internal digital core voltage (VCORE)

ADC4 also has an internal connection to the DAC output channels.
The analog switch inside the IO has a resistance which increases when the analog switch supply decreases.
So for cases where VDDA and VDD are low, there is a possibility to enable a voltage booster which will supply the analog switch and guarantee low resistance.
It is recommended to use the VDDA supply for the analog.
But when VDDA is lower than 2.4 Volts and VDD is larger than 2.4 Volts, the power supply can be switched to VDD.
If both VDDA and VDD are lower than 2.4 Volts, the voltage booster should be enabled.

ADC Sampling time control (ADC1)

- Channel-wise programmable sampling time
  - Different sampling times available (5, 6, 12, 20, 36, 68, 391, 814 cycles)
- Flexible Sampling time
  - Bulb sampling mode
    - Only available in discontinuous mode
    - Sampling starts immediately after last conversion.
    - Useful with high impedance sources
    - Very long sampling time
  - Sample time control trigger mode
    - Sampling time is fully controlled by the trigger signal
    - Rising edge starts sampling
    - Falling edge stops sampling and the conversion starts



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This slide describes the sampling time control applicable to ADC1.
The first step of a conversion consists in loading the Sample & Hold capacitor with the voltage to be measured.
Longer sample times ensure that signals having a higher impedance are correctly converted.
The sampling times, in ADC clock cycles, are listed on this slide, from 5 to 814.
The sampling time can be programmed individually for each input channel of ADC1.
The ADC1 implements two mechanisms that were introduced with the STM32G4 series.
The first one is the bulb mode which works only in discontinuous mode.

In this mode, sampling starts immediately after last conversion finishes without going to idle state. This provides less latency from the trigger signal to the start of the conversion.
The very first ADC conversion, after the ADC is enabled, is performed with the sampling time programmed in SMP bits.
The Bulb mode is effective after the second conversion.
The second mechanism is the sampling mode based on the trigger signal.

- Rising edge starts sampling.
- Falling edge stops sampling and the conversion starts.

Calibration

- 14-bit ADC linearity hardware calibration
  - For 14-bit ADC, linear calibration is mandatory to compensate for capacitor array mismatch
  - Calibration must be executed at ADC start up and takes 25502 clock cycles
    - Software can copy the calibration factor to flash memory to speed up the start up sequence at the next wake up
    - Calibration data is independent of temperature and voltage dependency so the customer can perform calibration once during their final production test
- 14- and 12-bit ADC offset calibration (both 14 bits and 12 bits)
  - Offset calibration must be executed at ADC start up and also when VDDA or the temperature changes
    - Calibration takes 683 clock cycles(14 bits), 82 clock cycles (12 bits)
      - Software can copy the calibration factor to flash memory to speed up the start up sequence at the next wake up

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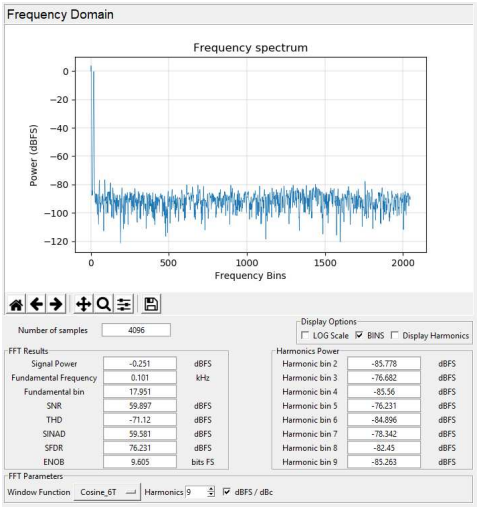
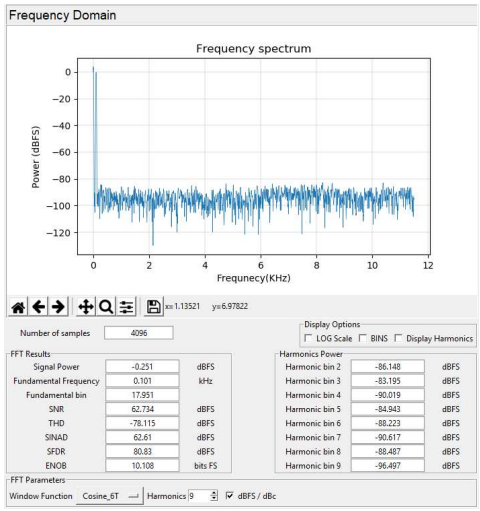
Both ADCs provide an automatic calibration procedure that controls the whole calibration sequence including the ADC power-on and off.
The ADC1 integrates a hardware linear calibration mechanism.
Generally more than 14-bit ADCs require this calibration to compensate for capacitor array mismatch, so like STM32H7 series, linear calibration is included in the STM32U5.
Since the calibration takes 25502 clocks to complete, the calibration value can be stored to flash memory in order to accelerate the ADC boot time.
The linear calibration is independent of voltage and temperature, so it should only be run once during the final

production test.
Both ADC1 and ADC4 support a hardware offset calibration mechanism.
As the offset can be dependent on the voltage or temperature, it might be necessary to re-calibrate in case of significant voltage or temperature change.

Linear Calibration effect



Without Linear Calibration



With Linear Calibration
Measured on NUCLEO, VDD=VDDA=VREF+

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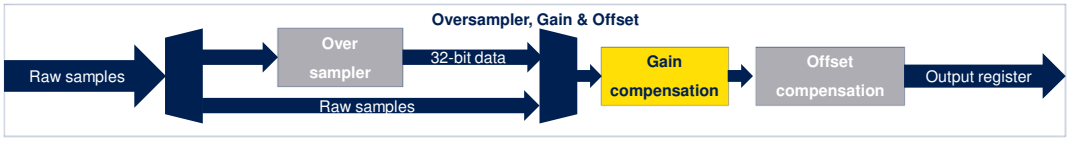
These figure indicate the ADC1's linear calibration effect.
ADC1 is converting 100Hz sinusoid signal.
Without calibration THD indicates -71dBFS, with calibration THD improves to -78dBFS.

Gain compensation (ADC1)



- Gain compensation (**ADC_GCOMP**)
  - Improves the dynamic range of the ADC even when the input range is not aligned with the reference voltage
    - Applying a gain factor helps extend the signal range to map it to the full ADC range
  - It is applied on all converted data (all channels) after oversampling shift
  - Gain factor = (**ADC_GCOMP.GCOMPCOEFF[13:0]**)/4096
  - The gain factor can range from 0 to 3.999756
  - After each conversion, data is computed with the following formula
    - DATA = DATA(adc result) x (GCOMPCOEFF[13:0])/4096

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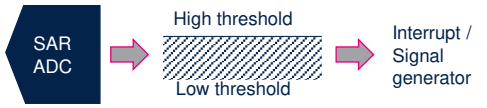
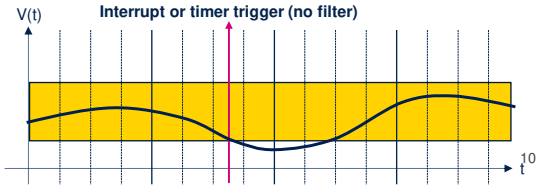
This slide describes the ADC1 gain compensation feature.
A gain factor can be applied to the raw samples in order to improve the dynamic range.
The gain factor is performed after the oversampling.
It is programmable in the range 0 to almost 4 can be adjusted with 0.025% steps.

Analog watchdog filter (ADC1 & ADC4)

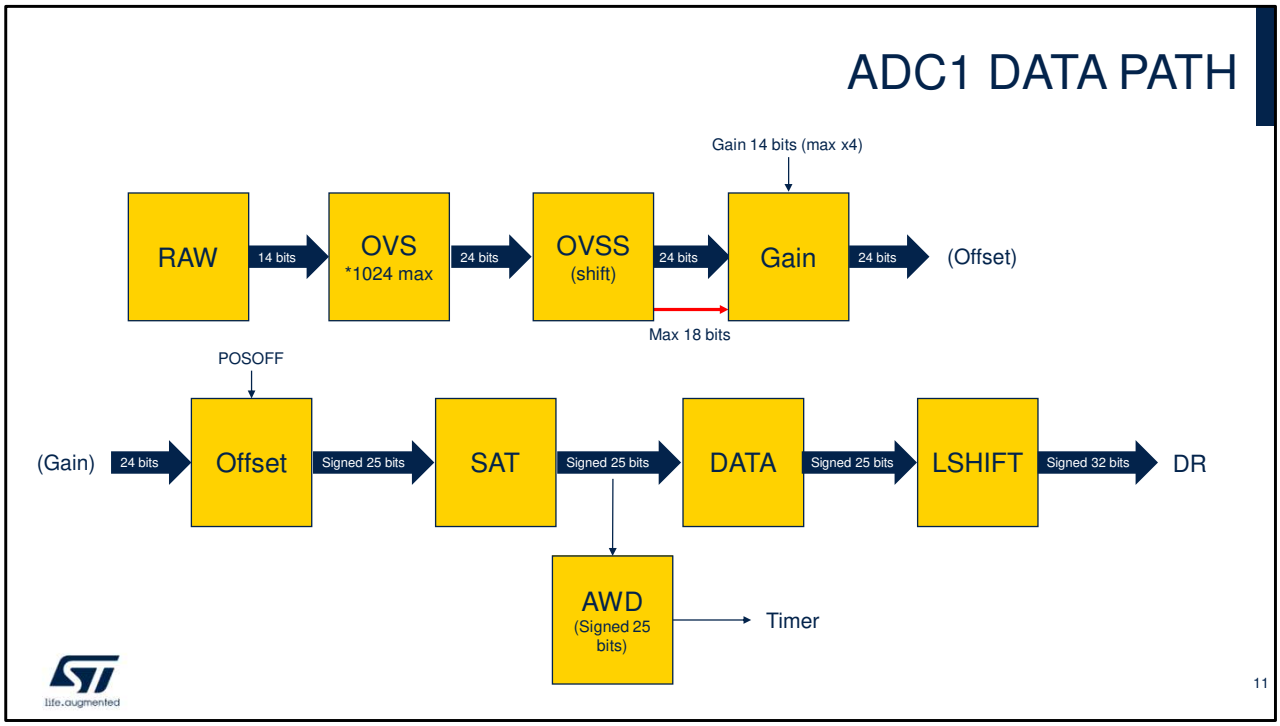
- The ADCs have three Window watchdogs
  - One Analog Watchdog can monitor one selected channel or all enabled channels
  - Two Analog Watchdogs can monitor several selected channels
  - Each watchdog continuously monitors an over- and/or under-threshold condition, then generates either an interrupt or an external signal
- ADC1 analog watchdog filter (only with AWD1)
  - Interrupt or signal generation only after programmable number of consecutive threshold detections



Window Watchdog	Channel to monitor
AWD1	1 (regular, injected, regular or injected) or all (regular, injected, regular or injected)
AWD2	All channels selected in ADC_AWD2CR
AWD3	All channels selected in ADC_AWD3CR



Each ADC has 3 integrated analog watchdogs with high and low threshold settings. The ADC conversion value is compared to this window threshold, if the result exceeds the threshold, an interrupt or timer trigger signal can be asserted without CPU intervention.
Regarding ADC1, the Analog watchdog 1 also has a filtering capability.
If data is out-of-range for a number of times higher than the value specified in AWDFILT in ADCx_HTR1 register, the AWDx flag is set and the corresponding interrupt is issued.



This figure details the various stages of the ADC1 data path, from raw sample to data register update.
Raw data is first passed to the oversampling block and the resulting value can be left or right shifted in the OVSS stage.
The oversampling unit preprocesses the data to offload the main processor. It can handle multiple conversions and average them into a single data with an increased data width, up to 24 bits.
The data then enters the gain stage followed by the offset stage.
The internal multiplier width is 32 bits and the input data width for the gain compensation must be less than 18 bits, because 18 + 14 = 32 bits.

Note that the output of the offset stage is a signed 25-bit value.
Before this data is passed to the analog watchdogs, a saturation control is performed.
The offset correction might result in the data width being wider than the original data. To limit the original width, data saturation can be enabled.
Then finally data is passed to the left shift logic block and stored in the data register.
The OVSS and LSHIFT bitfields in the ADC_CFGR2 register selects the alignment of the data stored after conversion. By default, data are right-aligned

Concurrent mode protection(12 bits)

- When the ADC samples the input signal, it will charge the sample&hold capacitor
  - This will sink (or source) current from the input pin as well as the VREF+ pin
- Two control bits VREFPROTEN and VREFSECSMP improve the concurrent operation of ADC1 and ADC4
  - When VREFPROTEN = 1 and ADC1 starts sampling, ADC4 activity is put on hold for one ADC clock cycle
  - When VREFSECSMP = 1 and ADC1 starts sampling for the injected channel, ADC4 activity is put on hold for one ADC clock cycle
  - This affects the ADC4 conversion latency

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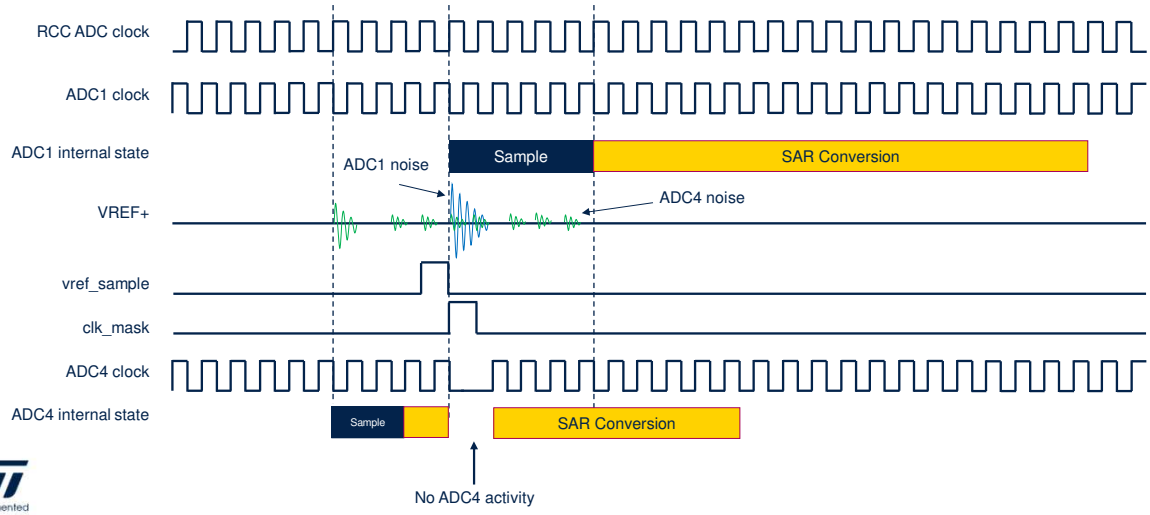
ADC4 implements a mechanism, to support concurrent operation mode.
When ADC1 start sampling, it will create some noise on the VREF+ reference voltage.
If ADC4 runs at that time, the ADC4 conversion result is perturbated.
To avoid such noise, ADC1 uses an internal signal to notify ADC4 that sampling is in progress, so that ADC4 suspends its operation for one clock cycle.
As soon as the ADC1 sampling phase starts, ADC4 is put on hold for one ADC4 clock cycle, thus resulting in an ADC4 conversion time that is one clock cycle longer.
Additionally, ADC1 might have two sampling phases during the ADC4 conversion. This is due to the injected

conversion function of ADC1. By setting VREFSECSMP in the ADC_PWR register, ADC4 operation can be put on hold twice during the conversion phase. When the VREFSECSMP bit is set, the ADC4 is two clock cycles longer.

Concurrent mode timing on STM32U5

- VREFPROTEN=1: Vref protection function is enabled



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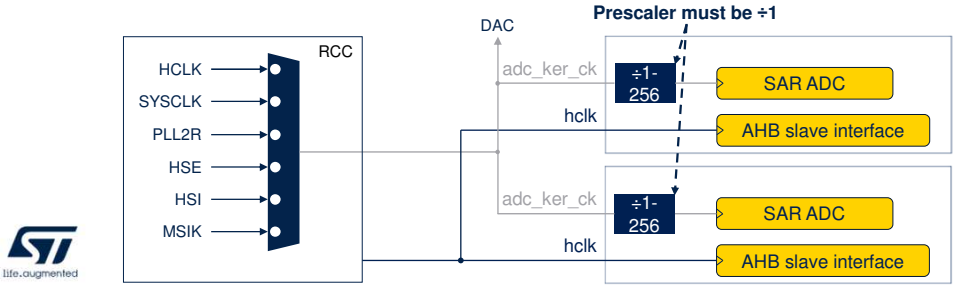
This timing diagram clarifies the VREF protection mechanism, used when ADC1 and ADC4 are used concurrently.
First, ADC4 samples an analog channel. This generates noise on VREF+.
Then ADC1 also starts sampling.
Since VREF protection is enabled, this stalls ADC4 for one clock cycle, thanks to the internal clock mask signal.
During that clock cycle, ADC1 generates noise on VREF+.
One clock cycle later, the conversion resumes in ADC4.
In this way the noise generated by ADC1 will not affect the ADC4 conversion.

Errata

- Simultaneous use of the ADCs
  - When ADC1 performs sampling, it sinks large current pulses, perturbating the VREF+ voltage
  - This VREF+ perturbation can cause an error in the ADC4 conversion
  - ADC4 uses the VREF+ voltage for every clock (successive approximation comparison)
- Limitation
  - To avoid perturbation, both ADCs need to use same clock (same frequency and same phase)



As explained for the previous slide, concurrent sampling on ADC1 and ADC4 can cause errors.
However, just enabling the VREF protection function is not sufficient.
A second condition is required: both ADCs need to use the same clock, same frequency and same phase.
The prescaler used to generate the sampling and conversion clock must be initialized with value 1.

ADC4 autonomous mode

- To reduce the power consumption of the system, ADC4 supports Low-power Background Autonomous Mode (LPBAM) in Stop0, Stop 1 and Stop 2 modes
  - The ADC4 kernel clock is automatically switched on when requested by ADC4, and automatically switched off when ADC4 does not request it
  - The default state of ADC4 is power off
  - Hardware trigger to ADC issues the clock request, the ADC regulator is then enabled and the ADC conversion starts
  - ADC result can be used for analog watchdog or DMA transfer
  - Once the programmed conversion is finished, the clock request is de-asserted and ADC4 re-enters a power off state

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ADC4 supports the autonomous mode to further reduce the system power consumption.
In this mode, the ADC defaults to power off state.
When a hardware trigger is detected, the ADC4 powers up and then issues a clock request.
The ADC4 start sequence is managed by a state machine.
Once this sequence has completed, the ADC conversion is performed.
The resulting ADC data can be used by an analog watchdog or transferred to memory by the LPDMA.
Once all planned conversions are finished, the clock is stopped and ADC returns to power off state.
During this sequence, the Cortex-M33 is not involved.

ADCs ~~target~~ specification

ADC features	STM32L5 12-bit ADC	STM32U5 12-bit ADC4	STM32U5 14-bit ADC1
VDDA	1.62 to 3.6V		
VREF+	2V to VDDA if VDDA>2V or = VDDA if <2V	1V to VDDA	2V to VDDA if VDDA>2V or VDDA if <2V
Resolution	From 6 to 12 bits		From 8 to 14 bits
Effective Number Of Bits (ENOB)	10.9 bits (differential)	10.90 bits	12.8 bits (differential)
fADC (ADC clock frequency)	Up to 80MHz	Up to 55MHz	Up to 55MHz
Max Speed	5 Msps	2.5 Msps	2.5Msps
Inputs	Single and Differential	Single end only	Single and Differential
ts (Sampling time)	From 2.5 to 640.5 ADC clock cycles	From 1.5 to 160.5 ADC clock cycles	From 5 to 814 ADC clock cycles
tconv (conversion time)	t_s + 12.5 ADC clock cycles (for 12 bits resolution)		t_s + 17 ADC clock cycles (for 14 bits resolution)
IDD from VDDA	16 µA at 10 ksps 160 at 1 Msps (730 at 5 Msps)	10 µA at 10 ksps 180 µA at 1 Msps 360 µA at 2.5 Msps	130 µA at 10 ksps 550 µA at 1 Msps, differential inputs, 14-bit 970 µA at 2.5 Msps, differential inputs, 14-bit

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This table compares the characteristics of the STM32U5 ADC1 and ADC4 with STM32L5 ADCs.
The VDDA voltage range is the same, the VREF+ voltage range is the same for STM32L5 ADC and STM32U5 ADC1. ADC4 supports a VREF plus range from 1 volt to VDDA.
The Effective number of bits (ENOB) is a measure of the dynamic range of the ADC. In differential mode, the ENOB of STM32U5's ADC1 reaches 12.8 bits.
Thanks to its higher frequency, the maximum number of mega samples per second is larger for STM32L5's ADCs compared to STM32U5's ADCs.
The ADC4 of STM32U5 does not support differential inputs.

Note that the minimum sampling time for STM32U5's ADC4 is only 1.5 clock cycles.
The larger the resolution, the longer the conversion time.
The 14-bit ADC4 also consumes more than 12-bit ADCs.
For low acquisition frequencies, the ADC4 of the STM32U5 consumes less than the ADCs of STM32L5, which is convenient when periodic voltage monitoring is performed in LPBAM.

Digital to analog converter (DAC)

Now let’s look at the features of the DAC.

DAC

- One DAC interface, two outputs
- When the DAC output is connected to the OPAMP/Comp/ADC, the GPIO can be used for other functionalities
- Sample and hold mode for autonomous mode
  - DAC output voltage can be updated during Stop Mode
  - Hardware trigger to the DAC causes a clock request, then the LPDMA can update the DAC output register
  - Once the DMA transfer is finished, the clock request is de-asserted
- The DAC is now an AHB slave device, not the APB slave device
- The DAC kernel clock is common to the ADCs to avoid perturbation

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The STM32U575/585 integrates one DAC module with two analog outputs.
The Basic functionality is very similar to the DAC of STM32L5.
The DAC output can be routed to internal resources without using GPIO.
The dac_outx can use an internal pin connection to on-chip peripherals such as a comparator and operational amplifier.
The STM32U5 DAC supports Low-power Background Autonomous Mode (LPBAM) in Stop0, Stop 1 and Stop 2 modes.
By using the LPDMA and a hardware trigger, the DAC output can be updated even when the system clock is

stopped.
In this mode, the DAC only supports the Sample and Hold mode, using the LSI/LSE clock source for static conversion.
Uniike the STM32L5, the DAC is connected to the AHB bus, which offers a larger bandwidth than APB.
To minimize perturbations on VREF+, the kernel clock is the same as ADC1 and ADC4.

DAC specification

		STM32L5 Typical	STM32U5 Typical	Unit
VDDA	Buffer On	1.8 ~ 3.6	1.6 ~ 3.6	V
	Buffer Off	1.71 ~ 3.6	1.6 ~ 3.6	V
Resolution		12	12	bits
Differential Non Linearity (DNL)		+/- 2	+/- 2	LSB
Integral Non Linearity (INL)		+/- 4	+/- 4	LSB
Consumption	Buffer On	500	500	uA
	Buffer Off	155	14	uA
Settling time	Buffer On (50pF)	1.7	2.05	usec
	Buffer Off (10pF)	2.0	1.7	usec
Update rate	Buffer On (50pF)	1	1	Msamples/s

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This table compares the characteristics of the STM32U5's DAC with the STM32L5's DAC.
The STM32U5's DAC can work between 1.6 and 3.6 volts whether the buffer state is on or off.
When the DAC output buffer is ON or the DAC_OUT pin is connected, the minimum VDDA voltage value is 1.8V for the STM32L5 DAC.
12-bit monotonicity is guaranteed.
Operating at 1 Mega sample per second, power consumption is almost equivalent with respect to STM32L5.
By using Sample & Hold mode, the current consumption can be drastically reduced.
The STM32U5's DAC buffered output has a settling time of

2.05 µsec whatever the capacitive load up to 50 pF. The DAC can handle a sampling rate of 1 mega sample per second.

Thank you

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Several application notes dedicated to analog-to-digital converters are available.
To learn more about ADCs, you can visit a wide range of web pages discussing successive approximation analog-to-digital converters.
In addition to this presentation, you can refer to the following presentations:

- Reset and Clock Control
- Power management.