Hello, and welcome to this presentation of the STM32C0 System Configuration Controller.

Overview

- STM32C0xx microcontrollers feature a set of configuration registers
- The main purposes of the system configuration controller are the following:
  - Enabling /disabling I2C Fast-mode Plus high-drive
  - Configuring the Infrared Timer (IRTIM) module
  - Remapping the PA11 and PA12 GPIOs to PA9 and PA10
  - Selecting the memory accessible at address 0x0000_0000
  - Status of pending interrupts from each interrupt line
  - Enabling/disabling safety features

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STM32C0 microcontrollers feature a set of configuration registers located in the SYSCFG module.
The System Configuration Controller gives access to the following features:

- Enabling /disabling I2C Fast-mode Plus high-drive
- Configuring the Infrared Timer (IRTIM) module
- Remapping the PA11 and PA12 GPIOs to PA9 and PA10
- Selecting the memory accessible at address 0x0000_0000
- Status of pending interrupts from each external interrupt line
- Enabling/disabling safety features

I2C I/Os Fast-mode

- The I2C controller of the STM32C0 supports three speeds

Mode	Bit Rate	Extra output drive I/Os
Standard-mode (Sm)	≤ 100 Kbps	NO
Fast-mode (Fm)	≤ 400 Kbps	NO
Fast-mode Plus (Fm+)	≤ 1 Mbps	YES

- Extra output drive is controlled by the SYSCFG module
  - It can be enabled even when I2C is not the selected alternate function

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The I2C controller present in the STM32C0 supports 3 speeds:

- Standard-mode, the maximum bitrate is 100 Kilobits per second
- Fast-mode, the maximum bitrate is 400 Kilobits per second
- Fast-mode Plus, the maximum bitrate is 1 Megabit per second.

Fast-mode Plus requires a high drive capability, which is enabled in the SYSCFG module.
Since high-drive is controlled at pin level, it is also available for the other alternate functions.

I2C I/Os Fast-mode

Pin	I²C alternate function	I²C FM+ mode enabled
PC14	I2C1_SDA	SYSCFG_CFGR1[I2C_PC14_FMP]=1 OR SYSCFG_CFGR1[I2C1_FMP]=1
PA9	I2C1_SCL	SYSCFG_CFGR1[I2C_PA9_FMP]=1 OR SYSCFG_CFGR1[I2C1_FMP]=1
PA10	I2C1_SDA	SYSCFG_CFGR1[I2C_PA10_FMP]=1 OR SYSCFG_CFGR1[I2C1_FMP]=1
PB6	I2C1_SCL	SYSCFG_CFGR1[I2C_PB6_FMP]=1 OR SYSCFG_CFGR1[I2C1_FMP]=1
PB7	I2C1_SDA	SYSCFG_CFGR1[I2C_PB7_FMP]=1 OR SYSCFG_CFGR1[I2C1_FMP]=1
PB8	I2C1_SCL	SYSCFG_CFGR1[I2C_PB8_FMP]=1 OR SYSCFG_CFGR1[I2C1_FMP]=1
PB9	I2C1_SDA	SYSCFG_CFGR1[I2C_PB9_FMP]=1 OR SYSCFG_CFGR1[I2C1_FMP]=1

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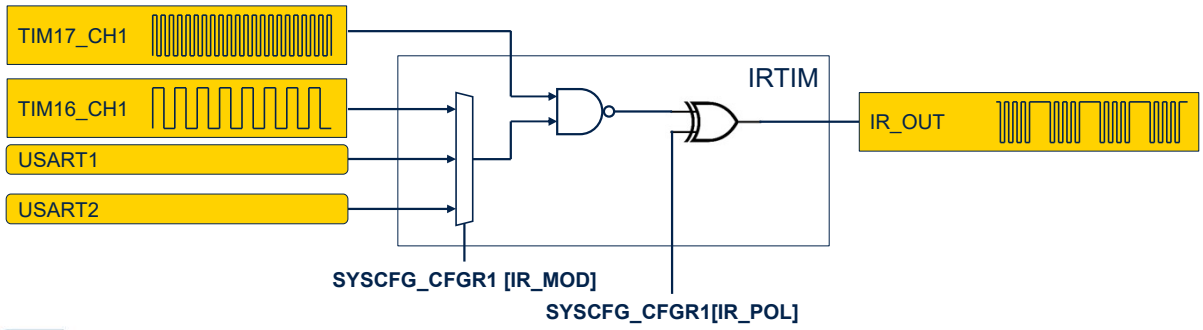
The high-drive capability of the I2C1 pins can be configured per pin through the I2C_PC14_FMP, I2C_PA9-10_FMP and I2C_PB6-9_FMP bits.

IRTIM Module Configuration

- The Infrared Timer (IRTIM) module relies on USART and Timer sources to generate the modulation envelope
  - The SYSCFG module is used to select the source signal
  - It is also used to activate an output inverter



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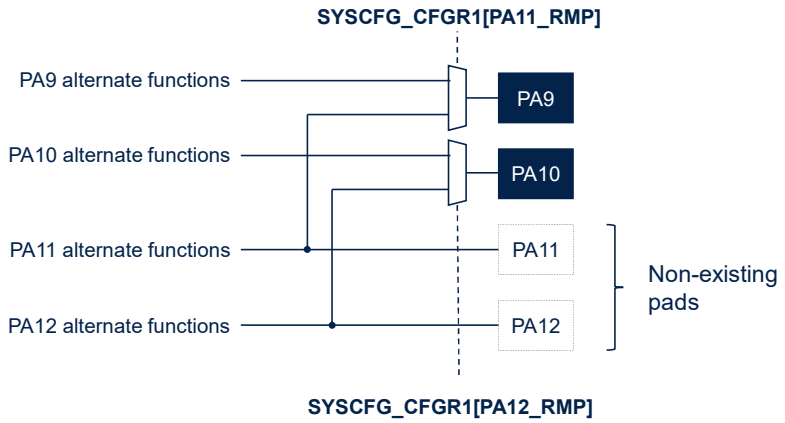
The Infrared Timer (IRTIM) unit requires a modulation envelope signal that is provided either by USARTs or by TIM16.
The IR_MOD field in SYSCFG_CFGR1 register controls the related input multiplexer.
The IR_POL bit in the SYSCFG_CFGR1 register selects whether the output signal is inverted.

GPIO Remap

- Two GPIOs PA12 and PA11 can be remapped by PA10 and PA9 respectively in order to give access to their functions when the Pins are not natively available on the package



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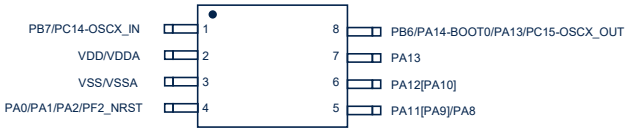
When the PA11_PA12_RMP bit in the SYSCFG_CFGR1 register are set, the PA11 and PA12 alternate functions are remapped to pins PA9 and PA10.
This is useful when these alternate functions are needed, because PA11 and PA12 have no dedicated IO pads.

GPIO Multibonding

- One PIN on package bonded to multiple PADs on the silicon
  - i.e. PA0, PA1, PA2, PF2-NRST bonded to the PIN #4 of SO8 package



- When several GPIOs are internally connected to the same pin, SYSCFG_CFGR3 register allows assigning only one to keep setting specified by its corresponding GPIOx_MODER register like digital output
  - The other GPIOs are forced into digital input mode regardless their corresponding GPIOx_MODER register settings

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One PIN on the package can be bonded to multiple PADs on the silicon for instance. PA0, PA1, PA2, PF2-NRST bonded to the PIN #4 of SO8 package.
When several GPIOs are internally connected to the same pin, the SYSCFG_CFGR3 register allows assigning the one to keep setting specified by its corresponding GPIOx_MODER register.
The other GPIOs are forced into digital input mode regardless their corresponding GPIOx_MODER register settings.

GPIO Multibonding – security

- The default and secure settings can be overridden by clearing SECURE_MUXING_EN bit in FLASH_OPTR
- Such action must be thoroughly considered as it can cause conflict on connected GPIOs (short-circuit) in case of wrong GPIO configuration

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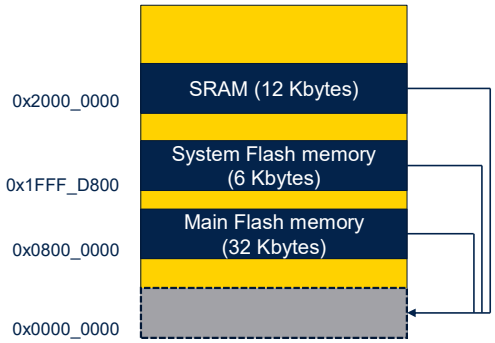
The default setting when the SECURE_MUXING_EN bit is set in FLASH_OPTR is described on the previous slide.
It is safe, because the configuration in which any 2 GPIOs bonded together with Push-pull output configuration with different output levels cannot happen.
However, for some application it may be beneficial to multiply the maximum output current on the PIN by using several GPIOs bonded together to boost the total output current on such particular PIN.
If the SECURE_MUXING_EN bit is cleared in FLASH_OPTR, the user can enable output on more GPIOs bonded together in GPIOx_MODER register.
The user software must ensure that there is no conflict between the GPIOs.

Memory Mapping

- Three memories can be aliased at address 0x0000_0000
  - Main Flash memory
  - System Flash memory
  - Embedded SRAM



SYSCFG_CFGR1[MEM_MODE]
=0bX0: Main Flash memory
=0b01: System Flash memory
=0b11: SRAM
- Default value depends on the state of pins BOOT0, nBOOT1, nBOOT0 and BOOT_SEL Option bits and BOOT_LOCK control bit

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The MEM_MODE field in the SYSCFG_CFGR1 register selects which memory is accessible at address 0.
Three memories can be aliased to address 0: Main Flash memory, System Flash memory or SRAM.
Note that the default setting of this field depends on boot pin, option bytes and control bit.

Safety Features

- The SYSCFG_CFGR2 register controls safety features:
  - One bit is used to enable/disable the assertion of TIM1/16/17 Break input when the Cortex®-M0+ lockup occurs
  - When a fault or supervisor call occurs at a priority of -1 or -2, the Cortex-M0+ automatically enters lockup state

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The SYSCFG_CFGR2 register contains the control and status bits linked to safety.
LOCKUP_LOCK control bit enables the connection of Cortex-M0+ LOCKUP state towards the timers break inputs.
This allows timer outputs to be placed in a known state during an application crash.
Once programmed, the connection is locked until the next system reset.

Interrupt Line Status Registers

- A dedicated set of read-only registers is implemented in the SYSCFG module to collect all pending interrupt sources associated with each interrupt line into a single register
  - This allows users to check by a single read operation which peripheral requires service
  - In order to explain the benefit of these registers, the next slide describes the management of EXTI interrupt requests

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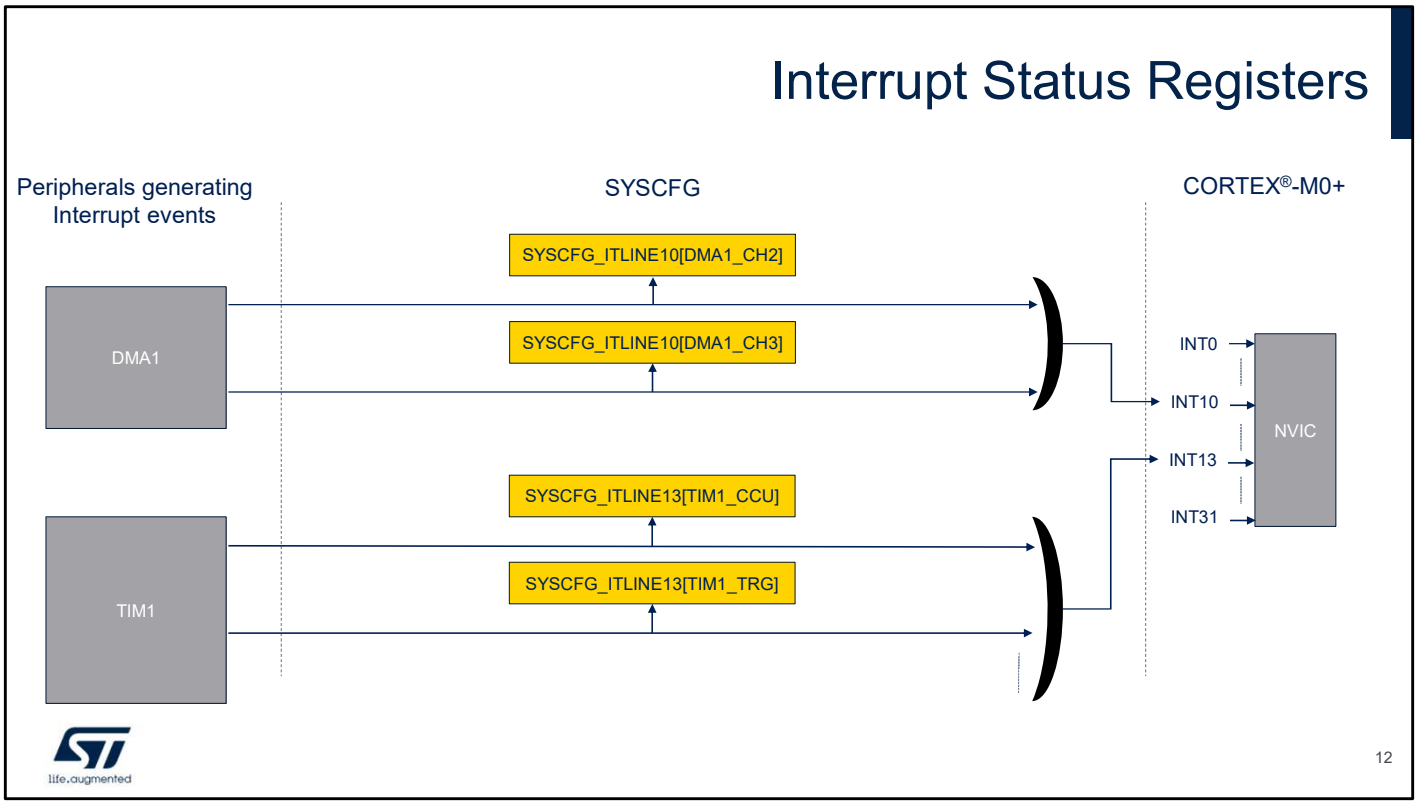
The SYSCFG module supports 4 interrupt line status registers. They enable software to easily find the cause of an EXTI interrupt, by having in the same register all pending interrupt sources associated with a particular interrupt line.
In the STM32C0, there is one interrupt line status register per peripheral capable of asserting an external interrupt.
The benefit of these interrupt line status registers is explained in the next slide.



The left part of the figure represents the peripherals able to assert external interrupts.
The SYSCFG interrupt status registers appear in the middle of the figure.
The connection of the external interrupts to the NVIC is indicated on the right part of the figure.

Related peripherals

- Refer to these training modules linked to this peripheral:
  - Inter-Integrated Circuit (I²C)
  - Infrared Timer Interface (IRTIM)
  - General-purpose Input/Output (GPIO)
  - Interrupts (NVIC-EXTI)
  - Timers (TIM)

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In addition to this presentation, you can refer to I2C, IRTIM, GPIO, interrupts and timers training modules.

References

- For more details, please refer to following documentation:
  - AN2606: STM32 microcontroller system memory boot mode

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For more details, please refer to application note AN2606: STM32 microcontroller system memory boot mode.

Thank you

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Thank you for attending this presentation!