Hello, and welcome to this presentation of the RAM configuration controller which configures the features of the internal SRAMs: SRAM1, SRAM2, SRAM3, SRAM4, and Backup SRAM.

RAM Configuration Overview

- Error code correction (ECC on SRAM2/3 & BKPSRAM)
- SRAM-ECC software disable with Keys
- SRAM software erase with key
- Write protection (1-Kbyte granularity on SRAM2)
- Programmable wait states for voltage scaling Range 4

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The RAM configuration controller is in charge of:

- Handling the error code correction, or ECC, supported by SRAM2, SRAM3 and backup SRAM
- Disabling ECC through a software sequence based on a key register
- Performing global SRAM erasure through a software sequence also based on a key register
- Protecting SRAM2 against write accesses for each 1-KB chunk
- And programming the number of wait states according to the actual frequency when the microcontroller is in voltage range number 4.

SRAMs Features

X = supported feature	SRAM1 (192 KB)	SRAM2 (64 KB)	SRAM3 (512 KB)	SRAM4 (16 KB)	BKPSRAM (2 KB)
LPBAM in Stop 0/1	X	X	X	X	X
LPBAM in Stop2	-	-	-	X	-
Optional retention in Standby	-	X	-	-	X
Optional retention in VBAT	-	-	-	-	X
Erased with RDP regression	X	X	X	X	X
Erased with tamper detection	-	X	-	-	X
Optionally erased with system reset	X	X	X	X	-
Software erase	X	X	X	X	X
ECC	-	X	X	-	X
Write protection	-	X	-	-	-
Wait states	X	X	X	X	X

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This table summarizes the features of the internal SRAMs. Let us start with the features supported by all internal SRAMs:

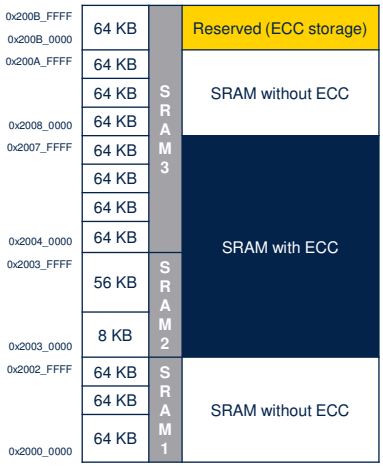
- Low-power background autonomous mode in stop 0 and stop 1 modes
- Erasure when the Readout Protection level is decreased
- Software erase
- Adjustment of the number of wait states in voltage range 4.

Low-power background autonomous mode in stop 2 is only supported by SRAM4, because it belongs to the smartrun domain. The smartrun domain architecture relies on a DMA allowing autonomous operation during low-power modes down to Stop 2.

The contents of SRAM2 and backup SRAM can be retained in standby mode.
The contents of backup SRAM can be retained in VBAT mode.
SRAM2 and optionally backup SRAM are protected by the tamper detection circuit, and are erased by hardware in case of tamper detection.
The ECC is supported by SRAM2, SRAM3 and backup SRAM when enabled with the SRAM2_ECC, SRAM3_ECC and BKPSRAM_ECC user option bits.
The SRAM2 is made of 64 1-Kbyte pages. Each 1-Kbyte page can be write-protected by setting its corresponding PxWP bit in configuration registers.

SRAM1/2/3 memory map with ECC

- ECC Storage:
  - SRAM3: 64 Kbytes area, the upper block
  - SRAM2: the data bus is 39 bits (7 bits for ECC Storage and 32 bits for data) so that the entire SRAM2 is ECC protected
- SRAM3 ECC specific management:
  - When ECC is enabled, only the first 256 Kbytes of SRAM3 are with ECC
  - The next 192 Kbytes are without ECC
- ECC
  - SEDC: Single Error Detection Correction (Interrupt)
  - DED: Double Error detection (interrupt or NMI)



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SRAM2, SRAM3 and backup SRAM implement a unit capable of detecting and correcting single bit errors and detecting double bit errors, thanks to seven ECC bits, that are added per 32 bits of data.
Four 64-KB blocks of SRAM3 and the 64 kilobytes of SRAM2 are ECC protected.
Regarding SRAM3, the ECC codes are stored in a dedicated part of the SRAM: the upper 64-kilobyte part of SRAM3. This area shall not be used by applications.
Regarding SRAM2, the information which is stored is 39-bit wide, 32-bit data +7-bit ECC. Consequently the entire SRAM2 is ECC protected.
Optionally, the full SRAM2 or 8 Kbytes or 56 Kbytes can be retained in Standby and Stop 3 modes, supplied by the

low-power regulator. This is called standby with SRAM2 retention mode.
ECC error detection is reported to the Cortex-M33 as follows:
- Single error detection and correction cause an interrupt request
- Double error detection causes a non-maskable interrupt
- The failing address is latched in a register.

Activating/Deactivating ECC by software

- When ECC is enabled (by user option bits), the ECCE bit is automatically set after system reset
- The ECC can be deactivated by executing a software sequence:
  - This helps to check ECC effects on the application
- When ECC is deactivated (ECCE = 0), the SRAM3 ECC storage area can be read and written for ECC user test purposes
- When the ECC is activated (ECCE = 1), this area is reserved for ECC storage purpose and cannot be read nor written

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ECC can be automatically enabled by programming user option bits in the flash memory.
ECC can be disabled by executing a software sequence that writes keys into ECC key registers.
Since ECC requires a read-modify-write operation when writing partial data (byte or halfword), the performance can be measured with and without ECC.
When ECC is disabled in SRAM3, the last 64 kilobyte block containing the ECC codes is accessible by masters. This can be used for error injection.
When ECC is enabled in SRAM3, this area is reserved and cannot be accessed by masters.

RAM Wait States (WS)

Wait States (Latency)	HCLK in VOS Range 1	HCLK in VOS Range 2	HCLK in VOS Range 3	HCLK in VOS Range 4 & LPBAM
0 WS (1 AHB cycle)	≤ 160 MHz	≤ 100 MHz	≤ 50 MHz	≤ 12 MHz
1 WS (2 AHB cycle)	-	-	-	≤ 24 MHz

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To correctly read data from SRAMs, the appropriate number of wait states must be programmed, depending on the AHB clock frequency (HCLK) and voltage scaling range, as shown in this table.
Note that 1 wait state is required in range 4, when the frequency exceeds 12 megahertz.

Write protection (SRAM2)

- The SRAM2 is made of 64 x 1-Kbyte pages of granularity
- Each 1-Kbyte page can be write-protected independently
- Set the PxWP (x = 0 to 63) bit in *RAMCFG_RAM2WPR1* and *RAMCFG_RAM2WPR2*

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The SRAM2 is made of 64 1-Kbyte pages. Each 1-Kbyte page can be write-protected by setting its corresponding PxWP bit in the RAMCFG memory 2 write protection 1 and 2 registers.
Two registers are necessary to form a bitmap of 64 bits.
The consequence of attempting to write to write-protected page is that the SRAM controller returns an error response to the AHB master.
When this master is the Cortex-M33 CPU, this error causes a bus fault exception.
When this master is a DMA channel, this error is interpreted as a DMA transfer error.

Software erase

- SRAM erase can be requested by executing a software sequence
- In case of read/write access to SRAM while ongoing erase to the same address then wait states (AHB cycles) are automatically inserted until the end of the erase
- Total erase duration :

  N AHB clock cycles, where N is the size of the SRAM in 32-bit words
- Note: not possible to access the RAM during an erase cycle:
  - SRAMBUSY flag is set in the SRAM interrupt status register as long as the erase is ongoing
  - Accesses are blocked
  - Wait states are inserted on the AHB bus until the end of the erase operation

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SRAM erase can be requested by executing a software sequence, based on keys that have to be written to key registers.
SRAMBUSY flag is set in the related SRAM interrupt status register as long as the erase is ongoing.
The total duration of each SRAM erase is equal to N AHB clock cycles, where N is the size of the SRAM in 32-bit word units.
If the SRAM is read or written while an erase is ongoing, wait states are inserted on the AHB bus until the end of the erase operation.

RAMCFG interrupt

- Interrupts:
  - SEDC with interrupt generation
  - DED with interrupt or NMI generation
  - SEDC and DED status
  - Failing addresses are latched in registers

	Interrupt event	Exit Sleep mode	Exit Stop mode	Exit Standby modes
RAMCFG	ECC single error detection and correction	Yes	Yes (Stop 0/1)	No
	ECC double error detection	Yes	Yes	No
NMI	ECC double error detection	Yes	Yes	No

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The RAM configuration controller generates the following interrupt requests:

- A regular interrupt in the event of a single error detection and correction
- The non-maskable interrupt in the event of a double error detection.

Status registers provide the current status of these events, the address at which a correctable error has been detected and the address at which a non-correctable error has been detected.

Note that these addresses are locked until software clears the Address latch enable bit in the control register.

The table indicates the effect of low power modes on the RAM configuration controller.

Sleep mode has no effect, RAMCFG interrupts cause the microcontroller to exit the sleep mode.
In stop mode, the contents of RAMCFG registers and SRAM contents are kept, the ECC is functional and ECC error interrupt or NMI causes the microcontroller to exit the stop 0 and stop 1 modes.
In Stop3, no SRAM access is possible.
In Stop2, only SRAM4 remains accessible in the SmartRun Domain by implementing the low-power background autonomous mode, or LPBAM.
So in Stop2 and Stop3, no ECC error can occur, because SRAM4 is not ECC protected.
In standby mode, the RAMCFG module is powered down and must be reinitialized after exiting standby.

Thank you

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Thank you for attendeding this presentation on the RAM configuration controller!
In addition to this presentation, you can refer to the presentation on power management.