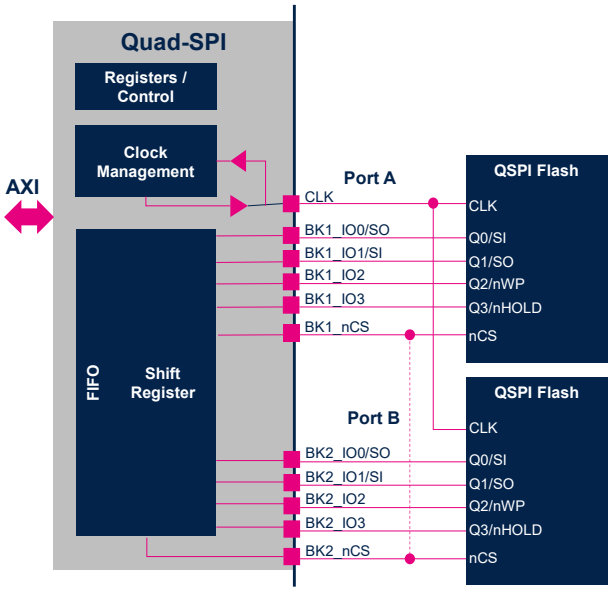
Hello, and welcome to this presentation of the STM32 Quad-SPI memory interface. It covers the features of this interface, which is widely used for connecting external memories to the microprocessor.

Single or dual Quad-SPI access?

Flexible selection between number of pins and performance

- Quad-SPI supports single and dual external Flash operation(*)
  - Port A and port B can operate simultaneously on two memories of same type and characteristics.
  - Port A and port B can operate non-simultaneously with different types of Flash memories (e.g : NOR + NAND)
- 4-bit or 8-bit data bus



* : depends on part numbers

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2

The Quad-SPI memory interface integrated inside STM32MP1 microprocessors provides a communication interface, allowing the microcontroller to communicate with external SPI and Quad-SPI memories.
The Quad-SPI memory interface supports the connection of one or two external memories. This means that data can be transferred over a 4- or 8-bit data bus in between the memory and the microcontroller. It gives the user flexibility to choose between the number of pins required for connection (6 for a single and 10 for a double connection) and the performance of the data transfer (4 bits for a single or 8 bits for a double connection).

Key features

- Three operating modes
  - Indirect
  - Status-polling
  - Memory-mapped
- Optimized operations for communication (**)
  - Dual-Flash mode* (8 bits for accessing two Flash memories in parallel)
  - Single data rate (SDR) and Dual data rate (*) (DDR) support

* : Depends on part numbers
** : Maximum frequency is product dependent, please refer to the product datasheet

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The Quad-SPI memory interface offers three operating modes. It is optimized for communication with external memories with support for Dual-Flash mode, allowing to access 8 bits in a single reading cycle. It also supports both single- and dual-data rate operation.

Operating modes

Flexible operating modes to reduce CPU load

- Indirect mode
  - All the operations are performed through registers (classical SPI)
- Status polling mode
  - Automatic periodical read of the Flash status registers and interrupt generation on match
- Memory mapped mode
  - External Flash seen as internal for read operations

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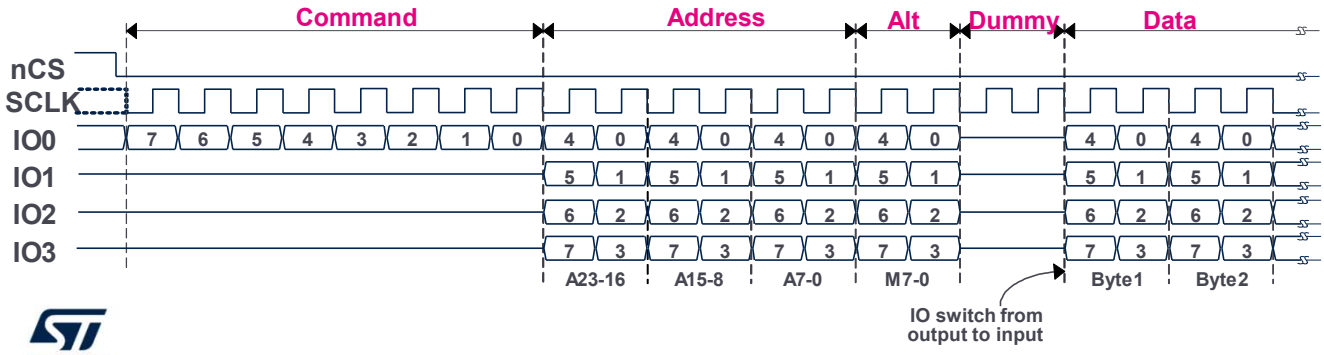
4

The Quad-SPI memory interface operates in three different modes:
1. Indirect mode, where it behaves as classical SPI interface and all operations are performed through registers,
2. Status-polling mode, where the Flash status registers are read periodically with interrupt generation,
3. Memory-mapped mode, where the external memory is seen as an internal memory for read operations.

Frame format

Compatible with any single/dual/quad SPI serial Flash memory

- Quad-SPI commands contain up to 5 configurable phases
  - Each phase could be enabled or disabled
  - Configurable length for each phase
  - Configurable number of lines for each phase



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5

The Quad-SPI memory interface offers high flexibility in frame format configuration. This flexibility allows it to address any serial Flash memory. Users can enable or disable each of the five phases and configure the length of each phase as well as the number of lines used for each phase.

Indirect operating mode

Classical SPI interface

- Same use as a classical communication IP
  - The data is transferred by writing or reading a data register
  - Number of bytes specified in the data length register
- Management of data FIFO with
  - Interrupts flag (Transfer Complete Flag)
  - DMA support
- Launching a command
  - When writing the instruction if only the instruction is needed
  - When writing the address if only the instruction & address are needed
  - When writing the data when the data phase are needed

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The Quad-SPI memory interface used in indirect operating mode behaves like a classical SPI interface. Transferred data goes through the data register with FIFO. Data exchanges are driven by software or by the DMA controller, using related interrupt flags in the Quad-SPI status registers.
Each command is launched by writing the instruction, address or data, depending on the instruction context.

Status polling operating mode

Reduced software overhead

- Specific mode for polling a Status register
  - Programmable register length: 8/16/24/32-bit
  - Repeats the read operation at a defined rate
- Mask the response and generate an interrupt in case of match
  - Programmable mask (PSMKR register)
  - The masked value is compared bit per bit with the match register (PSMAR)
  - The result of the comparison can be ANDed or ORed.
  - Interrupt is generated when succeed (Stop on Match Flag)
- Automatic stop when a match occurs

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7

A specific mode has been implemented in the Quad-SPI interface to autonomously poll the status registers in the external Flash memory. The Quad-SPI interface can also be configured to periodically read a register in the external Flash memory. The returned data can be masked to select the bits to be evaluated. The selected bits are compared with their required values stored in the match register. The result of the comparison can be treated in two ways: in ANDed mode, if all the selected bits are matching, an interrupt is generated. In ORed mode, if one of the selected bits is matching, an interrupt is generated. When a match occurs, the Quad-SPI interface can stop automatically.

Memory-mapped mode

- **Simple extension of memory into the project**
- **Low-power management**

- Prefetch for eXecute-in-Place (XiP)
- External Flash seen as an internal one with wait states
  - Read operations are automatically generated on AXI-interface
  - Frame & opcode defined during IP configuration as for Indirect mode
- Pin nCS is held low and clock is stopped to stall the Quad-SPI bus and relaunch a sequential read if needed
- Timeout counter to release pin nCS High for low power

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8

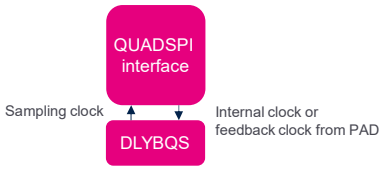
The Quad-SPI memory interface also has a Memory-mapped mode. The main application benefit introduced by this mode is the simple integration of an external memory extension thanks to there being no difference between the read accesses of internal or externally-connected memories, except for the number of wait states.
This mode is only suitable for read operations and the external Flash memory is seen as internal one with wait states included to compensate for the lower speed of the external memory.
The maximum size supported by this mode is limited to 256 Mbytes.
The prefetch buffer supports execution in place, therefore code can be executed directly from the external memory without having to download it into the internal RAM.
This mode also supports SIOO mode (Send Instruction Only Once) supported by certain Flash memories, which allows the controller to send an instruction only once and to remove the

instruction phase for following accesses.

Delayed data sampling

Useful when signals are delayed due to PCB layout

- The sampling clock can be shifted by an additional ½ clock cycle
  - Supported only in SDR mode
- The output data can be shifted by a ½ system clock cycle
  - Supported only in DDR mode
- In addition, a dedicated delay block DLYBQS allows to fine-tune the timing of the sampling clock for improved performance



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9

Delayed data sampling allows users to compensate for the delay of the signals due to constraints on the PCB layout optimization. It allows applications to shift the data sampling time by an additional ½ clock cycle when operating in SDR mode. In DDR mode, the output data can be shifted by a ½ system clock cycle to relax hold constraints. An additional fine-grain delay can be added to the timing of the sampling clock by enabling the delay block dedicated to QUADSPI.

Interrupts and DMA

Interrupt event	Description
Timeout	Set when timeout occurs.
Status match	Set in automatic Polling mode when the masked received data matches the corresponding bits in the match register.
FIFO threshold	Set in Indirect mode when the FIFO threshold has been reached.
Transfer complete	Set in Indirect mode when the programmed number of data has been transferred or in any mode when the transfer has been aborted.
Transfer error	Set in Indirect mode when an Invalid address is being accessed.

- DMA requests can be generated in Indirect mode when FIFO threshold is reached.

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The Quad-SPI memory interface has 5 interrupt sources: Timeout, Status Match when the masked received data matches the corresponding bits in the match register in Automatic Polling mode, FIFO Threshold, Transfer Complete and Transfer Error.
DMA requests can be generated in Indirect mode when the FIFO threshold is reached.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop + LP-Stop	Frozen. Peripheral registers content is kept.
LPLV-Stop	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

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The Quad-SPI memory interface is active in Run and Sleep modes. A Quad-SPI interrupt can cause the device to exit Sleep mode. In Stop mode, the Quad-SPI memory interface is frozen and its registers content is kept. In Standby mode, the Quad-SPI is powered-down and it must be reinitialized afterwards.

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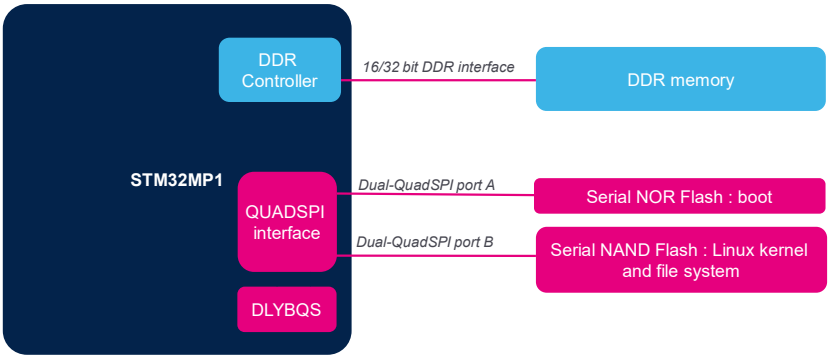
Application example

- External Quad-SPI is used in dual-Flash mode :
  - Serial NOR for First Stage Boot Loader (FSBL)
  - Serial NAND for second stage of boot (loading kernel and file system), and mass-storage



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The Quad-SPI interface of the STM32MP1 microprocessors is one of the supported boot source. It can be used in a dual-Quad configuration where one port is hooked on a serial NOR flash memory for the initial steps of the boot sequence, and the second port is connected to a serial NAND flash memory which embeds the Linux kernel and the file system, and hence can be used as a mass storage by the application. Because of the high speed supported by the interface and the very low pin count, such set-up offers highly optimized system integration and cost-efficient solution.

Related peripherals

- Refer to these trainings related to this peripheral:
  - RCC (Quad-SPI clock control, Quad-SPI enable/reset)
  - Interrupts (Quad-SPI interrupt mapping)
  - DMA and MDMA (Quad-SPI data transfer)
  - GPIO (Quad-SPI input/output pins)

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You can refer to the training slides related to the RCC, interrupts, DMA and GPIOs for additional information.

Thank you

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