Hello, and welcome to this presentation of the STM32H5 general-purpose IO interface. It covers the general-purpose input and output interface, and how it allows connectivity to the environment around the microcontroller.

GPIOs

- All GPIO features from legacy products are supported
- Up to 140 GPIOs on STM32H56x/57x and up to 49 GPIOs on STM32H503
  - With max frequency up to 200 MHz
- USB function with dedicated supply pin
  - Available on STM32H56x/57x devices, for packages starting from 100 pin
- With GPIOs on the dedicated VDDIO2 supply:

Product	Number of I/Os on VDDIO2	List of I/Os on VDDIO2
STM32H56x/573	10 (1)	(PD6, PD7, PG9:14, PB8, PB9)
STM32H503xx	9 (2)	(PA8, PA9, PA15, PB3:8)

(1) VDDIO2 pin available on packages starting from 144 pin
(2) VDDIO2 pin only available on WLCSP25

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All features of the legacy GPIO module are supported by the STM32H5.
The number of GPIOs depends on the package, 140 IO pads for the UFBGA176.
The maximum frequency for GPIOs is 200 MHz.
VDDUSB is the external independent power supply for USB transceivers.
VDDUSB voltage level is independent from the VDD voltage and must preferably be connected to VDD when the USB is not used.
This dedicated power supply is present only on packages having more than 100 pins.
VDDIO2 is the external power supply for up to 10 I/Os on STM32H5.

The VDDIO2 voltage level is independent of the VDD voltage and must preferably be connected to VDD when it is not needed.

High Speed Low Voltage (HSLV)

- Some I/Os support very high-speed mode thanks to new HSLV control bits in the GPIOx_HSLVR registers
  - Only I/Os with "_h" option support HSLV mode (refer to the I/O structure in the datasheet)
- The speed is improved by setting HSLV = 1 when VDDIOx < 2.7V
- Caution! HSLV must not be set if VDDIO > 2.7V (destructive !!…)
  - 2 option bytes forbid write access to the HSLV control bits and must be configured if needed:
    - IO_VDD_HSLV and IO_VDDIO2_HSLV
- Caution! Unless all I/Os of a communication peripheral support HSLV mode, this mode must not be set to avoid bad timing side effects

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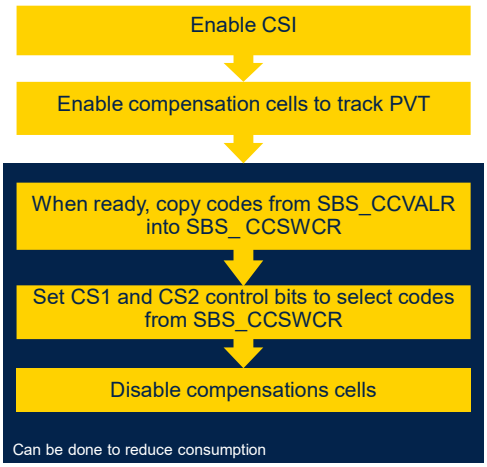
Some I/Os have the capability to increase their maximum speed at low voltage when configured in High Speed Low Voltage (HSLV) mode. They are identified by the suffix _h in the data sheet.
The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).
Caution: The I/O HSLV configuration bit must not be set if the I/O supply (VDD or VDDIO2) is above 2.7 V.
Setting it while the voltage is higher than 2.7 V can damage the device.
The I/O HSLV bit can be only set when the corresponding option bit is activated: IO_VDD_HSLV or IO_VDDIO2_HSLV depending on the I/O supply.

There is no hardware protection associated to this feature so it is recommended to use it only as a static configuration for fixed I/O supply.
High Speed Low Voltage should be disabled if all I/Os connected to a particular peripheral do not support this capability.

I/O compensation cell

- I/O commutation slew rate (tfall / trise) can be adapted by software depending on Process, Voltage and Temperatures conditions, in order to reduce the I/O noise on the power supply
- Two compensation cells:
  - one for I/Os supplied by VDD
  - one for I/Os supplied by VDDIO2
- Compensation cells can be used only when 1.6V ≤ VDDIOx ≤ 3.6 V
  - Enabled in the I/Os electrical characteristics



Note: I/O cempensation cell requires CSI to be enabled

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The I/O commutation slew rate, affecting rise and fall times, can be adapted by software depending on Process, Voltage and Temperatures conditions, in order to reduce the I/O noise on the power supply.
The compensation cell can be used only when VDDIOx is in the range 1.6 V to 3.6 V.
Two compensation cells are embedded, one for the I/Os supplied by VDD and one for the I/Os supplied by VDDIO2.
The I/O compensation cell generates an 8-bit value for the I/O buffer (4 bits for N-MOS and 4 bits for P-MOS), that depends on process, voltage, temperature (or PVT) operating conditions.
These bits are used to control the current slew-rate and

output impedance in the I/O buffer.
By default, the compensation cells are disabled, and a fixed code is applied to all I/Os.
The following sequence should be implemented to enable the compensation cells:
1- The CSI oscillator is used by the compensation cells and must be enabled
2- Enable the compensation cells in the SBS compensation cell control/status register
3- When enabled, the compensation cell tracks the PVT, and the 8-bit code is available in SBS_CCVR once the ready bit is set.
4- If the Code Selection bit is cleared, the I/O receives the code from SBS_CCVALR, resulting from the compensation cell.
To reduce the power consumption, it is recommended to copy the code from SBS_CCVALR to SBS_CCSWCR. After the result is ready, set the Code Selection bit and disable the compensation cell.
When the Code Selection bit is set, VDD I/O codes are received from the SBS compensation cell code register and not from the cell, which reduces the consumption.

I/O target spec with: VDD ≥ 2.7V

HSLV OFF	
OSPEED[1:0]	All I/Os
00 – low speed	16 MHz with 10 pF
01 – medium speed	60 MHz with 10 pF
10 – high speed	133 MHz with 10 pF
11 – very high speed	200 MHz with 10 pF

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The following slides indicate how to select the OSPEED value in the GPIO port output speed register according to the following parameters:

- VDDIO power supply range
- High speed Low voltage mode enabled or disabled.

For each OSPEED value, the maximum frequency also depends on the capacitive load.

Here VDD being larger than 2.7V, HSLV is necessarily off.

I/O target spec with: 1.71V < VDD < 2 V

HSLV ON	
OSPEED[1:0]	All I/Os
00 – low speed	16 MHz with 10 pF
01 – medium speed	60 MHz with 10 pF
10 – high speed	140 MHz with 10 pF
11 – very high speed	200 MHz with 10 pF

HSLV OFF	
OSPEED[1:0]	All I/Os
00 – low speed	5 MHz with 10 pF
01 – medium speed	20 MHz with 10 pF
10 – high speed	50 MHz with 10 pF
11 – very high speed	80 MHz with 10 pF

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Let us continue with VDD in range 1.71V to 2V.
In the table on the left, HSLV is ON, while in the table on the right HSLV is OFF.
For a given OSPEED setting, the maximum frequency is higher when HSLV is enabled.

I/O target spec with: 1.08 V≤ VDDIO2 ≤1.32 V

HSLV ON	
OSPEED[1:0]	All I/Os
00 – low speed	5 MHz with 10 pF
01 – medium speed	25 MHz with 10 pF
10 – high speed	55 MHz with 10 pF
11 – very high speed	77 MHz with 10 pF

HSLV OFF	
OSPEED[1:0]	All I/Os
00 – low speed	1 MHz with 10 pF
01 – medium speed	5 MHz with 10 pF
10 – high speed	10 MHz with 10 pF
11 – very high speed	30 MHz with 10 pF

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Let us continue with VDD in range 1.08V to 1.32V.
Same conclusion: the maximum frequency is higher when HSLV is enabled.

GPIO TrustZone Security

- Each I/O pin of the GPIO port can be individually configured as secure/non-secure in the GPIOx_SECCFGR register
  - Secure I/O access from non-secure is RAZ/WI

Security configuration		Alternate function
Peripheral	I/O pin	
Secure	Secure*	OK
Non-secure*		
Secure	Non-secure	Zero
Non-secure		OK

Security configuration		Analog value
Analog peripheral	Allocated I/O pin with analog switch	
Secure	Secure	OK
Non-secure		zero
Secure	Non-secure	zero
Non-secure		OK

*Default configuration after reset

Note: No TrustZone for STM32H503 devices

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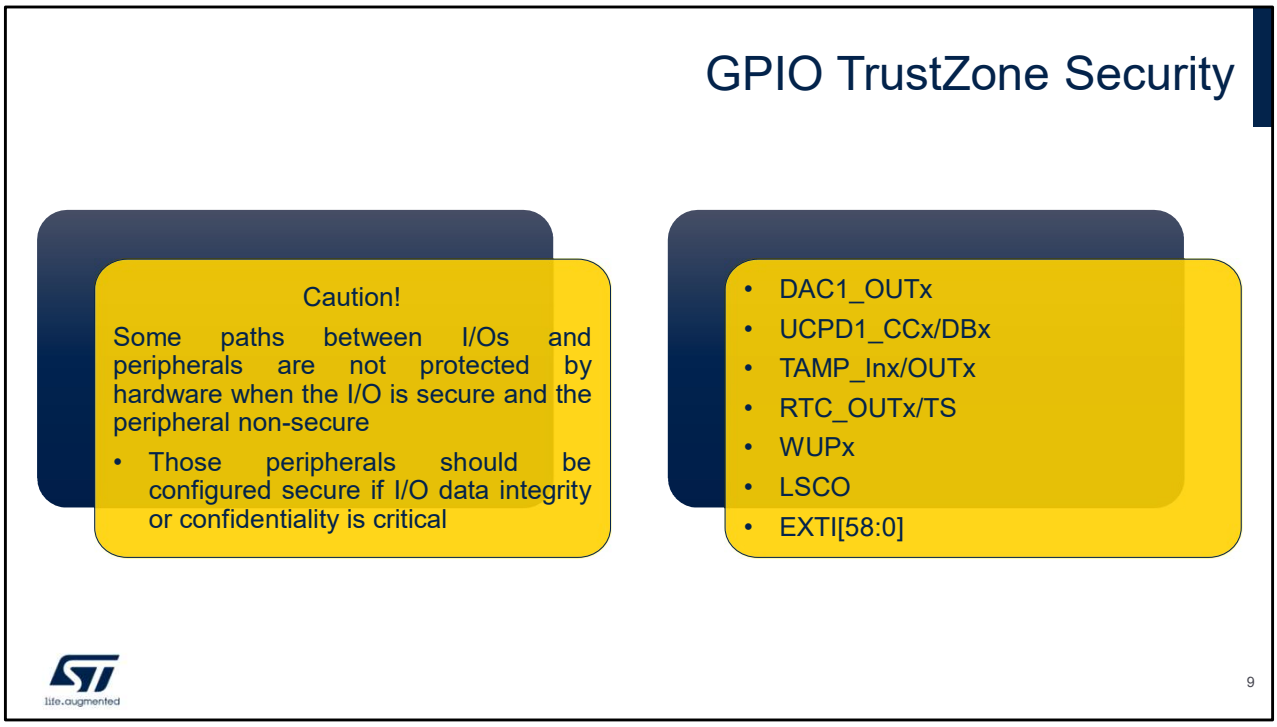
When the TrustZone is active, each I/O pin of the GPIO port can be individually configured as secure through the GPIOx_SECCFGR register.
When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, and I/O data are secure against a non-secure access.
In the case of a non-secure access, these fields are read as zero, and writes are ignored.
I/Os with peripheral functions are also conditioned by the peripheral security configuration.
In peripherals for which the I/O pin selection is done through alternate functions registers: if the peripheral is configured as secure, it cannot be connected to a non-

secure I/O pin.
If this is not respected, the input data to the secure peripheral is forced to 0 and the output pin value is forced to 0, thus avoiding any secure information leak through non-secure I/Os.
For I/Os with analog switches, directly controlled by peripherals, such as the ADC for instance: if the I/O is secure, the I/O analog switch cannot be controlled by a non-secure peripheral.
If this is not respected, the switch remains open. This prevents the redirection of secure data to a non-secure peripheral or I/O through the analog path.



The pin function is generally controlled by the GPIO Alternate Function Registers.
However, the so-called additional functions are directly selected and enabled through peripheral registers, not involving the GPIO module.
Some of the paths between these I/Os additional functions and peripherals are not blocked if the I/O is secure and the peripheral is non-secure.
Therefore it is recommended to configure those peripherals as secure even when not used by the application.
The list of these additional functions is indicated on the right.

GPIO Privileged/Unprivileged mode

- All GPIO registers can be read and written by privileged and unprivileged accesses, whatever the security state: secure or non-secure

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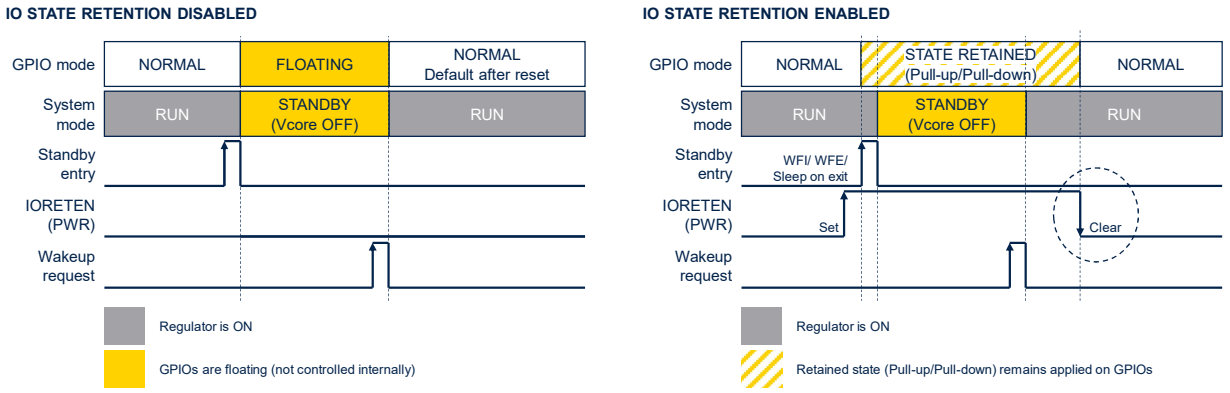
The GPIO module filters out accesses in its memory-mapped registers according to the security level, but not the privilege level.

GPIO output state retention in Standby mode



- GPIO output state can be retained in Standby mode, allowing the MCU to keep sensitive control signals set for an external devices
  - For example, during standby, STM32H5 can keep chip select or low-power mode control signal set for external devices
- Two bits are available to enable retention : 1 bit for IOs except JTAG & 1 bit for JTAG interface

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GPIO output state can be retained in Standby mode, allowing the microcontroller to keep sensitive control signal set for external devices, for example chip select or low-power mode control signals connected to external devices.
If the IORETEN bit in the PWR_IORETR register is set, the I/Os state is sampled during standby entry.
The state of I/Os is applied to the pin via pull-up and pull-down resistors.
The pull-up and pull-down resistors remains applied after Standby wakeup until the IORETEN bit in the PWR_IORETR register is cleared by software.

Low-power modes

Mode	I/O state
RUN, SLEEP, STOP	Active
STANDBY	I/Os can be configured to be retained (output state) or to remain floating in Standby mode
RESET	During and just after reset, the alternate functions are not active and most of the I/O ports are configured in analog mode In case of RESET (except POR reset) upon a wakeup from standby with I/Os state retention enabled, the IOs need to be configured and then released from retention state

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GPIOs are active in run, sleep, and stop modes.
In standby mode, the state can be retained or floating, as explained in the previous slide.
When the microcontroller is under reset, most of I/O pins are forced into an analog input mode.
In case of RESET, except Power-On Reset, upon a wakeup from standby with I/Os state retention enabled, the IOs need to be configured and then released from retention state.

Thank you

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Thank you for having attended this presentation on STM32H5 GPIO.
Refer also to the following presentations for more information if needed:

- Extended interrupts and event controller (EXTI)
- Power Management (PWR).