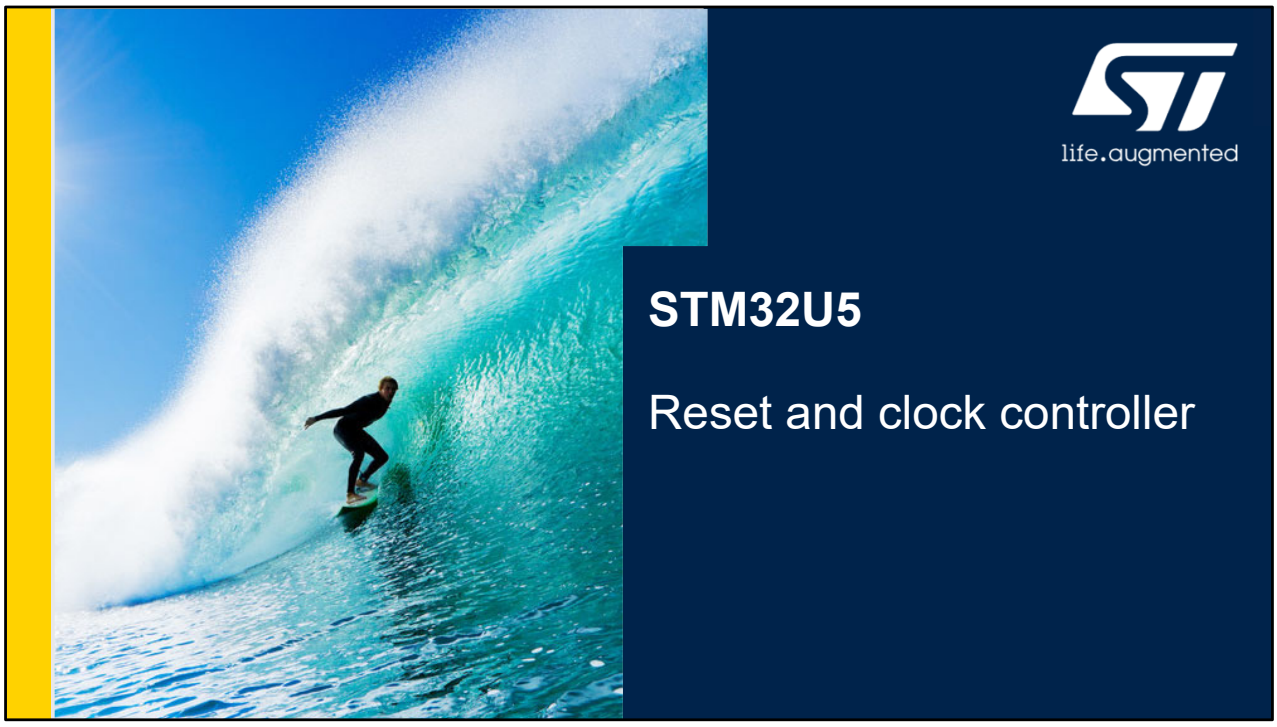

Hello, and welcome to this presentation of the STM32U5 reset and clock controller (or RCC).

Key features

Six internal clock sources

- High-speed internal 16 MHz RC oscillator (HSI16)
- Multi-speed internal RC oscillators for system clock and for peripherals kernel clock (MSIS and MSIK)
- Low-speed internal 32 kHz RC oscillator (LSI)
- High-speed internal 48 MHz RC oscillator (HSI48)
- Secure high-speed 48 MHz RC oscillator (SHSI) dedicated to SAES

Two external oscillators

- High-speed external 4 to 50 MHz oscillator (HSE) with clock security system
- Low-speed external 32.768 kHz oscillator (LSE) with clock security system

Three PLL, each with 3 independent outputs

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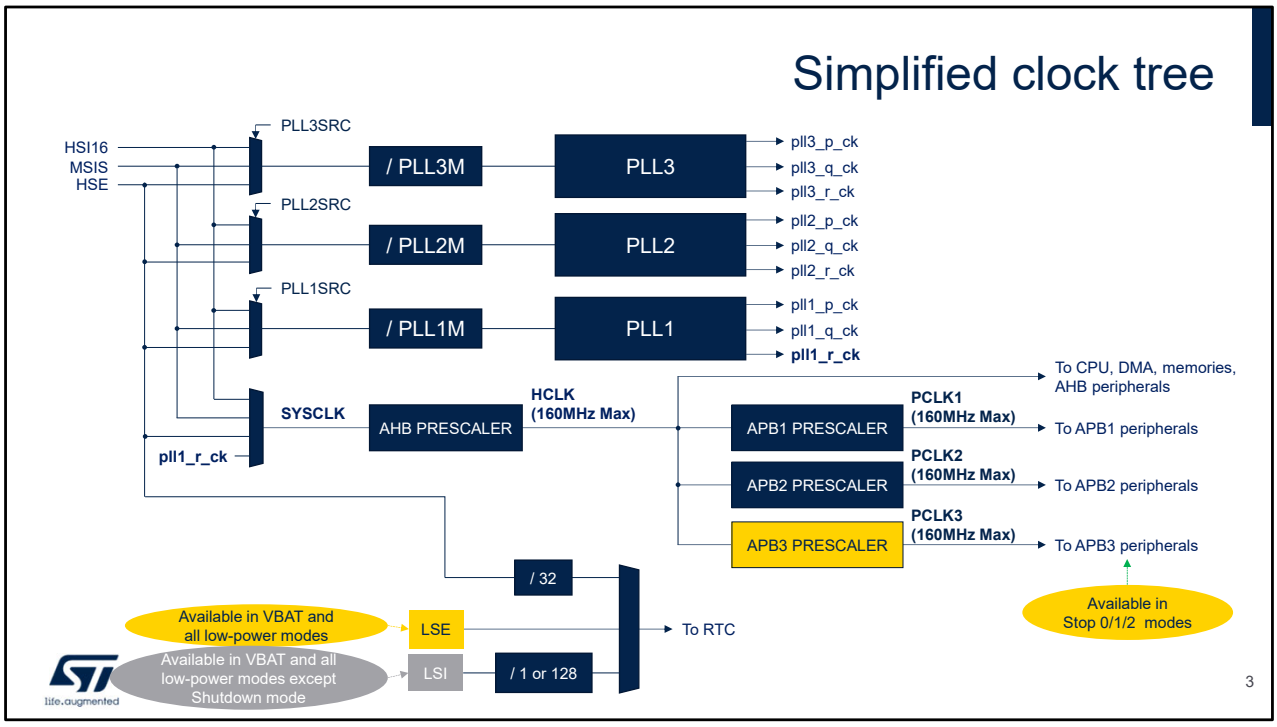
The STM32U5 reset and clock controller manages the system and peripheral clocks.
STM32U5 microcontrollers embed 6 internal oscillators, 2 oscillators for an external crystal or resonator, and three phase-locked loops (or PLLs).
Many peripherals have their own clock, independent of the system clock.
The RCC also manages the various resets present in the device.
The STM32U5 RCC provides high flexibility in the choice of clock sources, allowing the system designer to meet both power consumption and accuracy requirements.
The numerous independent peripheral clocks allow a designer to adjust the system power consumption without

impacting the communication baud rates, and also to keep some peripherals active in low-power modes.
Some peripherals support autonomous mode. They are able to generate a kernel clock request and an AHB/APB bus clock request when needed, in order to operate and update their status register even in Stop mode.



The system clock can be derived from the high-speed internal 16 MHz RC oscillator (HSI16), from the high-speed external 4 to 50 MHz oscillator (HSE), from the multiple-speed oscillator system (MSIS) or from the pll1_r_ck output of the PLL1.

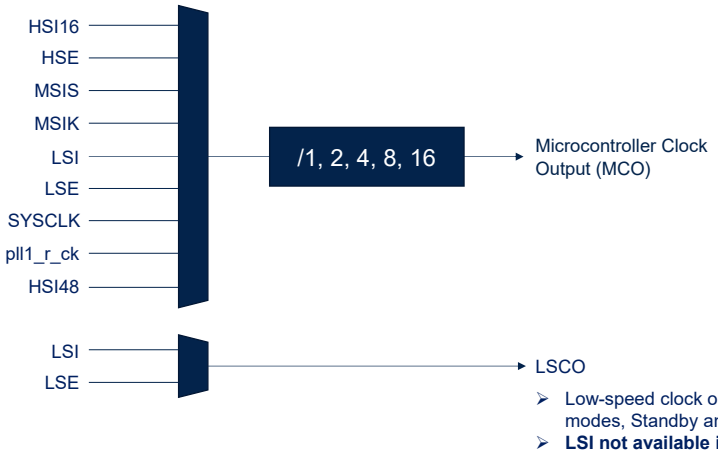
The AHB clock, called HCLK, is derived by dividing the system clock by a programmable prescaler.

The APB clocks, called PCLK1, PCLK2 and PCLK3, are generated by dividing the AHB clock by programmable prescalers.

The RTC clock is generated by the low-speed external 32.768 kHz oscillator (LSE), the low-speed internal 32 kHz RC oscillator (LSI), or the HSE divided by 32. This selection cannot be modified without resetting the Backup

domain.
The LSE can remain enabled in all low-power modes and in VBAT mode.
The LSI can remain enabled in all modes including VBAT but except Shutdown modes.

Clock-out capability



- Low-speed clock output (LSCO) is available in all Stop modes, Standby and Shutdown modes
- **LSI not available in Shutdown mode**

- The LSI clock frequency is either 32 kHz or 250 Hz depending on the LSIPREDIV bit in the RCC backup domain control register (RCC_BDCR)

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Various clocks can be output on I/O pads.
The Microcontroller Clock Output feature enables the external output of one of these nine clocks: HSI16, HSE, MSI System, MSI Kernel, LSI, LSE, SYSCLK, pll1_r_ck and HSI48.
The low-speed clock output feature enables the external output of the LSI or LSE clock, which is driven onto the Low-speed output clock or LSCO pad. This output remains available in all Stop modes, Standby and Shutdown modes, but not in VBAT mode.
Note that LSI is not available in shutdown mode and that the LSI frequency is selectable through a control register: either 32 Kilohertz or 250 hertz. Choosing 250 Hertz allows a lower consumption:

HSE, HSI16, HSI48, SHSI, LSI

- **HSE** from 4 to 50 MHz
  CSS with automatic switch to HSI
- **HSI16**: 16 MHz internal RC with user trim
  Can be used as a wakeup from Stop clock source, and during Stop 0,1,2 modes (RCC_CFGR1.STOPWUCK=1)
- **HSI48**: 48 MHz oscillator used for USB (OTG_FS with CRS), SDMMC and RNG
  Optional division by 2 for RNG when used in Range 4
- **SHSI** is a SAES dedicated kernel clock, 48 MHz +/- 15% jitter
- **LSI**: 32kHz or 250kHz, selected by RCC_BDCR LSIPREDIV
  Available in all power modes except Shutdown mode, and in VBAT mode

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This slide describes the features of five oscillators.
- The high-speed external oscillator provides a safe crystal system clock.
The HSE supports a 4 to 50 MHz external crystal or ceramic resonator, as well as an external source in bypass mode.
A clock security system automatically detects an HSE failure. In this case a Non-Maskable Interrupt is generated, and a break input can be sent to the timers in order to put critical applications such as motor control in a safe state.
When an HSE failure is detected, the system clock is automatically switched to an internal oscillator: either HSI16 or MSIS, so that the application software does not stop in the case of crystal failure.

- The high-speed internal oscillator is a 16 MHz RC oscillator which provides 1% accuracy and fast wakeup times. The HSI16 is trimmed during production testing, and can also be user-trimmed to take into account temperature and voltage variations.
The HSI16 can be automatically awoken when exiting any Stop mode in order to make it available for peripherals when it is not used as the system clock.
- The HSI48 is generated from an internal 48-MHz RC oscillator.
48 MHz is a canonical frequency for a USB module.
HSI48 can also be used as the reference clock for the RNG and SDMMC modules.
The HSI48 is associated with a special Clock Recovery System (CRC) circuitry that dynamically adjusts the frequency according to the receipt of a USB Start of Frame packet or the LSE or an external signal.
- The secure high-speed internal 48 MHz SHSI oscillator drives the Secure AES coprocessor, or SAES.
- The Low Speed Internal (LSI) oscillator is the unique clock of the independent watchdog and can be the clock of the RTC. It can be kept running in all Stop and Standby modes. The clock frequency is either 32 KHz or 250 Hz. When using the independent watchdog, 32-KHz operation is selected and forced on.

HSI16 target electrical characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency	VDD=3 V, TA=30 °C	15.92	16	16.08	MHz
	TJ = –10 °C to 100 °C, 1.58 ≤ VDD ≤ 3.6 V	15.84	-	16.16	
	TJ = –40 °C to 130 °C, 1.58 ≤ VDD ≤ 3.6 V	15.65		16.25	
User Trimming step		18	29	40	KHz
Startup time	-		2.5	3.6	µs
Stabilization time	At 1% of target frequency		4	6	
Power consumption	-		150	210	µA

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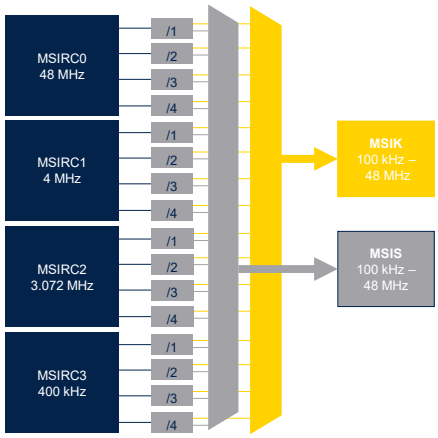
This table summarizes the features of the HSI16 oscillator.
The values come from the STM32U585xx data sheet DS13086 Revision 0.3.
Minimum, typical and maximum frequency are indicated for operation at 30 degree Celsius as well as the minus 10 to plus 100 degree Celsius temperature range.
The HSI16 frequency can be trimmed in the application with a typical step of 29 kilohertz.
Startup time and stabilization times are also indicated.
Note that the HSI16 has a faster startup time than the HSE crystal oscillator.
Finally the table provides the typical and maximum consumption of the HSI16, knowing that the HSI16 can be switched off using the HSION bit.

MSI (MSIK and MSIS) - overview

- 16 frequencies from 100 kHz to 48 MHz
  - The MSI is made up of four RC oscillators
  - Each MSIRCx feeds a prescaler providing a division by 1, 2, 3 or 4
  - 3.072MHz RC for audio frequencies
  - Each MSIRCx has user trim code
- Two output clocks are generated:
  - **MSIS**, that can be selected as the system clock
  - **MSIK**, that can be selected by some peripherals as the kernel clock
  - MSIS and MSIK frequencies are independently selected by RCC_ICSCR1[MSISRANGE,MSIKRANGE]



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The STM32U5 supports two Multiple-Speed Internal oscillators: the MSI System or MSIS and the MSI Kernel or MSIK. The MSIS is one of the oscillators that can be selected as the input clock of the PLLs.
The MSIK generates a clock that is independent of the system clock and therefore convenient for peripherals that require a fixed clock while the system clock may vary over time due to dynamic voltage and frequency scaling.
The MSI is made up of four internal RC oscillators: MSIRC0 at 48 MHz, MSIRC1 at 4 MHz, MSIRC2 at 3.072 MHz and MSIRC3 at 400 kHz. Each oscillator feeds a prescaler providing a division by 1, 2, 3 or 4.
MSIS and MSIK frequencies are independently selected by programming the control register RCC_ICSCR1.

In addition, when used in PLL-mode with the LSE, the MSI provides a very accurate clock source that can be used by the OTG_FS peripheral,

MSI (MSIK and MSIS) vs. MCU modes

- System clock after restart from Reset, wakeup from Standby/Shutdown modes
  - At Reset or when exiting Shutdown mode, MSIS and MSIK = 4 MHz
  - The MSIS and MSIK frequency at wakeup from Standby mode can be selected by software, from 1 to 4 MHz
- MSI up to 24 MHz can be used as wakeup from Stop system clock and during Stop 0, 1, 2 modes (RCC_CFGR1[STOPWUCK]=0)
- MSI-mode:
  - the MSI is in sampled mode in Range 4 and low-power modes when RCC_ICSCR1[MSIBIAS]=1 (lower accuracy/lower power)
  - The MSI is in continuous mode
    - in Range 1,2,3
    - In Range 4 and low-power modes when RCC_ICSCR1[MSIBIAS]=0

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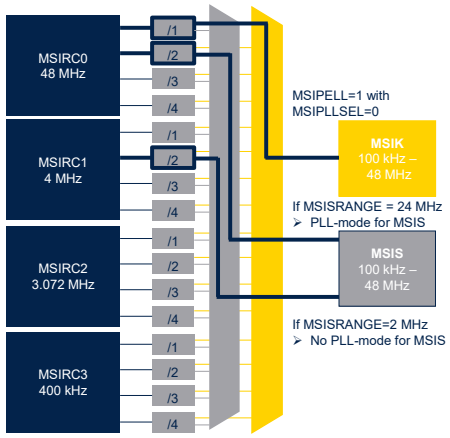
The MSIS clock is used as the system clock after restart from Reset, wakeup from Standby and Shutdown low-power modes.
After restart from Reset or when exiting Shutdown mode, the MSIS and MSIK frequencies are set to their default value 4 MHz.
When exiting the standby mode, the MSIS and MSIK frequency range is from 1 to 4 MHz.
When exiting Stop 0, 1 and 2 modes by issuing an interrupt or a wakeup event, HSI16 is selected as the system clock if the bit STOPWUCK is set.
MSIS is selected as system clock if STOPWUCK is cleared.
The wakeup time is shorter when HSI16 is selected as the

wakeup system clock.
The MSI selection allows a wakeup at a higher frequency, up to 24 MHz.
The last bullet describes the features of the MSI-mode. The alternate mode is called PLL-mode. It will be described in the next slides.
MSI-mode has two sub-modes: sampled or continuous.
The MSI is in continuous mode when the internal regulator is in voltage range 1, 2 or 3.
The MSI is in sampling mode when the regulator is in voltage range 4, or when the device is in Stop 1 or Stop 2 modes.
By default, the MSI is in continuous mode in order to maintain the output clocks accuracy.
Setting the MSIBIAS bit reduces the MSI consumption in range 4 but decreases its accuracy.
In range 4, when this bit is set, the sampled mode is enabled.

MSI (MSIK and MSIS) – PLL mode

- MSI-PLL mode (RCC_CR.MSIPLLEN=1): either MSIK (MSIPLLSEL=0) or MSIS (MSIPLLSEL=1) can be automatically calibrated with LSE
  - Only one of the 4 MSIRCx sources is calibrated
    - Both MSIK and MSIS are calibrated if sharing the same source
- Stabilization time:
  - RCC_CR.MSIPLLFAST=0
    - ➢ Stabilization time after setting MSIPLLEN=1 even when LSE is already enabled
  - RCC_CR.MSIPLLFAST=1
    - ➢ Almost no stabilization time after setting MSIPLLEN=1 when LSE is already enabled, and stabilization was previously done (useful when exiting Stop mode), but extra consumption



When a 32.768 kHz external oscillator is present in the application, it is possible to configure either the MSIS or the MSIK in PLL-mode.
In the case that MSIS and MSIK ranges are generated from the same MSIRC source, the PLL-mode is applied on both MSIS and MSIK.
When configured in PLL-mode, the MSIS or MSIK automatically calibrates itself thanks to the LSE. Consequently, the MSI accuracy is the LSE crystal accuracy.
At 48 MHz, the MSIK in PLL-mode can be used for the OTG_FS device, avoiding the need of an external high-speed crystal.
The figure on the right assumes that MSI-PLL mode is

enabled for MSIK and MSIS when the frequency is 24 MHz. In this case the MSIRC0 oscillator clock is calibrated.
The second frequency that can be selected for MSIS, 2 MHz, is provided by MSIRC1 and therefore PLL mode cannot be used.
The stabilization time of the MSI oscillators configured in PLL mode depends on the MSIPLLFAST bit.
When this bit is zero, 0.8 milliseconds is required, while when this bit is one, this time is reduced to 2 cycles when LSE is already enabled and stabilization was previously done.

MSI target electrical characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency	VDD=3 V, TA=30 °C	16 freq. from 98.3 kHz to 48 MHz			MHz
User Trimming step			0.3		%
Frequency drift over temperature vs. 30°C	Continuous mode	-4		2	%
	Sampled mode MSIBIAS=1			0.2	%
Frequency drift over VDD vs 3V	Continuous mode	-4		1	%
Frequency drift sampled mode	MSIBIAS=1 (range 4, LP modes)			0.2	%
Startup time	MSIRC0 48 MHz		13		cycles
	others		4		cycles
Stabilization time 1%	PLL-mode, MSIPLLFAST=0			0.8	ms
	PLL-mode, MSIPLLFAST=1	2			cycles

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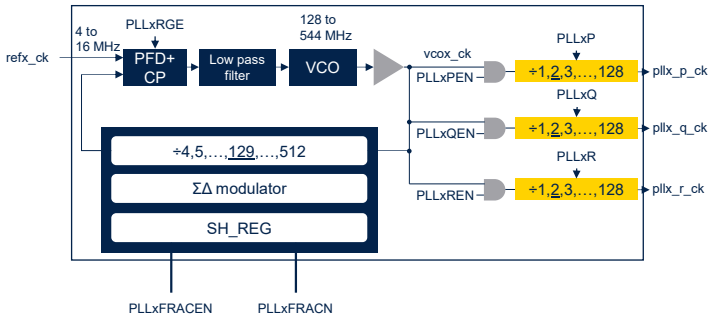
This table summarizes the features of the MSI oscillators. Minimum, typical and maximum frequency values are indicated for operation at 30 degrees Celsius.
The MSI frequency can be trimmed in the application with a typical step of 0.3% of the frequency.
The drift according to temperature and voltage variations are indicated. These variations can be monitored in order to dynamically update the calibration parameter.
Startup and stabilization times are also provided.

PLLs

- Three PLLs:
  - Main PLL for the CPU and certain peripherals
  - Two other PLLs for peripherals' kernel clock
- Input frequency from 4 to 16 MHz
- VCO from 128 to 544 MHz
- 13-bit fractional multiplication factor, programmable on the fly
- 3 outputs per PLL, with a VCO divider range from 1 to 128



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The three PLLs integrated in the RCC are completely independent
They have the same input stage: the input clock is either HSI16 or MSIS or HSE.
PLLs can be used to multiply the frequency of these reference clocks.
The PLL input frequency must be between 4 and 16 MHz and the frequency at the VCO must be between 128 and 544 MHz.
The value of the divider located after the clock multiplexer has to chosen accordingly. See the PLLxRGE parameter in the figure.
The PLLs are capable to working either in integer or Fractional mode, which is an important new feature of the

STM32U5.
The 13-bit sigma-delta (ΣΔ) modulator fine-tunes the VCO frequency in steps of 11 to 0.3 ppm .
The ΣΔ modulator can be updated on-the-fly, without generating frequency overshoots on PLL outputs.

CLOCK FREQUENCIES

Voltage range	SYSCLK	MSIK/MSIS	HSI16	HSI48	SHSI	HSE	PLL outputs (VCO max)
1	160 MHz	All ranges	Allowed	Allowed	Allowed	50 MHz	208 MHz* (128 to 544 MHz)
2	110 MHz	All ranges	Allowed	Allowed	Allowed	50 MHz	110 MHz (128 to 544 MHz)
3	55 MHz	All ranges	Allowed	Allowed	Allowed	50 MHz	55 MHz (128 to 330 MHz)
4	25 MHz	Up to 24 MHz	Allowed	Allowed (divided by 2)	Allowed (divided by 2)	24 MHz	Not allowed

* 200 MHz OCTOSPI kernel clock allowed

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This table indicates the maximum frequencies according to the voltage ranges.
In voltage range 1, the maximum performance is obtained: 160-MHz system clock, possibly 200-MHz for the OCTOSPI kernel clock.
In voltage range 2 and 3, the maximum system frequency is respectively 110 and 55 MHz.
In voltage range 4, the maximum frequency is 25 MHz and must be provided by an oscillator.
PLLs are disabled.

LSE

- LSE 32.768 kHz with 3 drive/power levels
- Available in all power modes and in VBAT mode
- By default LSE is only propagated to RTC/TAMP
  - Program RCC_BDCR[LSESYSEN]=1 if LSE is used by other peripherals (UART, peripheral trigger…) or by another RCC function (LSCO, MCO, MSI in PLL-mode)
  - LSE consumption increases when LSESYSEN=1

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The 32.768 kHz low-speed external oscillator can be used with an external quartz or resonator, or with an external clock source in bypass mode.
It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.
The oscillator driving capability is programmable. Three modes are available, from ultra-low power mode with a consumption of only 350 nanoamperes, to high-driving mode.
If the LSE is used by other peripherals or functions than RTC and TAMP, the LSESYSEN bit must be set .
The peripherals that can be clocked by the LSE are the USARTs, the low-power UART 1, the low-power timer 2,

the Cortex-M33 systick, the DAC1.

CSS on LSE

- Available in VBAT mode
- Detects clock missing or over frequency
- Detector + glitch filter consumption : 80 nA
- For revision C and later CSS detection signal can generate an interrupt with wake up from stop capability
- CSS detection signal is connected to a tamper

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A clock security system monitors for failure of the LSE oscillator. It detects a missing clock or overfrequency. The CSS on LSE works in all modes including VBAT. It is also functional during system reset, excluding power-on reset.

For revision C and later CSS detection signal can generate an interrupt with wake up from stop capability

The CSS on LSE failure is connected to a tamper event. In the case of a failure, the application can switch the RTC clock to the LSI. This is not automatic.

Peripheral clocks highlights

ADC1, ADC4 and DAC1 clocks share the same clock source to avoid VREF+ perturbation in case of simultaneous conversions

The OCTOSPI clock is allowed up to 200 MHz when the PLL is used

ICLK is the clock used by OTG_FS and SDMMC, and is selectable between HSI48, PLL or MSIK

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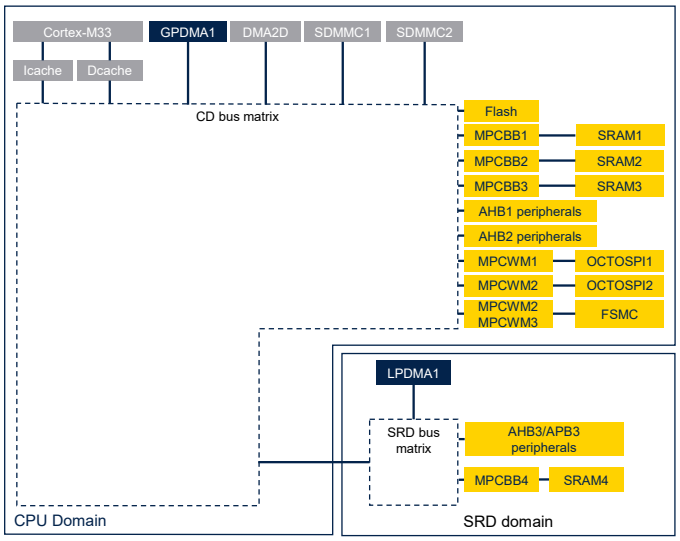
This slide highlights some interesting features of the STM32U5 clock architecture.
First, the ADC1, ADC4 and DAC1 modules share the same clock, which is the output of a multiplexer whose inputs are SYSCLK, HCLK, pll2_r_ck, HSE, HSI16 and MSIK. This shared clock scheme minimizes the VREF+ perturbations in the case of simultaneous conversions.
The OCTOSPIx kernel clock, can be up to 200 MHz when pll1_q_ck is used.
This clock is faster than the Cortex-M33 clock, in order to maintain a high performance when the core executes code from the external OCTOSPI memory.
ICLK is the clock of the USB OTG full speed module and one of the clocks that can be selected for the SD MMC

controllers, the other one being pll1_p_ck.
A multiplexer selects the source of ICLK: either MSIK, HSI48, pll1_q_ck or pll2_q_ck.

CPU domain (CD) and Smart run domain (SRD)

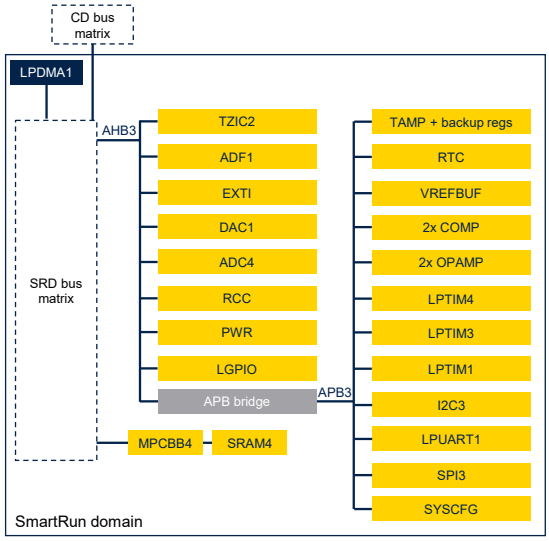


- Stop 0 & Stop 1:
  - CD & SRD fully powered
    - All autonomous peripherals are functional, thanks to GPDMA1 and LPDMA1
- Stop 2:
  - CD in retention (lower leakage mode)
    - No dynamic activity possible
  - SRD fully powered
    - SRD autonomous peripherals are functional thanks to LPDMA1

Some peripherals support autonomous mode. They remain active while the microcontroller is in a low power stop mode.
These peripherals generate a kernel clock request and an AHB/APB bus clock request when needed, in order to operate and update their status register even in Stop mode.
Depending on the peripheral configuration, either a DMA request or an interrupt can be associated to the peripheral event.
Upon an AHB or APB bus clock request from an autonomous peripheral, either the MSI or HSI16 oscillator is woken up,
If the autonomous peripheral is configured with DMA

requests enabled, a data transfer is performed thanks to the AHB/APB clock.
The bus clocks as well as the oscillator (HSI16 or MSI) are automatically switched off as soon as the transfer is finished, if no other peripheral requests it.
The device automatically goes back in Stop mode.
The autonomous peripherals mapped on AHB1, AHB2, APB1 and APB2, belong to the CPU domain, also called CD, and are autonomous in Stop 0 and Stop 1 only with the GPDMA1 and SRAM1, SRAM2, SRAM3 or SRAM4.
The autonomous peripherals mapped on AHB3 or APB3 belong to the SmartRun domain, also called SRD, and are autonomous in Stop 0, Stop 1 and Stop 2 with the LPDMA1 and SRAM4.

Smart Run Domain



This figure indicates which memories, masters and peripherals belong to the SmartRun domain, which remains fully functional in stop 2 low power mode.
The SRD includes peripherals connected to AHB3 and APB3.
The masters are the CD bus matrix, which is idle in stop 2 mode and the low power DMA1, that can be used to transfer data from peripheral to SRAM4 or from SRAM4 to peripheral, without needing to wake up the CPU domain.
Note that the presentation on power management describes various scenarios involving DMA and peripherals working in autonomous mode.

Thank you

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For more details, please refer to application note AN2867, an oscillator design guide for STM8S, STM8A and STM32 microcontrollers and application note AN5676 which explains how to calibrate STM32U5 internal RC oscillators