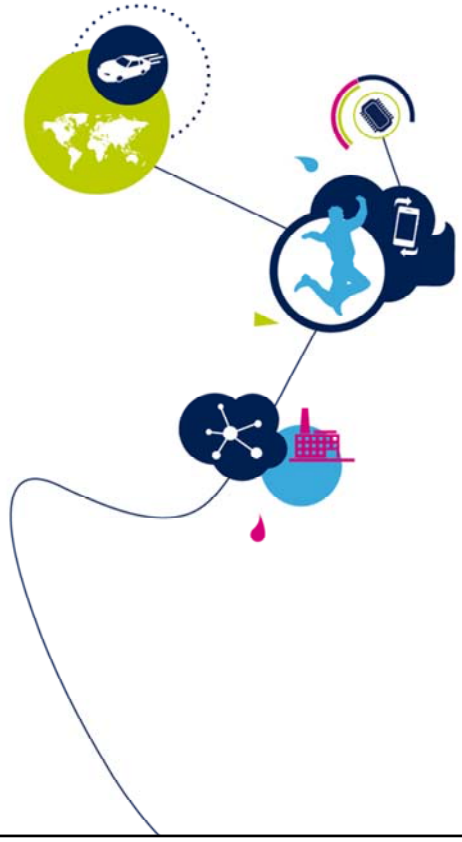
STM32L5 - DFSDM

Digital filter for Sigma-Delta modulators interface
Revision 1.0



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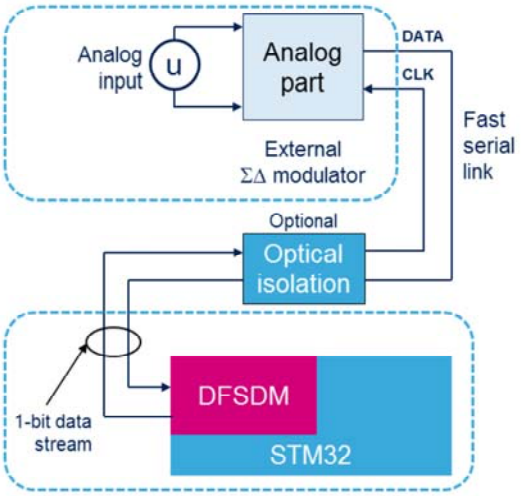
Hello, and welcome to this presentation of the STM32 Digital Filter for Sigma-Delta modulators interface.
It covers the features of this interface, which behaves like an analog-to-digital converter (ADC) with an external analog part and configurable speed versus resolution ratio.

DFSDM: introduction and typical usage

Behaves like ADC with scalable speed/resolution and external analog front-end



ADC in spread architecture

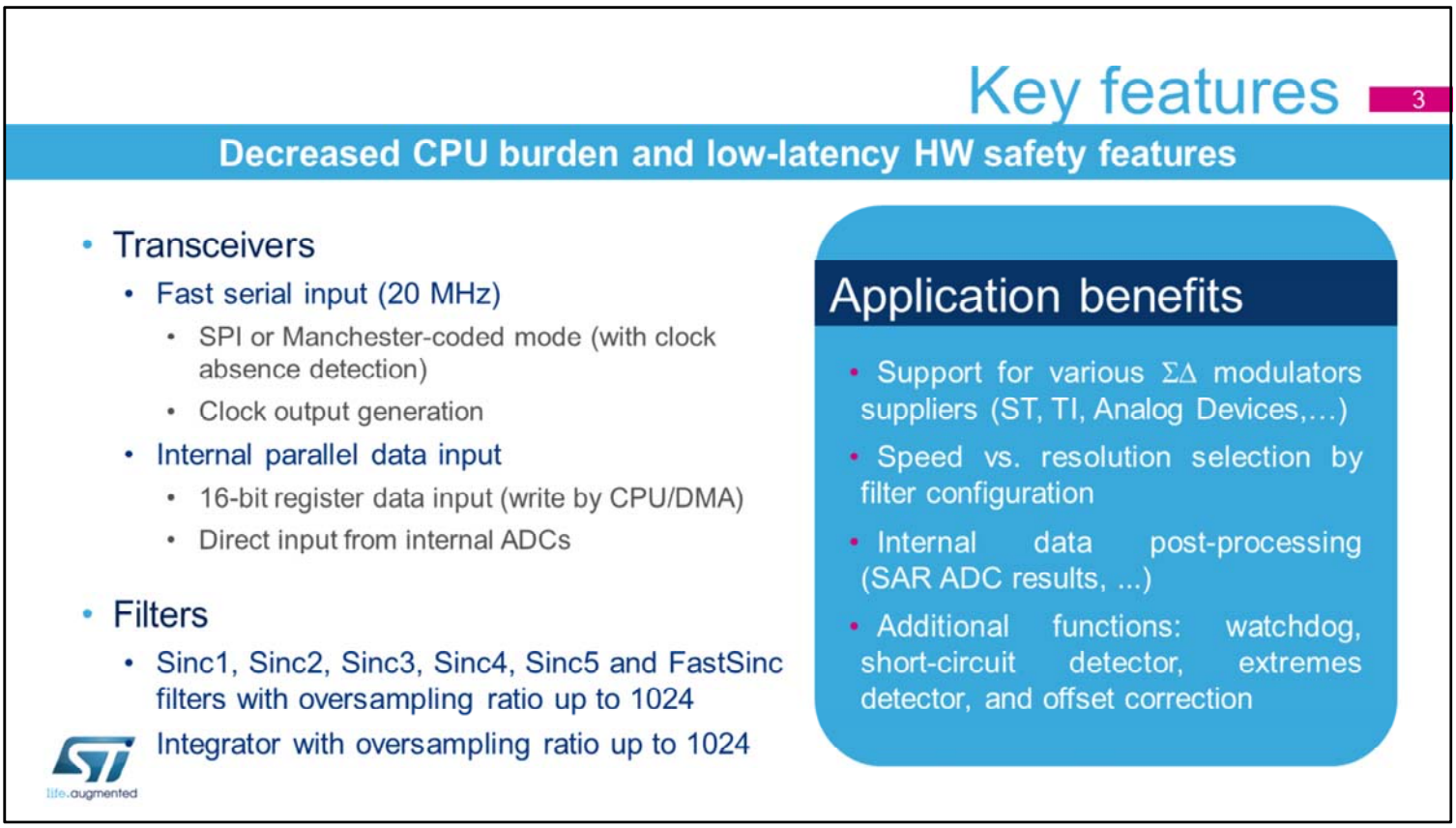
- Split of analog and digital parts:
  - Benefit from external analog selection
  - Benefit from internal digital features (DFSDM)

Application benefits

- External analog part: selection according to needs: precision, less noise, extra fast, galvanic isolation, linearity, cheap, high voltage-side operation
- Digital part: serial line interface (1 or 2 wires), scalable speed vs. resolution (up to 24 bits), full features like ADC
- Examples: electricity meter, motor control, medical applications, MEMS microphone audio, etc.

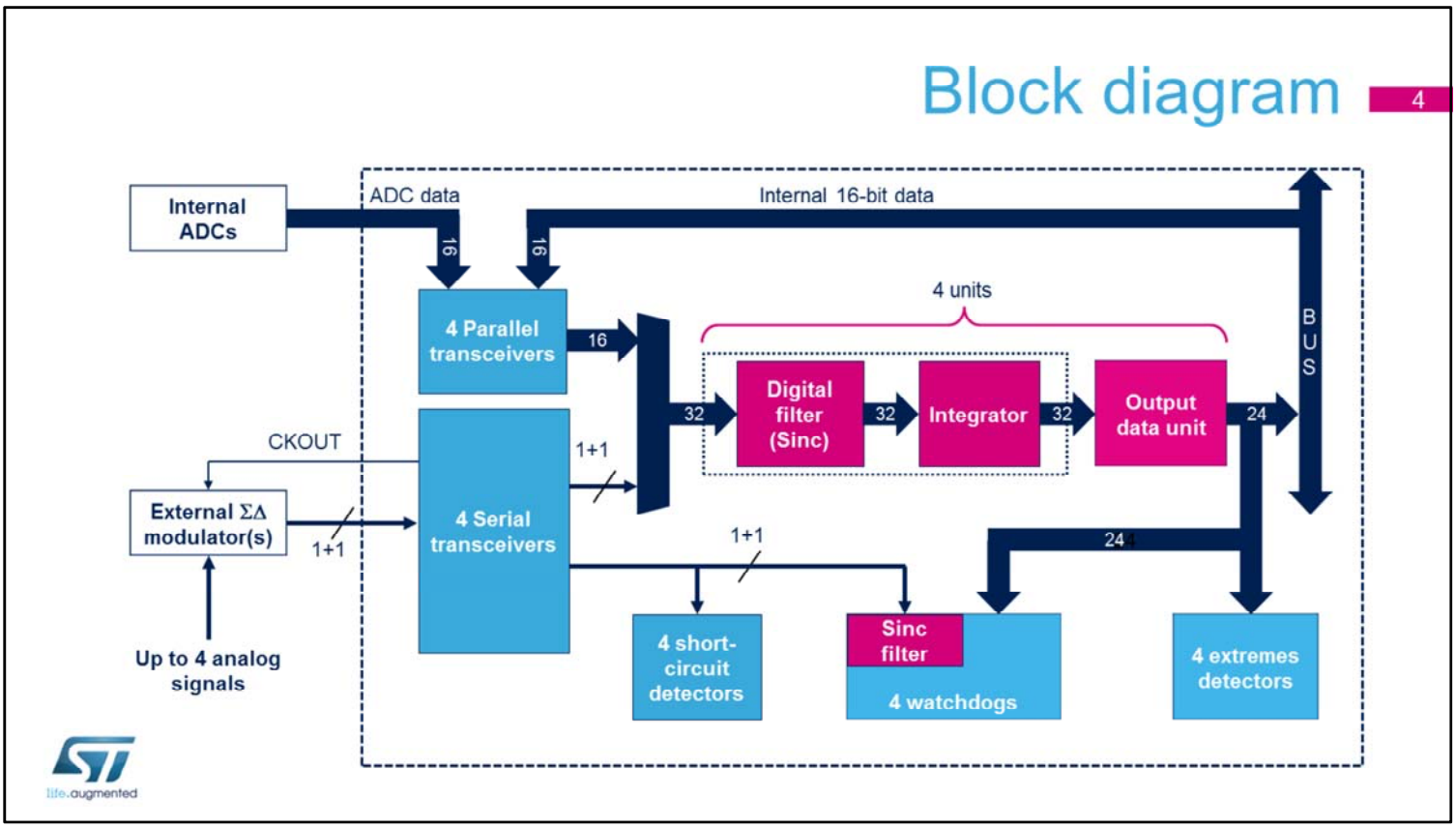
The DFSDM behaves like a standard ADC with the analog part outside the microcontroller.
The DFSDM represents the digital part which is connected to the analog part through a fast serial interface. The external analog part is usually a Sigma Delta modulator offered by a wide range of vendors. This feature offers the possibility to choose a specific analog part according to the user needs, like galvanic isolation for motor control or metering applications, with a low noise and high precision analog part for sensor data acquisition applications or an inexpensive analog part for low cost applications. Finally the analog part provides digitized data for the DFSDM.
The digital part (represented by the DFSDM peripheral) processes digital signals from external data. Therefore it offers a scalable ratio solution between speed and resolution but also an additional functionality integrated

in standard built-in ADC (like analog watchdogs, injected and regular conversions, flexible triggering system, break signal generation, extreme detector).
Digital MEMS microphones providing a Pulse Density Modulation (PDM) output data format can be directly connected to the DFSDM which can process directly the audio signal.
The DFSDM is able to process the external serial data and also the internal parallel 16-bit data transfer provided by the CPU or the direct memory access controller (DMA) from memory.



Transceivers provide the serial connection to the external sigma-delta modulator.
They support serial connections with configurable protocols (SPI or Manchester-coded) and configurable parameters.
Transceivers also support internal 16-bit parallel data inputs which are written to the DFSDM input data registers by the internal ADCs or the CPU or the DMA controller.
Filters are the core of the DFSDM function – they perform 1-bit stream filtering to provide higher output resolution at lower speeds.
There is an additional integrator behind the digital filter which provides additional data averaging.
Applications can be designed with various types of Sigma-Delta modulators (from various vendors).
The parallel data input feature can perform post-

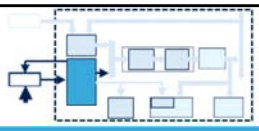
processing of any internal data (for example, internal ADC streams, audio data filtering, etc.).
Additional functions are explained later in detail.



The entire Digital Filter for Sigma Delta Modulators interface consists of:

- 4 Serial transceivers
- 4 Sinc filter parts and integrators
- 4 Output data units
- 4 Analog watchdogs
- 4 Short circuit-detectors
- 4 Extreme detectors
- 4 Parallel data input registers

DFSDM can provide one external output clock signal to drive external ΣΔ modulator(s) clock input(s). It is provided on CKOUT pin.



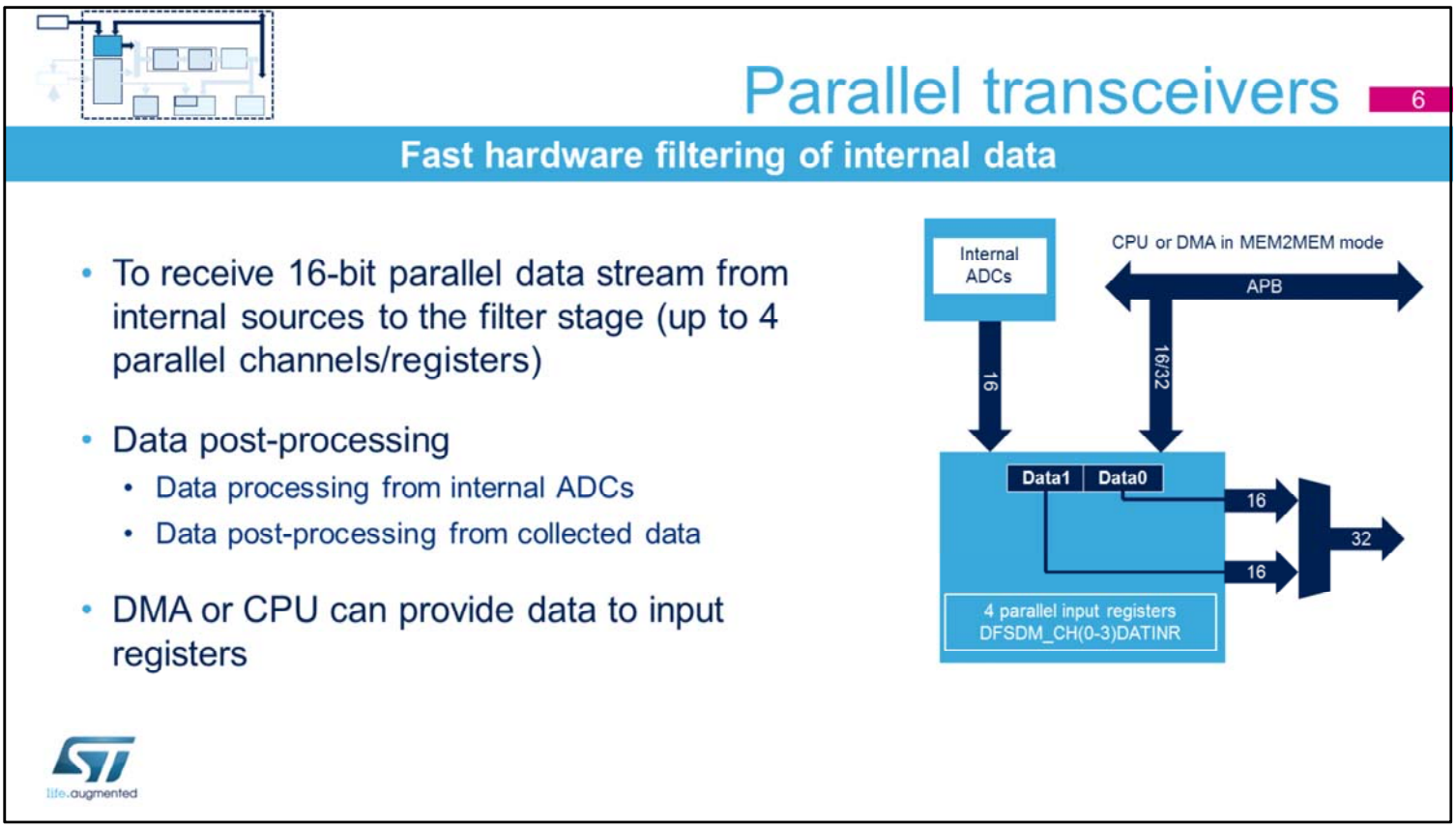
Serial transceivers

Compatible with any ΣΔ modulator output protocol

- To receive raw 1-bit serial stream from SD modulator and provide data & clock to the filter stage (up to 4 input serial channels)
- Any SD modulator output protocol support:
  - SPI mode (clock and data wire): falling/rising sampling edge, data rate measurement, clock presence detection
  - 1-wire Manchester-coded mode: lowest system cost (single isolator per input channel)
- Output clock generation on external pin:
  - Derived from system clock or audio PLL clock (divider)

Serial transceivers provide the connection to the external Sigma-Delta modulator.
SPI mode works up to 20 MHz (or the DFSDM clock divided by 4). There are configurable options including sampling edge selection, data rate measurement, and clock presence monitoring.
1-wire Manchester-coded mode (where clock is recovered from the data) works up to 10 MHz (or DFSDM clock divided by 6).
A synchronization detection feature is available in Manchester mode.
Manchester mode also offers the lowest system cost in case of optical isolation of the Sigma-Delta modulator – then only one single isolator per input channel is necessary.
The DFSDM clock features a clock output signal to drive the Sigma-Delta modulator. It can be used as a source

for the SPI clock input by internal interconnection in order to save external pins.
The clock output has an adjustable division factor and can be driven either from the System clock or from the fine-tuned Audio PLL clock.

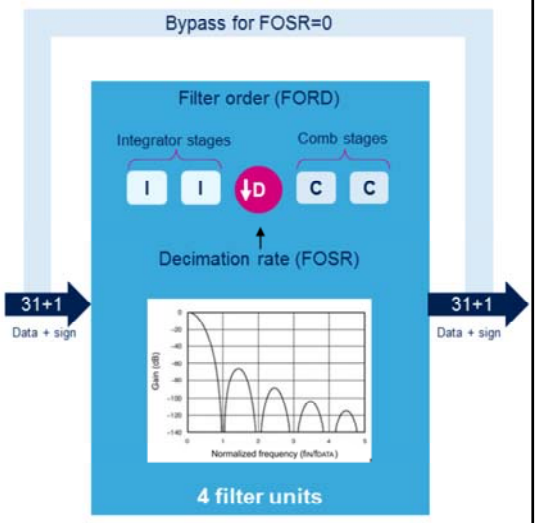


Parallel transceivers provide parallel inputs from internal data sources; for example, from memory buffers.
Parallel inputs are usually used for fast hardware filtering of internal data from the ADC or any data collected from a communication peripheral.
Data can be written to the DFSDM parallel input registers by the CPU or the DMA controller configured in memory-to-memory transfer mode.
Internal analog-to-digital converters can provide data directly to the DFSDM parallel input registers.

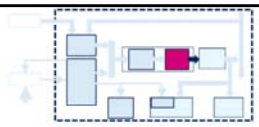
Sincx/x digital filter

CPU-free digital filtering

- Digital filter stage performs digital filtering of input data stream
  - Mean value of input data stream from SD modulator is the final ADC value (averaging)
  - Sincx filter performs moving average over given number of samples (oversampling ratio)
- Configuration options:
  - Filter type: Sinc1, Sinc2, Sinc3, Sinc4, Sinc5 and FastSinc
  - Oversampling ratio (FOSR): 1-1024 (can be bypassed)
  - Speed vs. resolution balance selection
  - Filter data resolution is 31-bit (maximum)



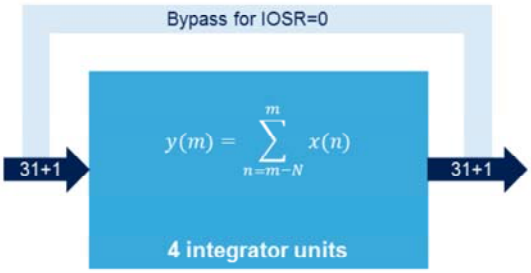
The digital filter averages the 1-bit input data stream from the Sigma-Delta modulator into a higher resolution, but with a slower data output.
The digital filter is a Sinc X type with an order from 1 to 5. A FastSinc type filter is also available for selection.
The oversampling ratio means how many samples will be averaged in a single filter run. The oversampling ratio can be selected in a wide range from 1 to 1024.
Not all combinations of filter order and oversampling ratios are available because in higher filter orders the oversampling ratio must be reduced to not overflow over the 31-bit data width (which is the internal filter resolution).



Integrator unit

Additional increase of resolution

- Integrator stage performs additional signal processing – averaging of data from digital filter (summing N samples)
- Configuration:
  - 1 to 256 samples (N) to sum
  - Can be bypassed (if IOSR = 0)
- Final result is sent to the output data unit



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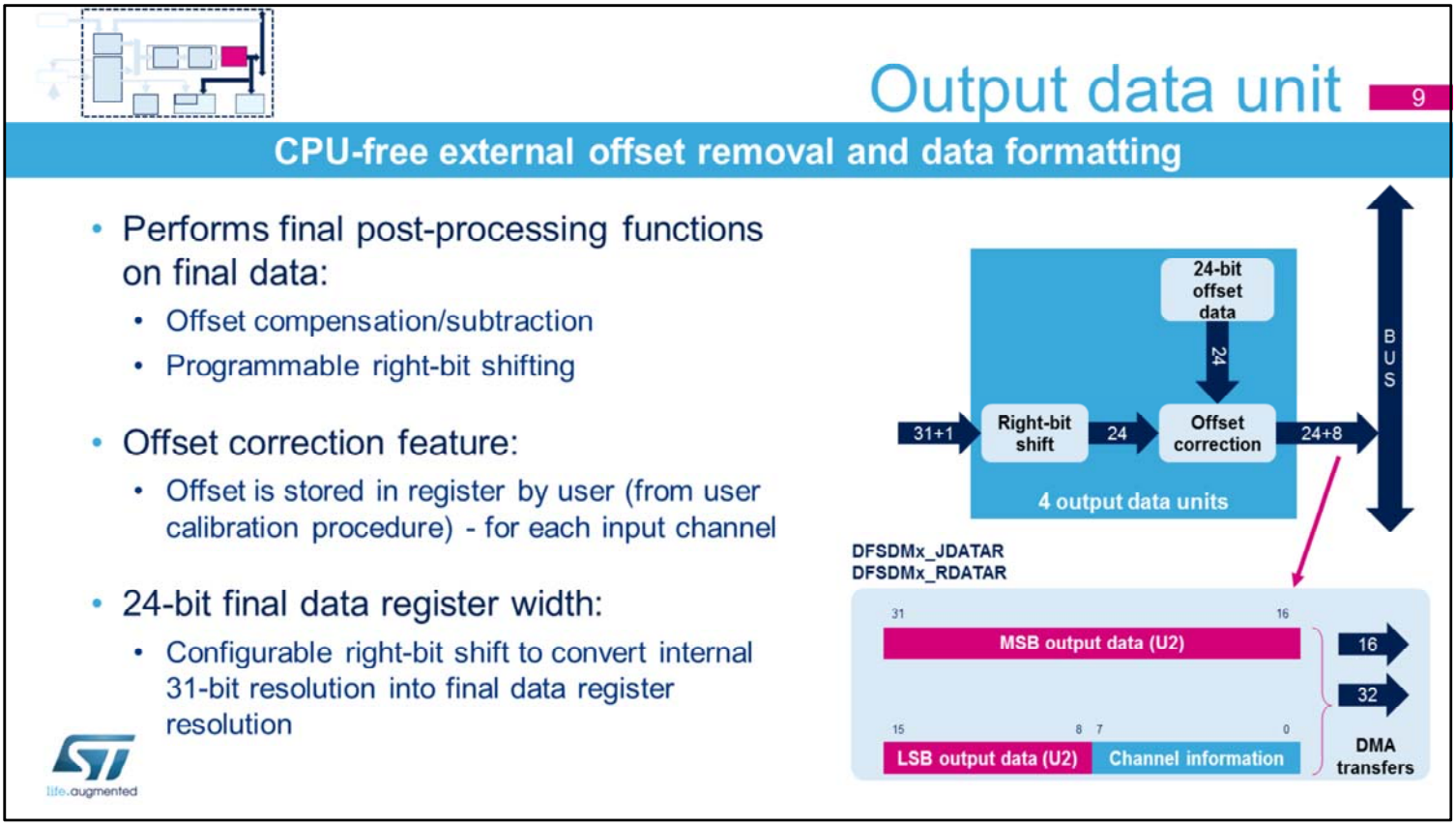
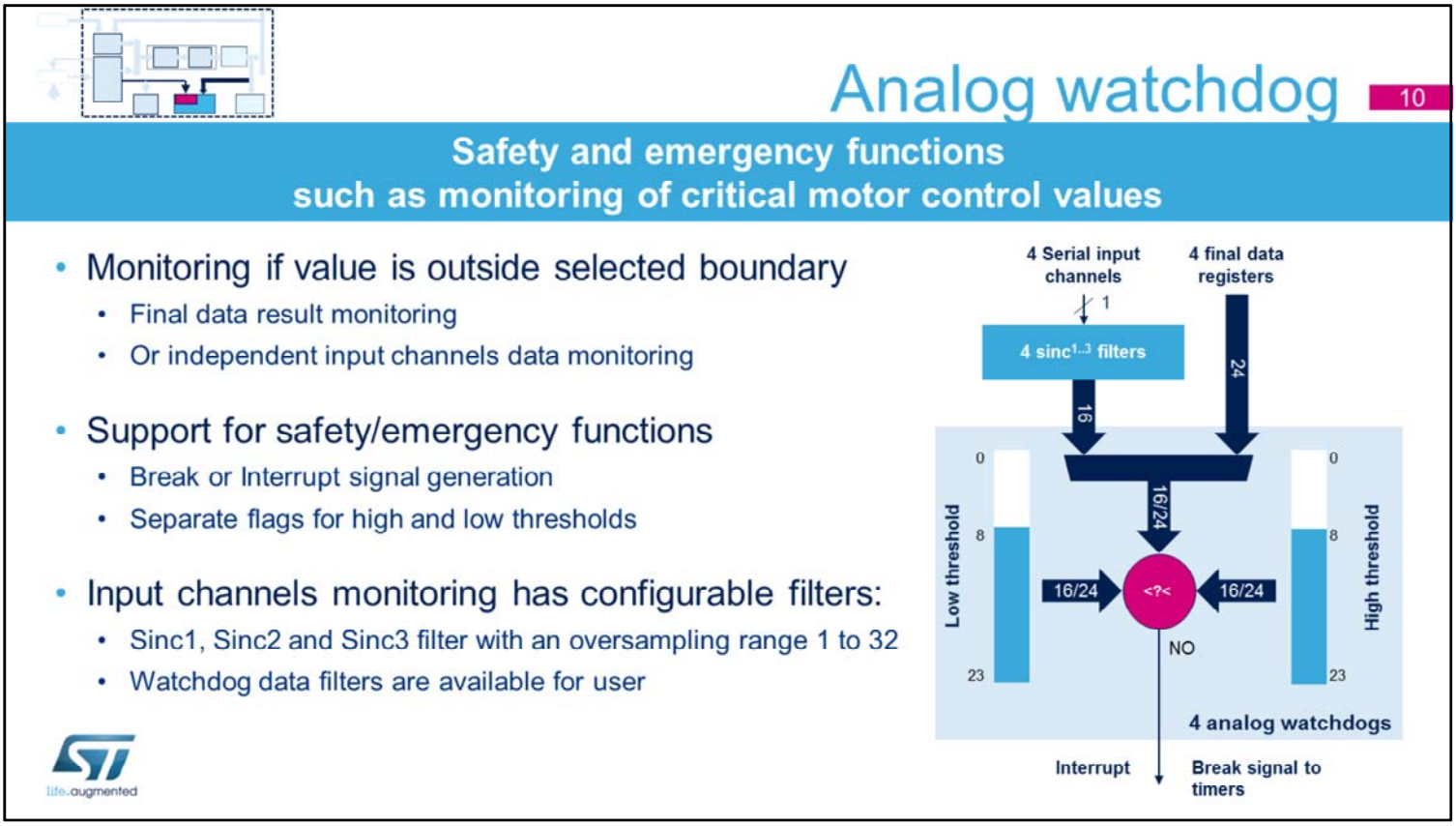
The Integrator unit performs additional simple averaging of data provided by the digital filter.
It provides just a simple summing of the data coming from the digital filter.
The number of samples to be summed can be set from 1 to 256. The correct configuration must take care that the final data length fits into the 31-bit width, which is the resolution of the internal integrator. The width of the data coming from the digital filter must also be taken into account.



The output data unit adjusts the final data before they are written to the final data register.
An offset value that will be automatically subtracted from the data result for each channel can be defined in the offset register. The correct offset values are determined using a calibration procedure. This calibration procedure should be programmed in user firmware and depends on the type of Sigma-Delta modulator connected and application needs.
The maximum resolution of the final output data register is 24 bits, but the internal resolution can go up to 31 bits. But certain applications have their own constraints; for example, 8-, 12-, 16-, or 24-bit data resolution.
Therefore, there is an option to perform a right-bit shift of the data to provide the final data result with the required width and not overflow the 24-bit width of the final data register. Right-bit shift is configurable from 0 to 31 bits.

The least significant byte contains channel status information.
The final resolution then depends on the digital filter and integrator settings as well as the right-bit-shift option.



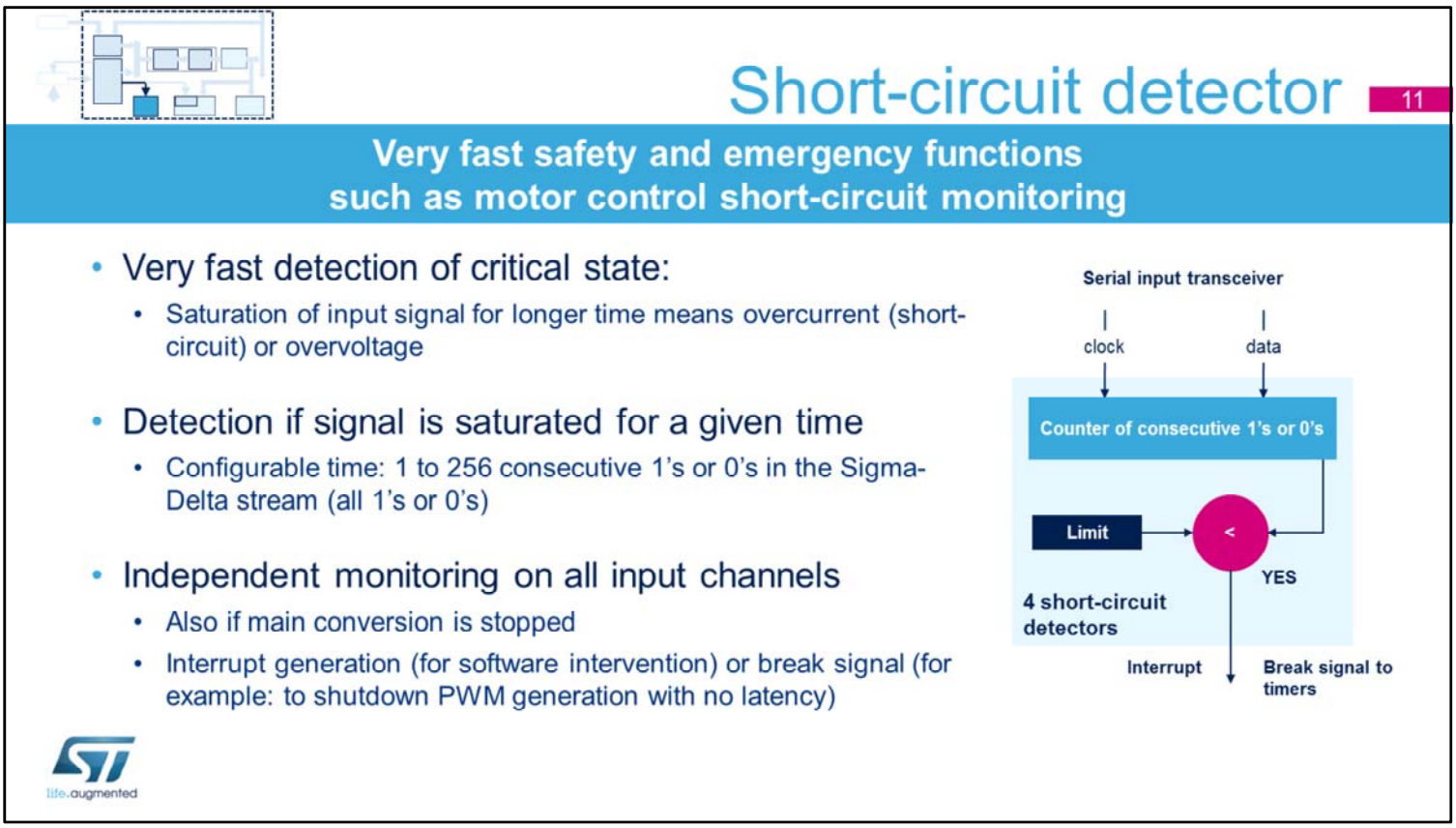
The analog watchdog monitors sample analog data to determine if it remains within the selected high and low threshold values. The input to the analog watchdog function can come from the result of the final converted data or directly from the input serial channels through a configurable filter.

If data exceeds the allowed boundaries, an interrupt can be requested or a break signal generated. In the case of an interrupt, software decides about the next actions. In the case of a break signal generation, a timer controlling a motor can be automatically put in a safety state.

There are separate high and low threshold levels and separate flags for each threshold to know if a threshold has been reached.

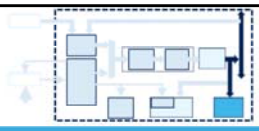
The analog watchdog can monitor 2 types of data. The first type is standard output data as with a standard ADC. The second type of data can come from serial

transceivers through configurable dedicated filters. This second option allows to select faster signal monitoring when the required speed and resolution is set by the filter parameters.
Each serial channel watchdog filter order is configurable from 1 to 3 and its oversampling ratio in the range from 1 to 32.
The data from these watchdog filters can also be read by user firmware.



The short-circuit detector monitors input serial channels for a saturation state. When an input signal is saturated, it means that it is outside the allowed measurement range and therefore there is an overflow or underflow condition. When measuring current, this event usually detects an overcurrent (or short-circuit), or an overvoltage when measuring the voltage.
Detection of input signal saturation is based on monitoring the input serial data stream coming from the sigma-delta converter and detecting consecutive ones or zeroes for a programmable delay. This maximum saturated time can be set in the range from 1 to 256 of sampled input data with the same value: zero samples or one samples.
Monitoring is performed independently from the main conversion. The main conversion can perform conversion from another channel or can also be stopped.

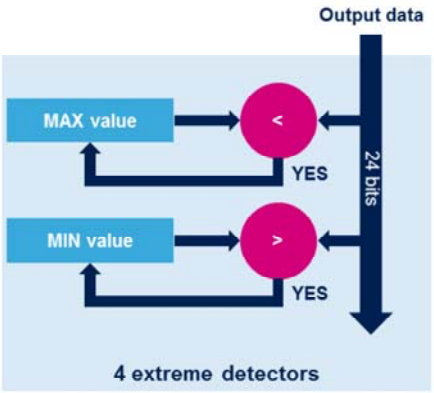
All input channels can be monitored in parallel with their own saturated time setting.
When a saturation event is detected, an interrupt can be requested or a break signal generated.
Then, just as with the analog watchdog, the software decides the following actions or the hardware break signal can perform a safety function without any software latency. For example, it can stop the timer which controls the motor in the event a short-circuit is detected.



Extremes detector

Hardware detection of peak values
Example: audio data normalization

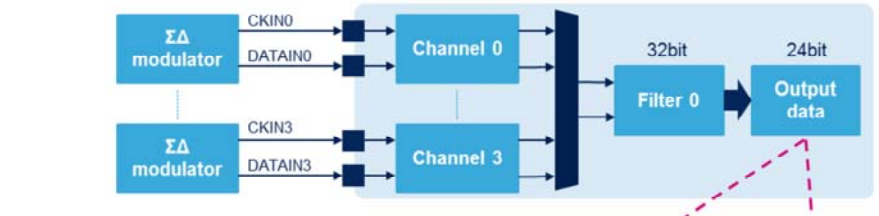
- Watching for minimum and maximum values in data output results
- Store the maximum and minimum values of the output data values into registers for selected channels
- Hardware monitoring of extreme values
- Extreme values are refreshed by software (by reading min/max registers)

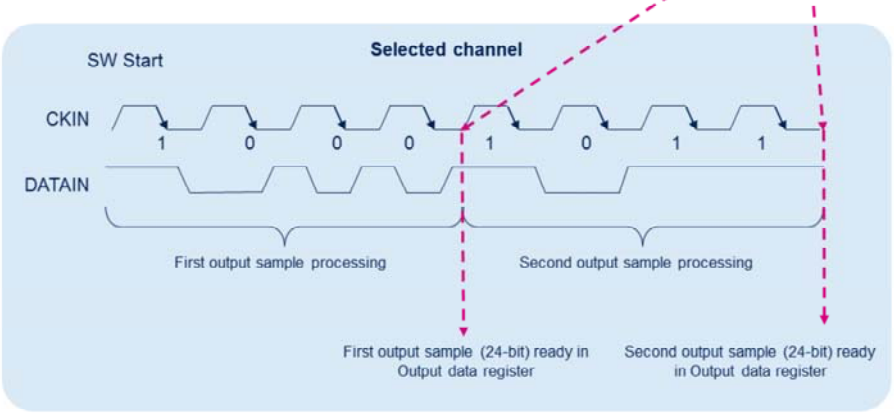


The extremes detector monitors output results and stores the extreme values into minimum and maximum registers as well as the associated channel number.
Monitoring of data for extremes is only performed on selected channels to ensure that channels do not mix different input levels.
Stored extreme values are refreshed each time the values are read in the register.

Regular conversions

- Only one channel selection (from 4 input channels)
- Launched by software only (no HW trigger)
- Continuous mode feature
- Can be immediately interrupted by injected conversion (with flag signaling this interruption)



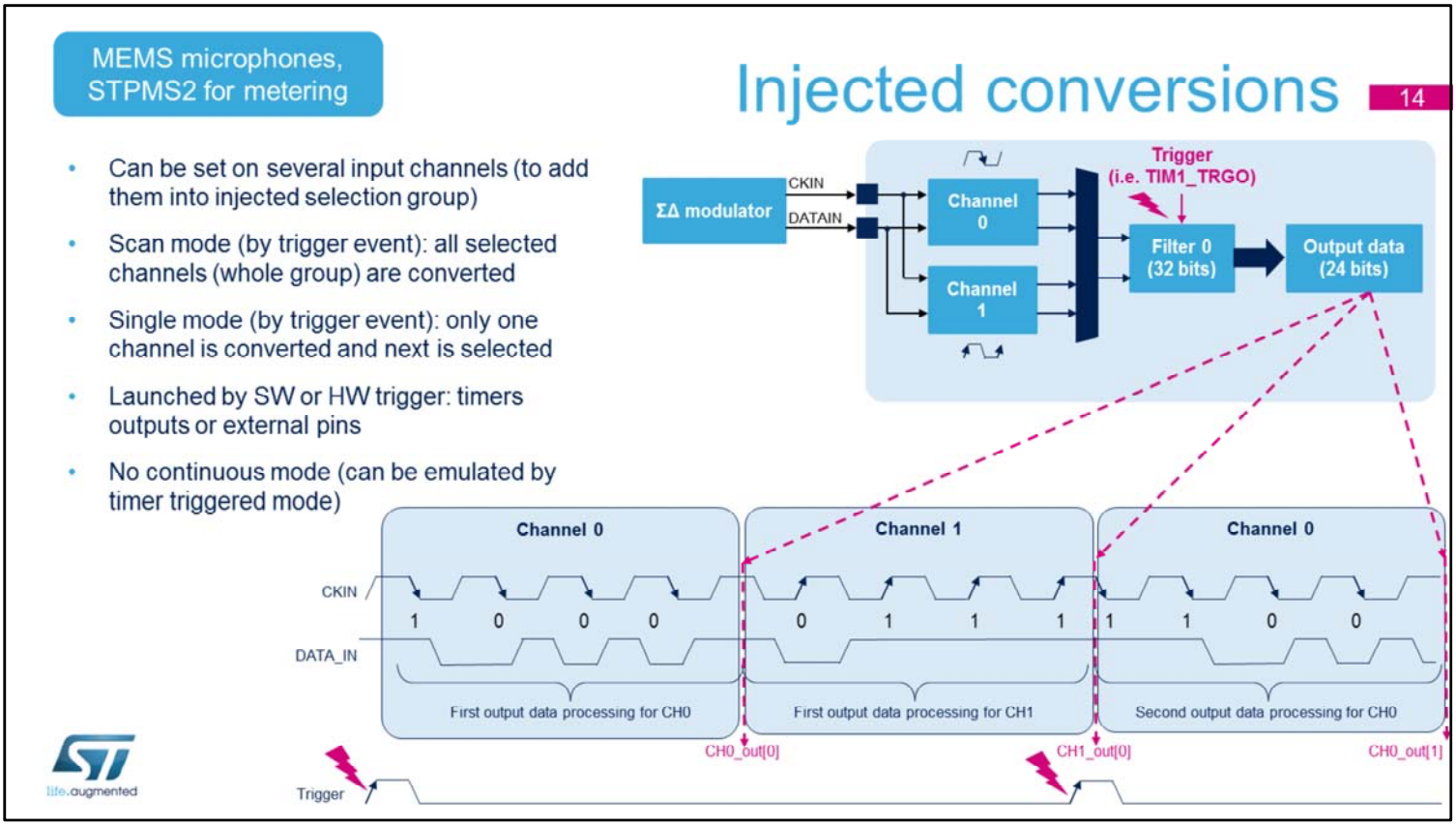


Regular conversions have lower priority and can be interrupted by an injected conversion. If the regular conversion was interrupted by an injected conversion, it is restarted once the injected conversion is finished and this interruption is indicated as a flag for this delayed regular conversion.

Regular conversions can be launched only by software and there is no scan mode available. Regular conversions can run in continuous mode, in which there is no channel switching, and they can be performed in fast mode without filter refill.

Regular conversions are used for measurements for which timing is not critical; for example, when measuring temperatures or slow signals.

Regular conversions are also typically used for continuous conversions from one channel only; for example, audio or energy-measurement applications.



Injected conversions have higher priority. They can interrupt regular conversions immediately and start just after being triggered. Any of the input channels can be assigned to an injected channels group. There are two modes of conversion behavior: scan mode and single mode.

In scan injected mode, all channels from the injected channels group are converted when a trigger occurs, starting from the lowest to the highest channel number in a group.

In single injected mode, only one channel from the injected channel group is converted and the next channel from the injected group is selected for the next conversion. The next trigger will start this next channel conversion and another higher channel from group is selected.

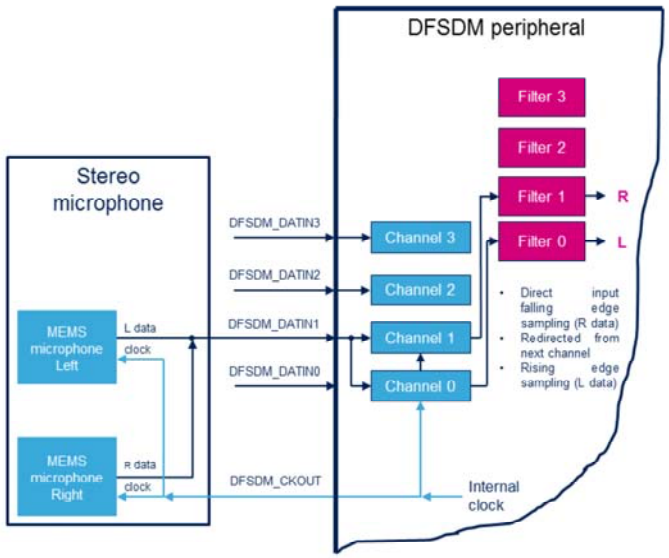
Injected conversions can be launched by software or by

hardware (from timers or an external pin).
Injected conversions cannot run in continuous mode, but this mode can be emulated using a periodic timer trigger.
Regular and Injected modes make it possible to choose the correct conversion mode according to application requirements.

MEMS microphone support (PDM)

Power consumption reduction and less CPU usage

- Microphones with PDM output support
- Simple connection:
  - Only 2 wires for both L/R microphones (common data and clock signal)
  - Channel separation is made inside (different sampling edges for L/R data)
- Output data rate and resolution set by filter configurations



The MEMS microphone provides a Pulse Density Modulated (PDM) data signal whose format is theoretically like the Sigma-Delta bit stream from Sigma-Delta modulator.
The MEMS microphone has stereo support if two microphones are connected in parallel with common data and clock signals:
Rising clock edge samples left audio data.
Falling clock edge samples right audio data.
Implementation into DFSDM transceivers requires this configuration:
Channel 0 uses redirection input from channel 1.
Channel 1 uses direct input.
Channel data (left vs. right) are separated inside by selecting either the rising or falling edge in the SPI configuration of channels.
The clock signal is provided by the DFSDM clock output

because the MEMS microphones are slaves and need an external clock for data sampling and communication.

Interrupts

Interrupt event	Description
End of conversion (regular/injected)	Set when conversion finishes (separate flags for regular and injected conversion)
Data overrun (regular/injected)	Set if injected converted data were not read from output data register (by CPU or DMA) and were overwritten by a new conversion (separate flags for regular and injected conversion)
Analog watchdog	Set if converted data (output data or data from analog watchdog filter) exceeds over/under high/low analog watchdog thresholds register (separate flags for high/low crossing detection)
Short-circuit detector	Set if the number of stable data samples exceeds selected short-circuit thresholds
Channel clock absence	Set if clock is absent on input serial channel clock pin

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A set of interrupts related to DFSDM events has been implemented to increase CPU performance.
This table lists all the DFSDM interrupt sources:

- End of conversion events, with separate flags for regular and injected conversions.
- Data overrun events, with separate flags for regular and injected conversions.
- Analog watchdog events.
- Short-circuit detector events.
- Channel clock absence event.

DMA

DMA request	Description
End of conversion (regular/injected)	DMA request is set when conversion finishes (regular or injected conversion)

- DMA requests can be enabled to decrease the CPU intervention to transfer converted data into memory
  - DMA channel configured as peripheral-to-memory transfer for data results transfer
- DMA "memory-to-memory" transfer mode can be used also as a parallel data input source – to transfer 16-bit data into the parallel input data register
  - The destination memory address is the address of DFSDM_CHyDATINR register

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To decrease the CPU intervention, conversions can be transferred into memory using a DMA transfer. DMA transfers for injected and regular conversions can be enabled separately. The DMA channel used to transfer the data results shall be configured in peripheral-to-memory mode.
The DMA controller can be used also as a method for fast data transfers into parallel data registers. In this case, the parallel data are transferred from the memory buffer into the parallel data register using the DMA mechanism. The DMA controller should therefore be configured in memory-to-memory transfer mode where the target address is the address of the parallel input data register.

Low-power modes

Mode	Description
Sleep	No effect ➢ Peripheral interrupts cause the device to exit Sleep mode
Low power run	No effect
Low power sleep	No effect ➢ Peripheral interrupts cause the device to exit Low-power sleep mode
Stop 1/2/3	Frozen ➢ Peripheral registers content is kept
Standby **Shutdown**	Powered-down ➢ The peripheral must be reinitialized after exiting Standby mode

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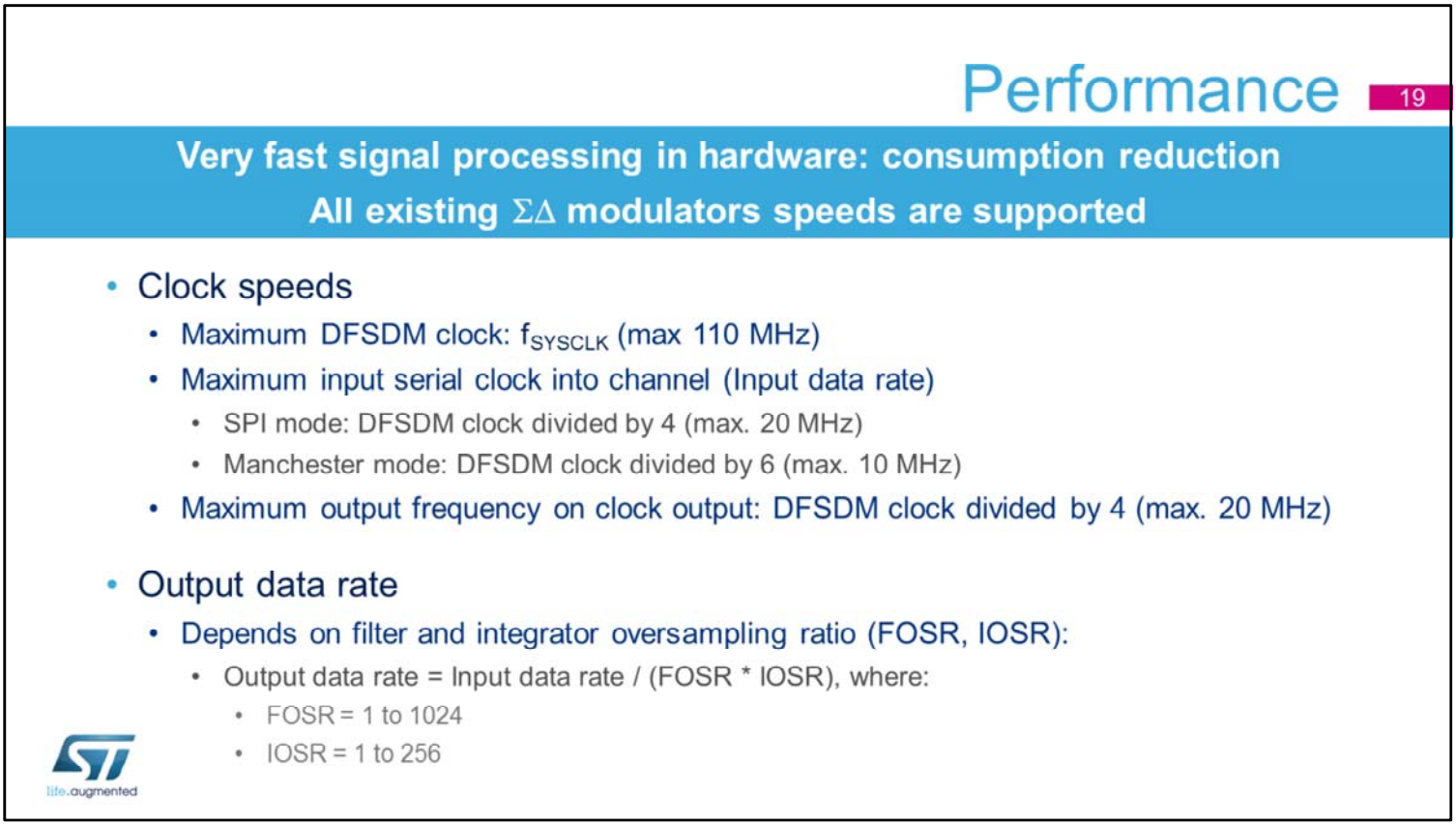
The DFSDM peripheral can be active only in Run and Sleep modes.
In Stop and Standby modes, the DFSDM must be disabled.



The DFSDM performance depends on the maximum allowed input data rate because each input data sample causes the next digital filter operation. The DFSDM allows operation at a maximum input data rate of 20 MHz in SPI mode or 10 MHz in Manchester mode.
Parallel data inputs have the same performance, so parallel data can be put into DFSDM at full 20 MHz speed using either the CPU or the DMA controller.
Applications benefit from the DFSDM high-speed processing which now supports all existing sigma-delta modulator speeds.

Application example 1- Stereo MEMS microphone

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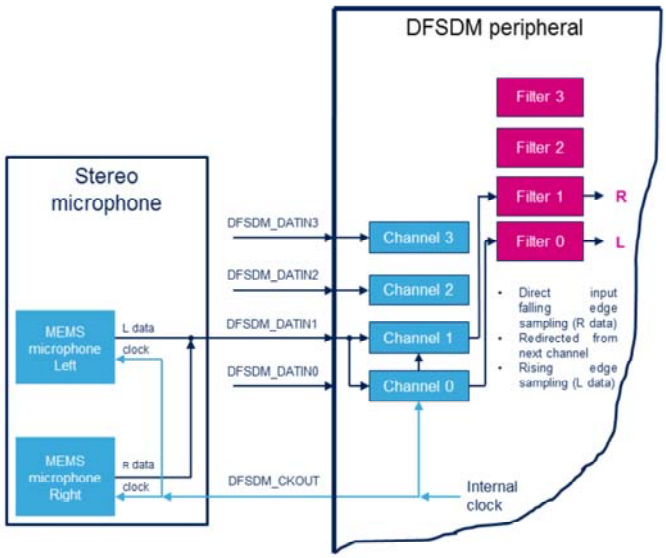
- Stereo MEMS microphone (with PDM output) playback
  - Only 2 wires are used to connect 2 microphones (stereo) – common clock and data wire with different sampling edges for left and right channels (and using the DFSDM feature: redirection of data from a given input channel pin to another channel's data input)
  - Regular conversions are used for two DFSDM channels in continuous mode.
  - Low CPU load:
    - One DMA transfers output audio data to RAM
    - Second DMA transfers those data to the I2S interface (which sends them to external audio codec and headphones)

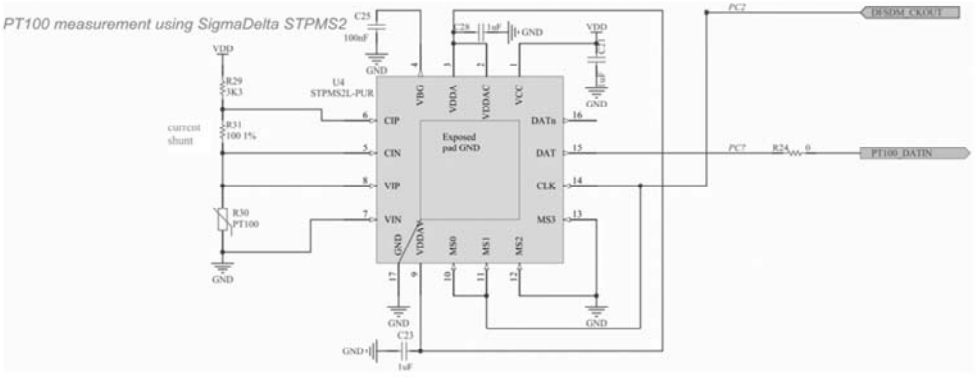


The STM32L5 evaluation board can be used to run simple application examples to help you explore the digital filter for Sigma-Delta modulators interface.
This example is a demonstration of the MEMS microphone directly connected to the DFSDM peripheral. Data from the microphone are processed by the DFSDM with correct filter settings and then collected into a memory buffer using regular continuous conversions and the DMA. The recorded data from the microphone are then immediately sent by the DMA controller from this buffer to the I2S peripheral and played by headphones.

Application example 2- PT100 thermometer

- An external STPMS2 device (dual-channel, second-order sigma-delta modulator) is used to sense 2 input channels
  - One channel senses voltage on PT100 sensor
  - Second channel senses current over PT100 sensor (on shunt)

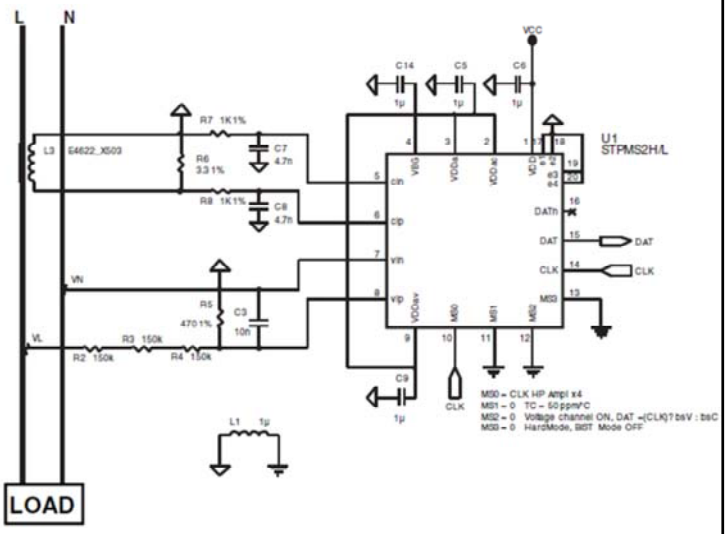
  Ratio of channels data results is the PT100 sensor resistance
- Injected scan conversion is used for those 2 channels with 1-sec periodic timer trigger



This example is a PT100 thermometer which uses an external STPMS2 sigma delta modulator which monitors two channels.
One channel senses the voltage and second one senses the current on the PT100 sensor.
Both channels are sampled using timer-triggered injected conversions in scan mode.
Software then computes the PT100 resistance from the collected data and finally the temperature.

Application example 3- Electricity meter

- Electricity meter with STPMS2
  - External STPMS2 device (dual SD modulator) is used to sense 2 input channels:
    - Voltage (voltage divider)
    - Current (current transformer or shunt)
  - Voltage and current samples are sent to DFSDM by serial interface (clock and data wire only)
  - The DFSDM processes the voltage and current samples into wide resolution
  - STM32 firmware calculates electric power and energy using FFT analysis

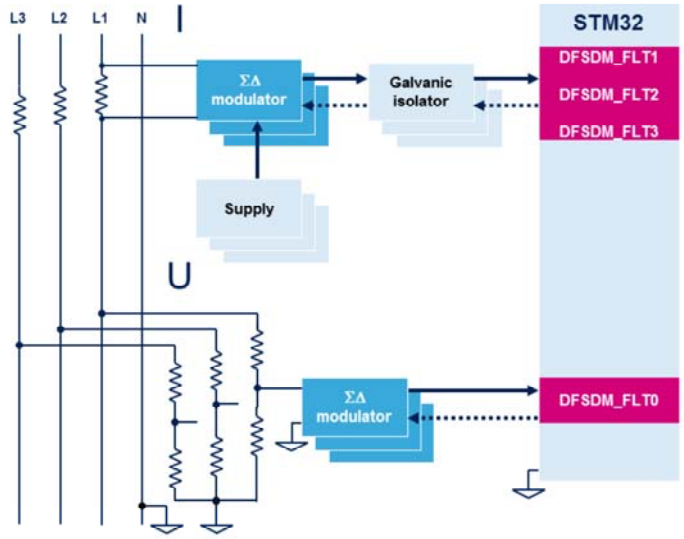


This example shows a typical one-phase electricity meter design using an STPMS2 device and STM32 microcontroller.
The STPMS2 is a dual-channel, Sigma-Delta modulator designed for electricity meter applications. It has voltage and current channel inputs.
The current channel features a programmable gain amplifier to cover a wide range of measured currents.
Sampled 1-bit data are sent by the serial interface to the host device (which is here the DFSDM interface).
Both voltage and current 1 bit data samples are sent on the same data wire, but the voltage is sampled on the rising clock edge while the current is sampled on the falling clock edge.
The clock is provided by the DFSDM and can run up to 4 MHz.
The DFSDM then processes the voltage and current channel 1-bit data streams into output data with a higher resolution and slower data rate.

Finally, the firmware uses FFT analysis to calculate the electric power and energy from the current and voltage samples.

Application example 4- 3-phase electricity meter

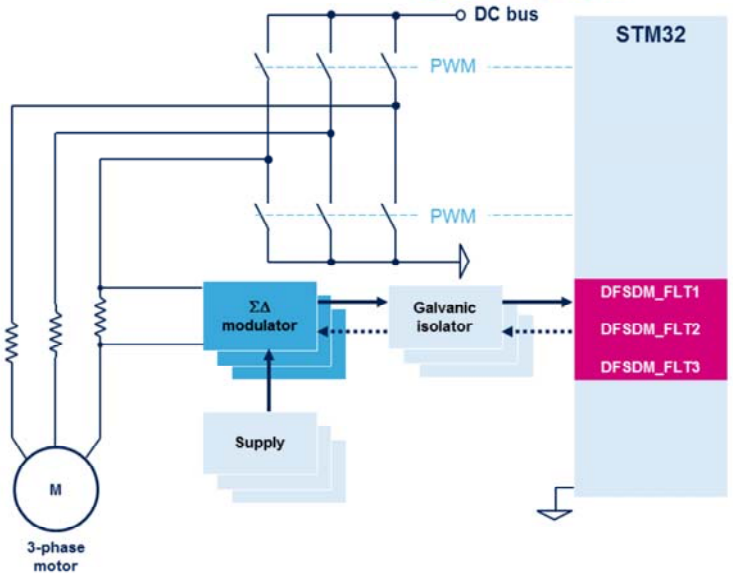
- 3-phase electricity meter (using shunts, no transformers)
  - Voltages (U) are sensed by resistor dividers
    - One DFSDM filter with 3 multiplexed inputs is used to scan 3-phase voltages.
  - Currents (I) are sensed by shunt resistors with galvanic isolated SD modulators
    - One or two isolation lines per phase are necessary only for current data transfers to DFSDM channels (Manchester-coded mode requires only 1 line)
  - STM32 firmware calculates electric power and energy



This example shows a 3-phase electricity meter design using shunt resistors for sensing current. There is no need to use expensive current transformers.
Voltages are sensed by three resistor dividers and external Sigma-Delta modulators.
Currents are sensed by three shunt resistors. Each shunt resistor voltage is sensed by one Sigma-Delta modulator. Because each Sigma-Delta modulator operates at a high-phase voltage, galvanic isolation is used for data transfers into the DFSDM. If the Sigma-Delta modulator uses the Manchester-coded serial protocol format (and has an internal clock source), only one isolator per phase is necessary.
If the Sigma-Delta modulator uses the SPI serial format, two isolators per phase are necessary. Each Sigma-Delta modulator is powered from a separate DC supply voltage.

Application examples 5- 3-phase motor control

- Used galvanic isolation for Sigma-Delta modulators: data and clock wires (for Manchester coding: data only)
- DFSDM performs 3 measurements from the same bit stream, in parallel:
  - High-accuracy low speed measurement, synchronized to the PWM period (uses main Sinc filter)
  - Continuous overload monitoring by watchdog (medium speed)
  - Continuous short-circuit detection with ultra-fast response (to disable the PWM generator)



life.augmented

This example is related to a 3-phase industrial (high-voltage, high-current) motor drive, where floating shunts and galvanic isolation are standard. A single reading channel is represented here, while in the application, 2 or 3 channels are used for the current in addition to 2 or 3 channels for the voltage. The currents are usually measured simultaneously by 3 DFSDM channels while the voltage can be measured sequentially with the same DFSDM channel.

The same bit stream is processed 3 times:

1st: For high-accuracy measurements, the main filter is used over a relatively long time. This is measured synchronously with a PWM period to avoid switching noise and have regular samples.

2nd: The watchdog channel uses the same bit stream with its own (lower order) filter, continuously monitors the signals and requests an interrupt in the case of an

overload, with medium reaction time.
3rd: The short-circuit detector is used to quickly detect a modulator saturation (continuous series of zeroes or ones with a programmable length), and automatically disables the PWM generator (through a dedicated DFSDM to the timer interconnection by a break signal).

Related peripherals

- Refer to these trainings related to this peripheral:
  - RCC (DFSDM clock control, DFSDM enable/reset)
  - Interrupts (DFSDM interrupt mapping)
  - DMA (DFSDM output data transfer, parallel data input)
  - GPIO (DFSDM input/output pins, triggers)
  - Timers (DFSDM trigger, break signal)
  - Peripherals interconnect matrix (DFSDM interconnection)

The peripherals listed here influence DFSDM behavior. Please refer to the corresponding training for more information.