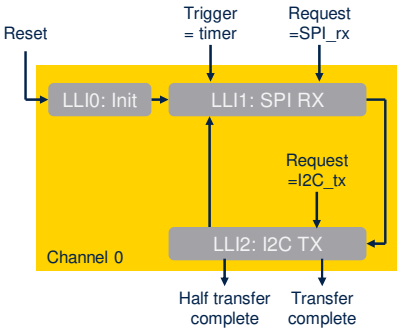
Hello, and welcome to this presentation which describes the control of the input and output signals of the GPDMA and LPDMA channels.

DMA transfer & input/output control DMA_CxTR2



- Flexible intra/inter channel synchronization at LLI level
- Programmable input control
  - Request selection
  - Trigger selection
  - Trigger mode vs transfer granularity
    - Data (block, 2D block, single/burst) or link
- Programmable output control
  - Event generation vs transfer granularity
    - Data (block, 2D block) or LLI or channel
  - Transfer complete hardware signal generation
    - Possibly used as trigger input of another channel
    - No need to be cleared, unlike the flag

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2

The DMA_CxTR2 register defines the input control (request, trigger events) and the output control (transfer complete event) of the transfer handled by the channel x at the LLI level.
This enables a flexible event-driven and hardware-based scheduling of a transfer under the global control of the software.
In the figure, a timer is used to trigger the transfer of the data received by the SPI module. When this transfer completes, a link to LLI2 is performed. The LLI2 handles an I2C transmission.
When this transfer completes, a link is performed to restore the settings related to the SPI receive transfer.
When the next timeout occurs, this sequence repeats.
The inputs of a DMA channel are:

- The request selection, for example the SPI Rx and the I2C Tx signals in the figure
- The trigger input. A programmed DMA transfer can be triggered by a rising/falling edge of a selected input trigger event, for example the timeout in the figure.

The transfer granularity conditioned by the trigger can be either the burst level, or the block level, or the 2D/repeated block level for channels 12 to 15, or the link level for the GPDMA.

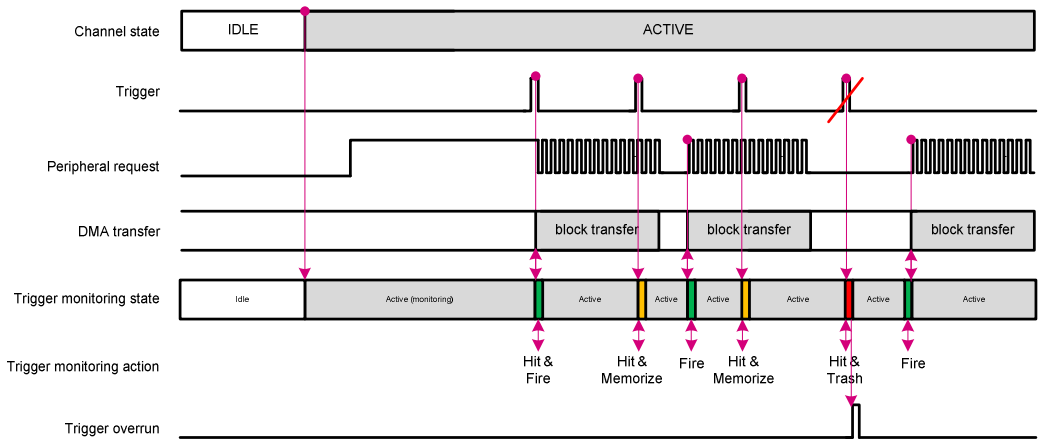
The transfer granularity conditioned by the trigger can be either the single data level, or the block level, or the link level for the LPDMA.

The output of a DMA channel is the transfer complete event, which can be used as a trigger input of another channel for inter-channel transfers chaining. Unlike the related software transfer complete flag, the software does not need to acknowledge and clear the transfer complete signal.

The transfer granularity for the transfer complete event generation can be either the block level or the 2D / repeated block level or LLI level or the channel level for the GPDMA.

The transfer granularity for the transfer complete event generation can be either the block level or LLI level or the channel level for the LPDMA.

Trigger hit, memorization and overrun



Configuration example:

- TRIGM[1:0]=2'b00 (block level);
- TRIGPOL[1:0]=2'b01 (rising edge)

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3

This timing diagram illustrates the trigger hit, the trigger memorization and the trigger overrun in the configuration example with a block-level trigger mode and a rising edge trigger polarity.

The DMA monitoring of a trigger for a channel x is started when the channel is enabled or loaded with a new active trigger configuration: rising or falling edge on a selected trigger.

The monitoring of this trigger is kept active during the triggered and uncompleted (data or link) transfer.

In this timing diagram, the first rising edge of the trigger starts the transfer, because the peripheral request is active.

If a new trigger is detected, this hit is internally memorized to grant the next transfer, as long as the

defined rising/falling edge and trigger selection are not modified, and the channel is enabled.
This is the case for the second rising edge of the trigger. It occurs when the first transfer is in progress. The second transfer is then triggered and starts when the peripheral request is asserted. This is the state called fire in the timing diagram.
After a first new trigger hit n+1 is memorized, if another trigger hit n+2 is detected and if the hit n triggered transfer is still not completed, hit n+2 is lost and not memorized.
A trigger overrun flag is reported and an interrupt is generated.
This is the case for the fourth rising edge of the trigger. The second rising edge is used to start the second block transfer. While this transfer is in progress, the third rising edge occurs and is memorized. Then the fourth rising edge causes an overrun condition, because the second transfer is not completed.
Note that the channel is not automatically disabled by hardware due to a trigger overrun.
Transferring a next LLIn+1, that updates the DMA_CxTR2 with a new value for any of trigger selection or trigger polarity, resets the monitoring, trashing the possible memorized hit of the formerly defined LLIn trigger.

Thank you

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In addition to this presentation, you can refer to the other presentations on the GPDMA and LPDMA:

- DMA overview
- DMA transfers hardware and software views
- Autonomous DMA & low power mode
- DMA linked list
- DMA Circular buffering & double buffering
- DMA 2D addressing
- DMA Register file
- DMA Error reporting.