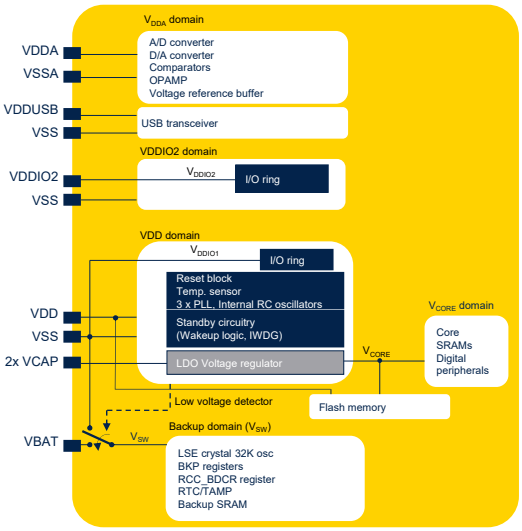
Hello, and welcome to this presentation of the STM32H5 power controller.
The STM32H5's power management functions and all power modes will also be covered in this presentation

STM32H503/56X/573 Power Supply with LDO

Supply	Min			Max	Description
VDDA		STM32H503	STM32H56X/573	3.6V	External analog power supply for ADC, DAC, COMP and OPAMP
	ADC	1.62V			
	COMP	1.62V	N/A		
	DAC	1.8V			
	OPAMP	2.0V	N/A		
	VREFBUF	N/A	2.1V		
VDDUSB	3.0V			3.6V	External independent power supply for USB transceivers
VDDIO2	1.08V			3.6V	External power supply for: ➢ STM32H56X/573: 10 I/Os (PD6, PD7, PG9:14, PB8, PB9) ➢ STM32H503: 9 I/Os (PA8, PA9, PA15, PB3:8)
VDD	1.71V			3.6V	External power supply for the I/Os that is, the internal regulator and the system analog such as reset, power management, and internal clocks
VBAT	1.2V			3.6V	Power supply when VDD is not present through power switch for RTC (real-time clock), external clock 32 kHz oscillator, backup registers and optionally backup SRAM



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STM32H5 devices have several independent power supplies, which can be set at different voltages or tied together.

The main power supply is VDD, supplying almost all I/Os except those part of the VBAT domain and some I/O pads powered by VDDIO2.

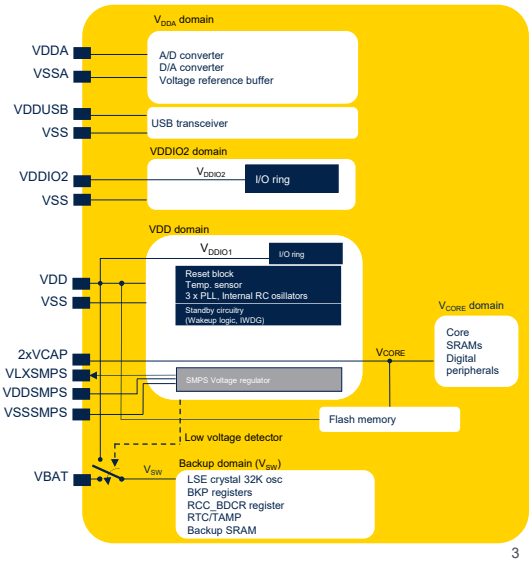
VDD also supplies the flash memory, the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog.

The STM32H503 only relies on integrated regulators, while STM32H56X and STM32H57X support either an Embedded regulator (LDO) or an SMPS stepdown converter regulator with configurable scalable output to

supply the digital circuitry.
VCORE supplies most of the digital peripherals, SRAMs and Flash memory controller.
VDDA voltage supplies the analog peripherals.
Also, USB transceiver and some I/O pads have their own independent power domains, powered by respectively VDDUSB and VDDIO2.
See the list of I/O pads powered by VDDIO2 in the table, it depends on the reference of the STM32H5.
A backup battery can be connected to VBAT pin to supply the backup domain.
If there are two VCAP pins (such as LQFP64 package), each pin must be connected to a 2.2 µF (typical) capacitor (for a total around 4.4 µF).
If only one VCAP pin is available, then it must be connected to a 4.7 µF capacitor.

STM32H563/573 Power Supply with SMPS

Power supply	Min	Max	Description
VDDA	1.62V (ADC, COMP) 1.8V (DAC) 2.1V (VREFBUF)	3.6V	External analog power supply for ADC, DAC, COMP and OPAMP
VDDUSB	3.0V	3.6V	External independent power supply for USB transceivers
VDDIO2	1.08V	3.6V	External power supply for: ➢ 10 I/Os (PD6, PD7, PG9:14, PB8, PB9)
VDD	1.71V	3.6V	External power supply for the I/Os that is, the internal regulator and the system analog such as reset, power management, and internal clocks
VDDSMPS	VDD	VDD	Supply voltage for the internal SMPS stepdown converter
VBAT	1.2V	3.6V	Power supply when VDD is not present through power switch for RTC (real-time clock), external clock 32 kHz oscillator, backup registers and optionally backup SRAM



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The STM32H56X and STM32H573 devices embed two regulators: one LDO or one SMPS depending on the package, to provide the VCORE supply.
The built-in Switched Mode Power Supply (SMPS) step down converter is a power-efficient DC/DC non-linear switching regulator that improves low-power performance when the VDD voltage is high enough.
The SMPS generates this voltage on VCAP (two pins), with a total external capacitor of 10 µF typical.
The SMPS generates the VCORE voltage on VCAP (two pins).
SMPS requires an external coil.

PWR features

Power supplies	STM32H503	STM32H562/573/563
VDD = 1.71 V to 3.6 V	**VDD** is provided externally through the VDD pins	
VDDA = **1.62 V (ADCs, COMP) to 3.6 V** **1.8 V (DAC) to 3.6 V** **2.0V (OPAMP) to 3.6 V** **2.1V (VREFBUF) to 3.6 V**	**VDDA** is independent from the VDD voltage and must be connected to VDD when these peripherals are not used	
VDDIO2 = 1.08 V to 3.6 V	**VDDIO2** is the external power supply for:	
	9 I/Os (PA8, PA9, PA15, PB3:8)	10 I/Os (PD6, PD7, PG9:14, PB8, PB9)
	The VDDIO2 voltage level is independent from the VDD voltage and must preferably be connected to VDD when those pins are not used	
VDDUSB = 3.0 V to 3.6 V	NA	**VDDUSB** is the external independent power supply for USB transceivers.
VBAT = 1.2 V to 3.6 V	**VBAT** is the power supply when VDD is not present through power switch for RTC (real-time clock), external clock 32 kHz oscillator, backup registers and optionally backup SRAM	

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This slide and the next one list the power supplies and related signals of the STM32H5.
VDD is the main I/O power supply.
VDDA is the analog power supply and positive reference voltage for the ADC.
VDDIO2 is an independent I/O supply for 9 or 10 I/O pads, depending on the exact reference of STM32H5.
The VDDIO2 voltage level is completely independent from VDD or VDDA. The VDDIO2 pin is available only for some packages.
VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage and must preferably be connected to VDD when the USB is not used.

A VBAT input is available for connecting a backup battery in order to preserve the RTC functionality and to backup 32x 32-bit registers and 4-Kbyte SRAM.

PWR features

Power supplies	STM32H503	STM32H562/573/563
VDDSMPS = 1.71 V to 3.6 V	NA	**VDDSMPS** is the external power supply for the SMPS step-down converter. It is provided externally through **VDDSMPS** supply pin, and must be connected to the same supply as VDD pin
VLXSMPS	NA	**VLXSMPS** is the switched SMPS step-down converter output
VREF-, VREF+	NA: VREF+/VREF- are bonded internally with VDDA/VSSA	**VREF+** is the input reference voltage for ADCs and DACs ➢ When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled **VREF-** must always be equal to VSSA
	NA	**VREF+** is also the output of the internal voltage reference buffer when enabled ➢ VREF+ can be grounded when ADC and DAC are not active VREF- and VREF+ pins are not available on all packages

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The I/O pads required to use the SMPS converter are:

- VDDSMPS, which is the external power supply for the SMPS step-down converter, to be connected to the same supply as VDD pin
- VSSSMPS is the SMPS ground
- VLXSMPS, which is the output of the SMPS step down converter, to be connected to ground through 2.2 µHenry inductance an 10 µF capacitor.

The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters.

When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled.

VREF+ is also the output of the internal voltage reference buffer (VREFBUF) when enabled.

Embedded Voltage Regulator

- Linear voltage regulator (LDO) is enabled on power-on reset
- To supply the VCORE from an external source
  - It is possible to disable the regulator by setting BYPASS bit in the PWR_SCCR register
- STM32H5xx devices embed one LDO or one SMPS, to provide the digital peripherals, SRAMs and the embedded Flash memory
  - Depending on the package configuration (SMPS or LDO)
  - The regulator is selected by hardware (SMPS and LDO regulator are exclusively selected)

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The Low Dropout (LDO) linear voltage regulator is enabled on power-on reset.
To supply the VCORE from external source, it is possible to disable the regulator by setting BYPASS bit in the PWR_SCCR register.
In this bypass mode, the internal voltage scaling is not managed internally, and the external voltage value must be consistent with the targeted maximum frequency.
Some STM32H5 MCUs embed two internal regulators to provide VCORE supply: LDO and SMPS, exclusively enabled by hardware, depending upon package configuration.

Power Supply Supervision

Monitor	Description	Event when out-of-range condition is detected
POR (Power-on reset)/ PDR(power-down reset)	The system has an integrated POR/PDR circuitry that ensures proper startup operation ➢ The system remains in reset mode when VDD is below a specified VPOR threshold, without the need for an external reset circuit	System reset
BOR (Brownout reset)	During power-on, the brownout reset (BOR) keeps the system under reset until the VDD supply voltage reaches the specified VBOR threshold ➢ A system reset is generated when the BOR is enabled and VDD supply voltage drops below the selected VBOR threshold	System reset
PVD (Programmable voltage detector)	The PVD can be used to monitor the VDD power supply by comparing it to a software programmable threshold ➢ The PVD can also be used to monitor a voltage level on the PVD_IN pin ➢ In this case PVD_IN voltage is compared to the internal VREFINT level	Interrupt
AVD (Analog voltage detector)	The AVD can be used to monitor the VDDA supply by comparing it to a software programmable threshold	Interrupt
VDDIO2 Voltage monitor (IO2VM)	The IO2VM monitors the independent supply voltage VDDIO2 to ensure that the peripheral is in its functional supply range	Flag
Out of functional range temperature monitor	A dedicated temperature sensor cell is embedded in the power control ➢ The junction temperature can be monitored by comparing it with two threshold levels, TEMPhigh and TEMPlow	Tamper
Out of functional range Backup domain voltage monitor	In VBAT mode, the battery voltage supply (backup domain) can be monitored by comparing it with two threshold levels: VBAThigh and VBATlow	Tamper

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The following units monitor the power supplies:

- Power-On-Reset and Power-Down-Reset, that ensure proper startup operation without needing an external circuit
- Brownout Reset, able to trigger a reset in case of VDD power drop
- Programmable Voltage Detector, that can be used to detect power drop for any power supply
- Analog Voltage Detector, that monitors VDDA
- VDDIO2 voltage monitor, that checks whether VDDIO2 is in functional range
- Two tamper detection mechanisms: junction temperature monitoring against fixed thresholds and VBAT power supply monitoring against fixed thresholds when VBAT mode is active.

Dynamic Voltage scaling

- The STM32H5 series support dynamic voltage scaling, to optimize the power consumption in run mode
- The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating Frequency
- Both regulators (LDO or SMPS) can provide four different voltages (voltage scaling) and can operate in Stop modes

Voltage scaling Range	Vcore	Max frequency
VOS0	1.35 V	250 MHz
VOS1	1.2 V	200 MHz
VOS2	1.1 V	150 MHz
VOS3	1.0V	100 MHz

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The STM32H5 MCUs support dynamic voltage scaling to optimize their power consumption in Run mode.
Dynamic Voltage and Frequency Scaling (DVFS) is an energy saving technique that exploits:

- The linear relationship between power consumption and operational frequency
- The quadratic relationship between power consumption and operational voltage.

The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.
Both regulators can provide four different voltages (voltage scaling) and can operate in Stop modes.
The main regulator operates in the following ranges:

- VOS0 (Vcore = 1.35V) with CPU and peripherals running at up to 250 MHz
- VOS1 (Vcore = 1.2V) with CPU and peripherals running at up to 200 MHz
- VOS2 (Vcore = 1.1V) with CPU and peripherals running at up to 150 MHz
- VOS3 (Vcore = 1.0V) with CPU and peripherals running at up to 100 MHz.

Embedded Voltage Regulator Operating Modes

Power mode	Description
RUN	• The voltage provides full power to the V_{CORE} domain • The regulator output voltage can be scaled by the software to different voltage levels • The VOS voltage scaling allows optimization of the power consumption when the system is clocked below the maximum frequency
STOP	• The voltage regulator supplies the V_{CORE} domain to retain the content of registers and internal memories • To further optimize the power consumption, the unused RAMs can be totally or partially shut-off • Internal oscillator HSI64 or CSI can be kept active during Stop in order to reduce wakeup time
STANDBY	• The regulator is OFF and the V_{CORE} domains are powered down • The content of the registers and memories is lost, except for the Standby circuitry and the Backup domain

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The embedded voltage regulator implements three different power modes: Run, Stop, and Standby mode.
In RUN mode, the voltage is provided to the VCORE domain according to the current voltage scaling level.
In STOP mode, the voltage is provided to the VCORE domain to a retention value, that ensures that registers contents and memory contents are preserved. Unused RAMs can be totally or partially shut off.
In STANDBY mode, the VCORE domain is powered down.

Low Power Modes

Power mode	Description
SLEEP	• CPU clock off, all peripherals including Cortex-M33 core such as NVIC and SysTick can run and wake-up the CPU when an interrupt or an event occurs
STOP	• The voltage regulator supplies the V_{CORE} domain to retain the content of registers and internal memories • To further optimize the power consumption, the unused RAMs can be totally or partially shut-off • Internal oscillator HSI64 or CSI can be kept active during Stop in order to reduce wakeup time
STANDBY	• The regulator is OFF and the V_{CORE} domains are powered down • The content of the registers and memories is lost, except for the Standby circuitry and the Backup domain • This mode achieves the lowest power consumption with BOR
VBAT	• Only the VBAT domain is powered • RTC, backup registers and anti-tamper detection circuit remain active • The GPIOs included in VBAT domain are directly controlled by the peripherals providing functions on these I/Os, whatever the GPIO configuration

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By default, the microcontroller is in Run mode after a system or a power reset.
Several low-power modes are available to save power when there is no need to keep the CPU running, for example when waiting for an external event

- SLEEP: Cortex-M33 core clock is gated off, while the remaining parts of the CPU continue to run, particularly NVIC and SysTick
- STOP based on the Cortex-M33 Deepsleep mode combined with the peripheral clock gating
- STANDBY, based on the Cortex-M33 Deepsleep mode, with the voltage regulators disabled
- VBAT, in which only the VBAT domain remains powered.

Each of these modes is going to be detailed in the next slides.

Low Power Modes-SLEEP Mode

- CPU clock off, all peripherals including Cortex-M33 core such as NVIC and SysTick can run and wake up the CPU when an interrupt or an event occurs
- Wakeup sources:
  - Any peripheral interrupt/wakeup event
- Wakeup system clock
  - Same as before entering Sleep mode
- Voltage regulators:
  - VOS3, VOS2, VOS1 or VOS0

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In SLEEP mode, the CPU clock is off, however all peripherals including Cortex-M33's embedded peripherals NVIC and SysTick can run and wake-up the CPU when an interrupt or an event occur .
In Sleep mode, all I/O pins keep the same state as in Run mode.
Software can decide for each peripheral whether its clock is gated off in SLEEP mode.
Wakeup sources are peripherals interrupts and wakeup events.
The clocks sources required to exit SLEEP modes are the same as the ones active before entering SLEEP mode.
Voltage regulators are active with voltage scaling levels VOS3 downto VOS0.

Low Power Modes-STOP Mode

- All clocks in the core domain are stopped, PLL, HSE crystal oscillators, HSI (except if HSIKERON is set), HSI48 and CSI RC (except if CSIKERON is set) are disabled
- LSE or LSI is still running
- RTC can remain active (Stop mode with RTC, Stop mode without RTC)
- System clock when exiting from Stop mode can be either HSI up to 64 MHz or CSI, depending on software configuration
- Wakeup sources: Any EXTI line (configured in the EXTI registers) Specific peripherals events

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Stop mode achieves the lowest power consumption, while retaining the content of SRAM and registers. All clocks in the Cortex-M33 core domain are stopped.
Stop mode stops all the clocks in the core domain and disables the PLLs, HSI, HSI48, CSI and HSE oscillators. However, HSI or CSI can be switched ON to generate a wakeup interrupt.
LSI and LSE remain active in Stop mode.
The RTC remains active when the RTC clock source is LSE or LSI.
RTC interrupts cause the device to exit the Stop mode.
The user selects which oscillator is used for exiting STOP mode: either HSI (64 MHz) or CSI (4 MHz).
The MCU exits Stop mode by enabling an EXTI interrupt

or event depending on how the low-power mode was entered.
When exiting the Stop mode, the MCU is in Run mode, VOS3.

Low Power Modes-STOP Mode

- Wakeup system clock:
  - CSI when STOPWUCK = 1 in RCC_CFGR
  - HSI with the frequency before entering the Stop mode, up to 64 MHz, when STOPWUCK=0
- Voltage regulators: SVOS3, SVOS4, or SVOS5

Voltage scaling Range	Vcore
SVOS3	1.0 V
SVOS4	0.9 V
SVOS5	0.74 V

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The HSI oscillator is selected as system clock if STOPWUCK control bit is cleared.
The wake-up time is shorter when CSI is selected as wake-up system clock, however the HSI selection allows a wake-up at higher frequency (up to 64 MHz).
The voltage regulator is configured by STOP Voltage Scaling SVOS control bits
The selected SVOS4 and SVOS5 levels add an additional startup delay when exiting from system Stop mode.

Low Power Modes- STANDBY Mode

- The internal regulator is switched off, the core domain is powered off
  - SRAMs and register contents are lost except for registers and backup SRAM in the Backup domain and Standby circuitry
- The PLL, the HSI RC, HSI48, the CSI RC and the HSE crystal oscillators are also switched off
  - The RTC can remain active (Standby mode with RTC, Standby mode without RTC)
- The Brownout reset (BOR) always remains active in Standby mode
- The state of the I/O (except I/Os used by standby mode) during Standby mode can be retained
- Wakeup sources: WKUPx pin edge, RTC event, external Reset in NRST pin, IWDG Reset
  - Wakeup system clock: HSI clock at 32 MHz

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The lowest power mode in which the brownout reset is active is the Standby mode.
In this mode, the regulator (LDO or SMPS) is OFF and the VCORE domains are powered down.
The SRAMs and register contents are lost except for registers in the Backup domain and Standby circuitry.
Standby mode stops all the clocks in the core domain and disables the PLLs, HSI, HSI48, CSI and HSE oscillators.
GPIOs state can be retained during Standby mode.
When exiting from the Stop mode or Standby mode, the Run mode voltage scaling is reset to the default VOS3 value.
The microcontroller exits Standby mode through an external reset (NRST pin), an IWDG reset, a rising edge

on one of the enabled WKUPx pins or an RTC/TAMPER event.
The system clock after wake-up is HSI at 32 MHz.

I/Os state retention during standby mode

- In the Standby mode, the I/Os are by default in floating state
- The IOs retention is configured by the IORETEN bit in the PWR_IORETR register

PWR_IORETR[IORETEN]	Description
0	IO Retention mode is disabled
1	IO Retention mode is enabling for all IO except the IO support the standby functionality and PA13, PA14, PA15 and PB4 (JTAG / SWD IO pads) ➢ When entering into standby mode, the output is sampled, and apply to the output IO during the standby power mode

- The state of I/Os is applied to the pin via pull-up and pull-down resistors, that remain applied after Standby wakeup until the IORETEN bit in the PWR_IORETR register is cleared by software

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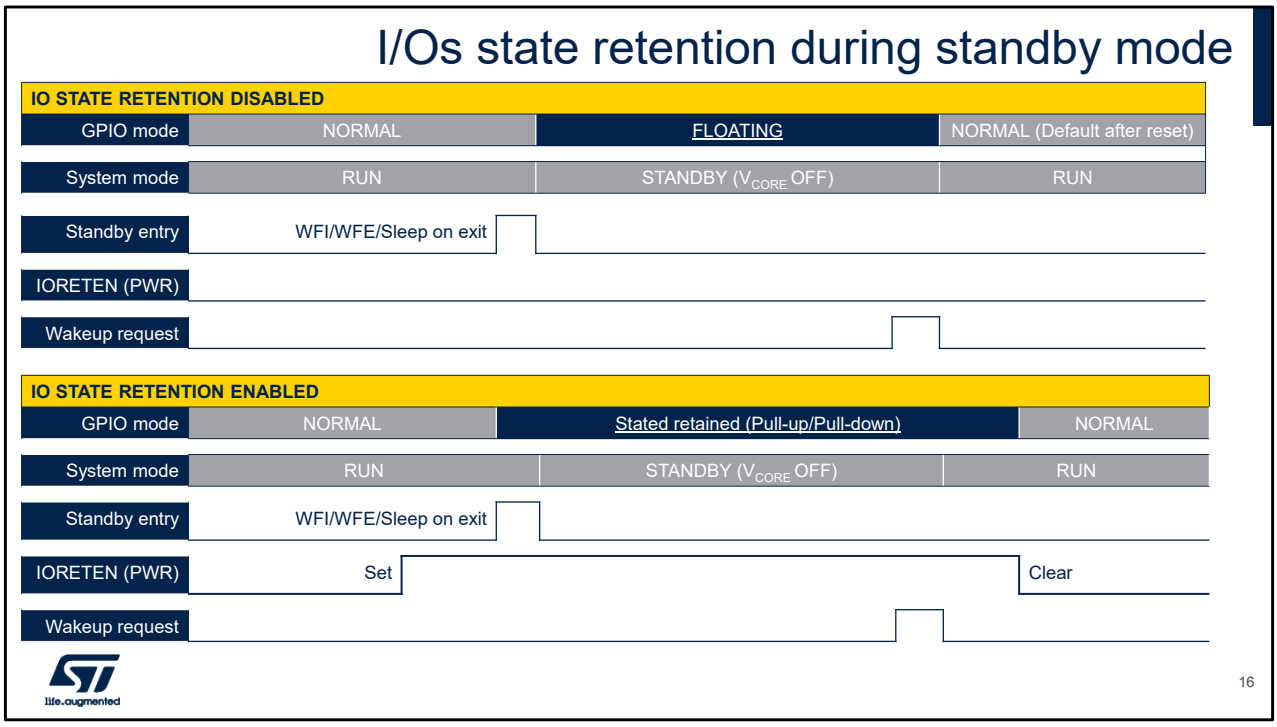
In the Standby mode, the I/Os are by default in floating state.
If the IORETEN bit in the PWR_IORETR register is set, the I/Os output state is retained.
I/O retention mode is enabled for all I/Os except those supporting the standby functionality and debug probe related IOs (PA13, PA14, PA15 and PB4).
When entering into Standby mode, the state of the output is sampled, and pull-up or pull-down resistor are set to maintain the I/O output during Standby mode.
After wakeup from Standby mode, as long as IORETEN bit is set, the retained state (pull-up/pull-down) remains applied.
Note that the STM32H5 features a separate control bit to activate IO retention on JTAG and Serial Wire Debug I/Os.



In the top timing diagram, IO retention is disabled, because IORETEN control bit is cleared at the time the microcontroller enters the STANDBY mode.
When software enters the STANDBY state due to Wait For Interrupt, Wait For Event instructions or Sleep on Exit mode, GPIOs transition to floating state, until a wakeup event occurs.
In the bottom timing diagram, IO retention is enabled.
When software enters the STANDBY state, GPIO's state is retained, until a wakeup event occurs, and software clears the IORETEN control bit.

Low-power mode monitoring pins

CSLEEP (1)	CSTOP (2)	MCU power modes (3)
0	0	Run mode
1	0	Sleep mode
1	1	Stop mode

(1) PWR_CSLEEP alternate function mapped on PC3

(2) PWR_CSTOP alternate function mapped on PC2

(3) CSLEEP and CSTOP signals are generated in V_{CORE} domain, consequently they are not driven in Standby

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In order to help the debug, two signals are available as device pin alternate functions: CSLEEP and CSTOP.
They enable to track transitions to / from RUN, SLEEP and STOP modes.
CSLEEP when set, indicates that the system is in Sleep or STOP mode.
CSLEEP when cleared, indicates that the system is in Run mode.
CSTOP when set, indicates that the system is in STOP mode, no AHB/APB clock is running
CSTOP when cleared, indicates that the system is not in STOP mode: AHB/APB clocks are running.
Since CSLEEP and CSTOP are generated in core domain, they are not driven in Standby mode.

VBAT mode

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including tamper pins
  - Backup registers
  - RCC_BDCR register
  - Backup memory, when backup regulator is enabled
- Automatic internal switch between VBAT and VDD when VDD is powered down and powered on
  - The switch to the VBAT supply is controlled by the power-down reset embedded in the Reset block
- Internal connection to ADC for voltage monitoring (VBAT/4)
- VBAT battery charging
  - When VDD is present, It is possible to charge the external battery on VBAT through an internal resistance

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The backup power domain includes:
- RTC and LSE oscillator
- Tamper pins
- RCC_BDCR register, that, among others, determines whether RTC clock is enabled
- Backup SRAM and the 32 backup registers.

In VBAT mode, only the LSE is running.
The RTC is functional in VBAT mode when it is clocked by the LSE.
The backup power domain remains powered-on by VBAT when the VDD power is switched off, switching is done automatically when VDD is powered down.
One channel of the ADC is dedicated for monitoring the external VBAT power supply pin.

The battery charging is enabled when setting VBE bit in the PWR_BDCR register.
When VDD is present, it is possible to charge the external battery on VBAT through an internal resistance
This is automatically disabled in VBAT mode.

PWR Interrupts

- The table below gives a summary of the interrupt sources and the way to control them
  - PWR interrupt requests

Interrupt vector	Interrupt event	Event flag	Enable control bit	Interrupt clear method	Exit Sleep, Stop modes	Exit and Standby modes
PVD/AVD output	Programmable voltage detector through EXTI line 16	PVDO/AVDO	EXTI line 16 enabled	Write EXTI PIF16 = 1	Yes	No

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The PWR module has a unique interrupt request that signals an event detected by the Programmable Voltage Detector or the Analog Voltage Detector.
The interrupt is connected to the EXTI module.
A power drop detected in the VDD or VDDA power domain can therefore be reported to software via an interrupt request.
These events also cause an automatic exit from SLEEP and STOP modes.

Option bytes

- The following option bits can be configured to prohibit a given low-power mode:
  - nRST_STDBY: When cleared, a reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a reset is generated when entering Stop mode

Two bits are available in the flash option bytes to prohibit entering a given low-power mode.
When cleared, these option bits trigger a reset when entering either Standby or Stop modes.
This is a security feature used to reduce the impact of unintentional entry into these low-power modes.
If these low-power modes are not used in user code, the option should be enabled.

PWR TrustZone security

- The PWR TrustZone security allows the following features to be secured through the PWR_SECCFGR register:
  - Low-power mode
  - Wake-up (WKUP) pins
  - Voltage detection and monitoring
  - VBAT mode
  - I/Os retention configuration
- Other PWR configuration bits are secure when:
  - The system clock selection is secure in RCC: the voltage scaling (VOS) configuration is secure
  - The UCPD1 is secure in the GTZC: the PWR_UCPDR register is secure

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When the TrustZone security is activated by the TZEN option byte in the flash memory option byte configuration register, some PWR register fields can be secured against non-secure access.
This is controlled by the PWR_SECCFGR register, which sets secure access permissions to sensitive PWR registers.
The following features can be programmed to be accessible only from the secure world:
-Low power modes
-Configuration of wakeup pins
-Voltage detection and monitoring
-I/O retention.
When the TrustZone security is disabled,

PWR_SECCFGR is read as zero / write-ignored and all other registers are non-secure.
An inheritance mechanism is implemented for other configuration registers of the PWR module:
- When The system clock selection is secure in RCC, the voltage scaling (VOS) configuration is secure
- When the UCPD1 is secure in the global trustzone controller: the PWR_UCPDR register is secure.

Thank you

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In addition to this training, you can refer to the following presentations:

- Reset and Clock Control
- Real-Time Clock
- Tamper.

See also the Application Note AN4938 for further explanations about the STM32H5 hardware development.