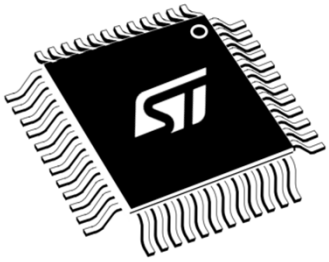
Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the microcontroller.

Overview



- Provides an interface for interaction with the external environment
  - Fully configurable
  - With interrupt and wake-up capability
  - Direct connection to AHB bridge

Application benefits

- Direct microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to AHB allows fast toggle response

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General-purpose IO pins of STM32 microcontrollers provide an interface with the external environment.
This configurable interface is used by the MCU and, also all other embedded peripherals to interface with both digital and analog signals.
Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.

Key Features

- Bi-directional operation of up to 68* I/O pins
  - Shared across up to 5 GPIO ports named GPIOA to GPIOF, with up to 16 I/O pins per port
    - All with external interrupt and wake-up capabilities
  - Atomic bit set and bit reset using BSRR and BRR registers
  - Independent configuration for each I/O pin
  - All most of I/O ports are in analog as default configuration after reset
- GPIOx register interface is directly connected to AHB bus and can be controlled with DMA
- Most I/O pins are 5 V tolerant

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* : Depends on part numbers and packages

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The general-purpose I/Os ports provide bidirectional operation – input and output – with an independent configuration for each I/O pin.
They are shared across up to 5 ports named GPIOA to GPIOD, and GPIOF.
I/O ports are directly connected to the AHB bus, thus enabling high-speed operation.
Each of them hosts up to 16 I/O pins.
I/O ports support atomic bit set and reset operations through BSRR registers, which allows the user to set and reset each individual bit of the output data register GPIOx_ODR.
During and just after reset, the alternate functions are not active and most of the I/O ports are configured in analog

mode to reduce power consumption.
Most of the I/O pins are 5 V tolerant when supplied from VDDIO above 1.6 V.

Operating modes

Flexible operating modes to best fit application needs

- Input modes
  - Floating (no pull resistor), input with pull-up/down, and analog input modes
- Output modes
  - Push-pull and open-drain modes with optional pull-up/down
- Analog function for ADC, DAC, operational amplifier and comparator
- Configurable output slew rate speed
- Alternate function mode (AF mode)
  - Push-pull and open-drain modes with optional pull-up/down
- Locking mechanism to freeze the I/O port configuration (GPIOx_LCKR)

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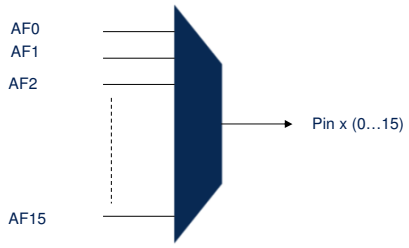
General-purpose I/O pins can be configured into several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input.
An I/O pin can be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 different ranges to compromise between maximum speed and emissions from the I/O switching and to adjust the application's EMI performance.
I/O pins are also used by other embedded peripherals to interface with the external environment.

Alternate function registers are used to select the configuration for the peripherals in this case.
Configuration of the I/O ports can be locked to increase robustness of the application.
Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.

Alternate functions

Structure of I/O pins is used as interface by other embedded peripherals

- Several integrated peripherals share the same I/O pins
  - Including USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, …
- Alternate function multiplexer selects the peripheral connected to the I/O pin
  - Only one alternate function is connected to a specific I/O pin at a single time
  - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers (x = A..D, F)



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Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins to interface with the external environment.
Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to an I/O pin at a single time.
Of course, this selection can be changed while the application is running through the GPIOx_AFRL and AFRH registers.

Independent VDDUSB supply

Independent VDDUSB brings benefits in a multi-supply environment

- VDDUSB* supply domain is independent of VDD
- Pins in the VDDUSB domain can be used to communicate with other circuits, i.e. USB, which are supplied by voltage rails other than VDD
- Up to 3 I/O pins

Application benefits

- Well suited for applications with two different power supplies / supply voltage without the need for external of level shifters

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* : Depends on part numbers and packages

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The Independent VDDUSB supply domain allows operation in an environment with several different logic supply voltages.
This second power rail can be used by up to 3 I/O pins, to communicate with other logic circuits, for instance USB, which are supplied by voltage rails other than VDD.
The use of independent voltage supplies may eliminate the need for external voltage shifters in the design.

Special considerations for I/O pins

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions are not active
  - I/O ports default to analog mode
  - Saves current consumption during and after reset (Schmitt trigger is off)
- Only SWD debug pins remain in AF pull-up/pull-down configuration
  - PA13: SWDIO
  - PA14: SWCLK
- PF2 share NRST and GPIO features
- PF3 can be used as boot pin (BOOT0) or as a GPIO

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During and after reset, the alternate functions are not active, only debug pins can be used in Alternate Function mode.
PF3 may be used as boot pin (BOOT0) or as a GPIO.
Depending on the nSWBOOT0 bit in the user option byte, it switches from the input mode to the analog input mode:

- After the option byte loading phase if nSWBOOT0 = 1.
- After reset if nSWBOOT0 = 0.

GPIO pin configuration

GPIOx are individually configured throught registers

GPIOx MODER[1:0]	GPIOx OTYPER	GPIOx OSPEED[1:0]	GPIOx PUPD[1:0]		I/O Configuration
0b00	X	X	0	0	Input, floating
			0	1	Input, Pull-up
			1	0	Input, pull-down
0b01	0	SPEED[1:0]	0	0	GP output, push-pull
	0		0	1	GP output, push-pull, pull-up
	0		1	0	GP output, push-pull, pull-down
	1		0	0	GP output, open-drain
	1		0	1	GP output, open-drain, pull-up
	1		1	0	GP output, open-drain, pull-down
0b10	0	SPEED[1:0]	0	0	Alternate function, push-pull
	0		0	1	Alternate function, push-pull, pull-up
	0		1	0	Alternate function, push-pull, pull-down
	1		0	0	Alternate function, open-drain
	1		0	1	Alternate function, open-drain, pull-up
	1		1	0	Alternate function, open-drain, pull-down
0b11	X	X	X	X	Input/Output Analog

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The configuration of any IO pin is achieved through 4 registers: GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR:

- Register GPIOx_MODER selects the functionality of the IO pin: digital input, digital output, digital alternate function or analog
- Register GPIO_OTYPER is relevant when the pin is an output: it selects open drain vs push-pull operation
- Register GPIOx_OSPEEDR configures the I/O output speed.
- Register GPIOx_PUPDR is relevant when the pin is not configured in analog mode. It enables /disables pull-up and pull-down resistors.

I/O output speed ranges are:

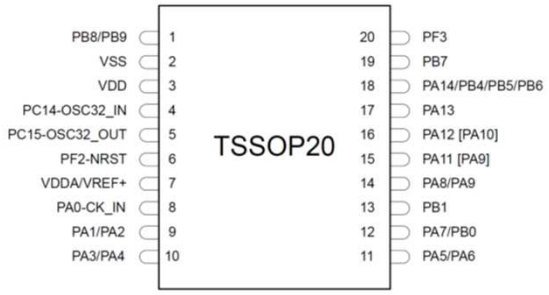
- 1 to 10 MHz
- 10 to 25 MHz
- 25 to 50 MHz
- 50 to 75 MHz.

This maximum frequency depends on VDDIO power supply and capacitive load.

Remapable GPIOs

Couple of I/O pins can be physically remapped

- Two GPIOs PA12 and PA11 can be remapped by PA10 and PA9 respectively in order to give access to their functions when the pins are not natively available on the package
  - The remap is handled through the SYSCFG_CFGR1 register



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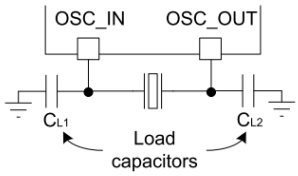
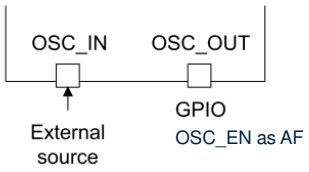
The two pins PA9 and PA10 can remap the two GPIOs PA11 and PA12 respectively.
With this remapping, alternate functions related to pins PA9 and PA10 are available.
For example, the STM32U031xx TSSOP20 package does not support PA10. If an alternate function of PA10 is required, then it can be output on PA12.
Note that this remapping also applies when the package supports pins PA9 and PA10 as independent pins.

Special considerations for HSE/LSE

OSC_OUT GPIOs can be used as standard IO

- When the oscillator is switched OFF, related pins behave as I/O pins
  - Valid for both HSE / LSE
  - This state is the default one after reset
- When user external clock mode is used, the second pin behaves as an I/O pin
  - Only OSC_IN or OSC32_IN is used as clock source
  - OSC_OUT and OSC32_OUT are I/O pins with OSC_EN feature in alternate function





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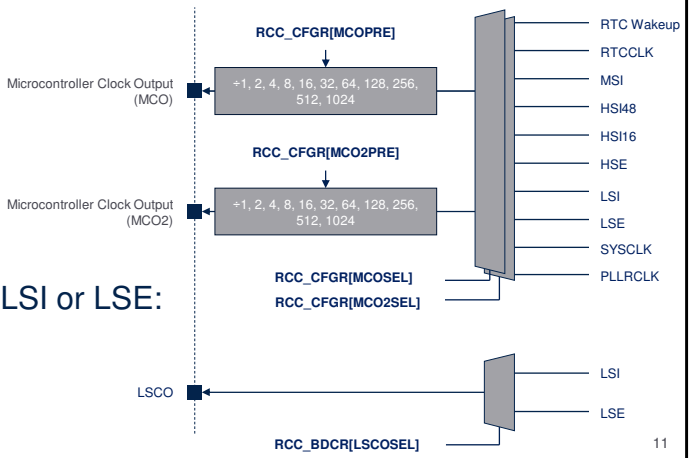
When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after a device reset.
When the external clock source is used instead of a crystal oscillator, only the related OSC_IN pin is used for the clock and the OSC_OUT pin can be used as a standard I/O pin or OSC_EN alternate function.

Clock-out on dedicated GPIO capability

Flexible multiplexed MCO and LSCO I/Os

- Multiplexers for MCO and MCO2, able to output clock on alternate function:
  - PA8, PA9, PF2 as MCO
  - PA8, PA10, PC2 as MCO2
- Multiplexer for LSCO, able to output LSI or LSE:
  - PA2 as LSCO



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STM32U0 allows to output most internal and external clock through the MCO and MCO2 multiplexers and use it as a clock source for other application components.
In addition, low sources clocks such as LSI and LSE can be also output on LSCO GPIO.

Multi-supply I/O pins

Some I/O pins can be supplied from different sources

- New I/O pin supply scheme brings new I/O pin structures and names
  - FT (Five Volt Tolerant) definition is extended by new abbreviation suffix
  - Maximum VIN is defined by lowest supply voltage connected to the structure of given I/O pin
  - For example, formula V_{IN} < min (V_{DD}, V_{DDA}) + 4.0 V applies for FT_a pin

Abbreviation suffix	Description	Example
_l	I/O with LCD function supplied by VLCD	FT_la
_f	I/O with Fm+ capability, supplied by VDD ➢ Fast-mode Plus (Fm+) bit rate of up to 1 Mbit/s and extra output drive I/Os	FT_f
_a	I/O with analog switch function, supplied by VDDA	FT_la
_u	I/O with USB function, supplied by VDDUSB	FT_ul

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A new multi-supply scheme of I/O pins brings new I/O pin structures.
Previously-used naming – FT (Five Volt Tolerant) , TT (Three Volt Tolerant) – has been extended by abbreviation suffixes to highlight alternate supply sources for each FT and TT I/O pin.
Previously-used name FTf for Fm+ capable pins has been transformed to FT_f, suffix _a marks pins supplied by analog supply, suffix _u is used for pins supporting USB.
The absolute maximum rating for each I/O pin is defined by the lowest voltage of the supplies listed for each I/O pin.

Low-power modes

Mode	I/O Description	Wake-up capability
Run	Active	NA
Sleep	Active	Any GPIO configured as EXTI
Low-power run	Active	
Low-power sleep	Active	
Stop 0	Active	
Stop 1	Active	
Stop 2	Active	
Standby	I/Os can be configured with internal pull-up, pull-down or floating in Standby mode	PA0, PC13, PE6, PA2, PC5
Shutdown	I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode	
Reset	Forced to Analog input mode when the MCU is under reset	NA

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I/O pins remain active in all modes except Standby and Shutdown, where the only available configuration is input with internal pull-up, pull-down resistor or floating input. When exiting Shutdown mode, the I/O configuration is lost. When the MCU is under reset, I/O pins are forced into an analog input mode.

Thank you

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Thanks for attending this presentation.