Hello, and welcome to this presentation, which describes the DMA 2D addressing mode supported by GPDMA. This is not to be confused with the Chrom-ART Accelerator controller, also known as DMA2D, which also implements 2D addressing mode.

GPDMA ch12-15
Burst, block and 2D addressing

- Linear addressing modes (LP, GP)
  - Fixed addressing (typically for peripheral data register access)
  - Contiguously-incremented addressing (typically for memory access)
    - Contiguous data blocks in memory (for a given LLIn), scanned from head to tail
  - Blocks up to 64kB (16-bit BNDT)

- Additional 2D addressing modes (GP ch12..15)
  - Repeated block mode: programmable repeated block counter (11-bit BRC, up to 2k blocks)
  - Programmable source/destination signed burst address offset (2x 14bit, up to +/-8kB)
    - Non-contiguous incremented/decremented addressing after each burst
  - Programmable source/destination signed block address offset (2x 17bit, up to +/-64kB)
    - Non-contiguous incremented/decremented addressing after each block

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2

This slide summarizes the addressing modes supported by both LPDMA and GPDMA.
LPDMA and GPDMA implement the following addressing modes:

- Fixed addressing, typically used to access a peripheral data register
- Contiguously-incremented addressing, typically used to access memory, in ascending address order
- The maximum block size is 64 kilobytes, due to the 16-bit field called BNDT, which stands for Block Number of Data bytes to Transfer.

The GPDMA channels 12 to 15 implement additional addressing modes:

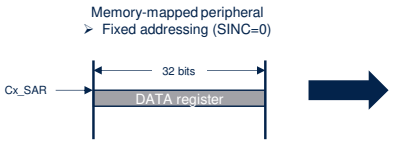
- Repeated block mode, based on a programmable counter

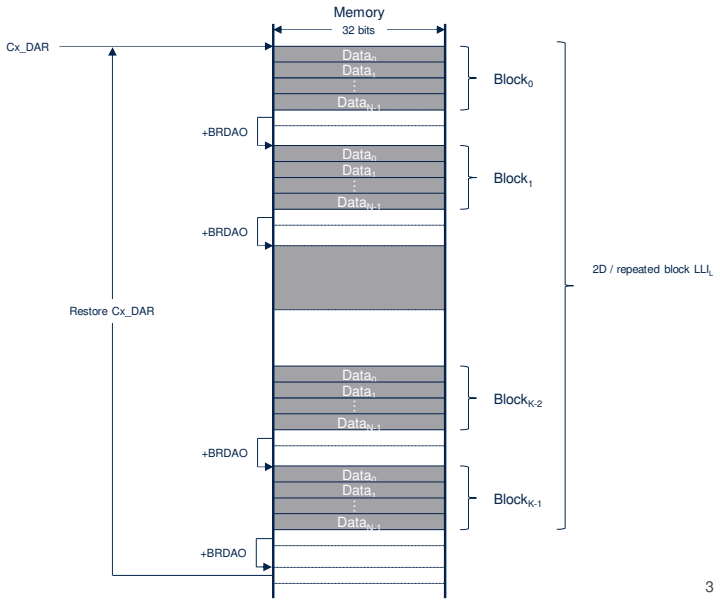
- Programmable source and destination signed burst address offset
- Programmable source and destination signed block address offset.

Thus, two programmable strides can be inserted: between consecutive bursts and between consecutive blocks.

2D addressing mode (continuous) (de)interleaving data/channels GP ch12-15

- Example: contiguous burst within a block
  - LLI: K blocks





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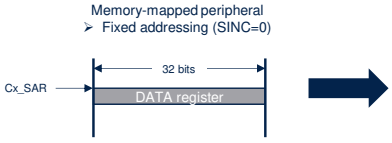
3

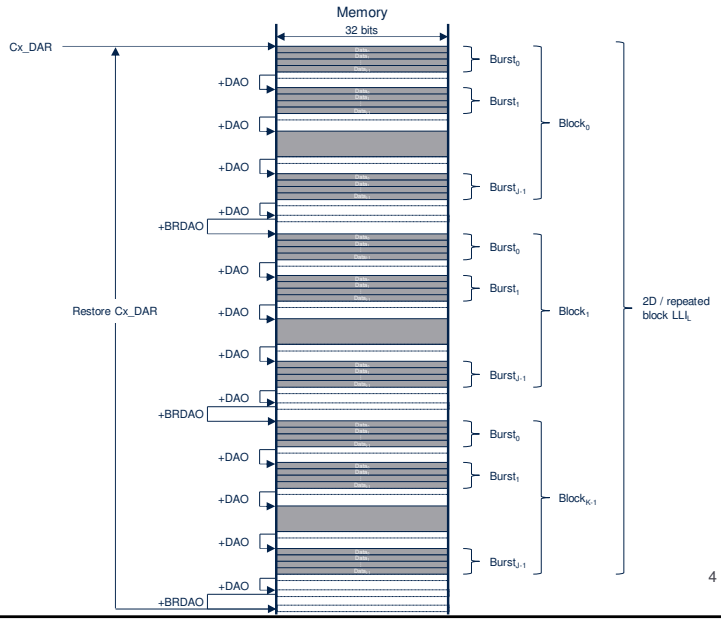
This figure highlights the repeated block mode and the stride between blocks.
This mode is useful for transferring the contents of a peripheral data register, typically an input FIFO, to non-contiguous buffers in memory.
After filling a block of N words, the DMA channel automatically adds the BDRA0 signed offset to the current address, jumping to the next buffer in memory.
At the end of the transfer, when K blocks will have been transferred, the Cx_DAR register, which points to the beginning of the first buffer, can be automatically restored, in order to implement circular buffers.
This automatic restoration requires a link operation.
In this example, bursts are placed contiguously in memory so the burst destination address offset (the

BDAO field of the Cx_TR3 register) must be null. For performances, destination transfers can be programmed as 4-word bursts.

2D addressing mode (continuous) (de)interleaving data/channels GP ch12-15

- Example: non-contiguous bursts within a block
  - Burst: I words
  - Block: J bursts
  - LLI: K blocks

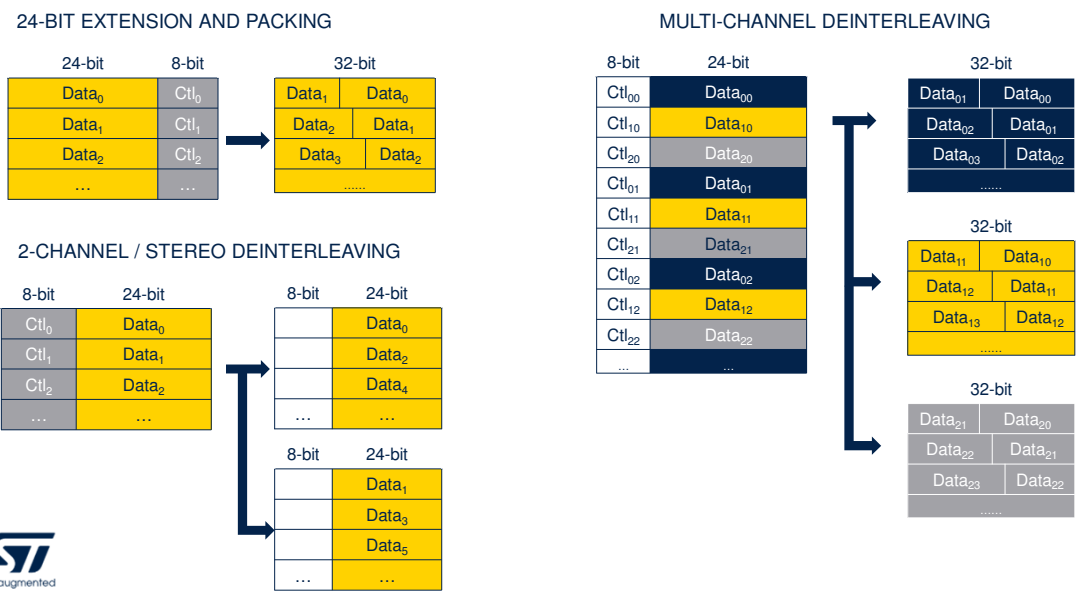




4

This figure highlights the repeated block mode, with the stride between bursts and the stride between blocks.
The GPDMA transfers K blocks of J bursts, each burst containing I words.
The stride between blocks is useful for transferring the contents of a peripheral data register, typically an input FIFO, to non-contiguous buffers in memory.
The stride between bursts is useful for interleaving or deinterleaving data and also for aligning data. Some use cases will be described in the next slide.

2D addressing mode
GP ch12-15



The first use case of burst stride is 24-bit extension and packing.
A source buffer contains data and control pairs. GPDMA channels 12 to 15 are capable of extracting the data field and packing the resulting 24-bit data back-to-back in the destination buffer.
A burst address offset of +1 byte and a burst length of 3 bytes can be programmed for the source.
No burst stride is requires on the destination. The destination can be programmed as a 4-word burst for best write performance.

The second use case consists in deinterleaving stereo audio samples into two separate buffers, one containing the right samples, the other the left samples.

There are several possible implementations.
One can be based on 2 GPDMA channels, one for the left samples, one for the right samples.
Then if the source buffer contains 2xN samples, the left/even samples may be read by a programmed source 1-word burst, with a source burst address offset of 4, and a source block size of 4xN bytes. And the destination can be programmed as a 4-word burst for best write performance.

An alternative implementation can allocate a single GPDMA channel.
A source with a burst of 1 word and a (source) burst address offset of +4.
A source with 2 blocks (i.e. BRC=1), one (source) block being 2x N bytes.
A destination with 4-word burst optimized writes, optionally with a (destination) block address offset.

In the last use case, data is deinterleaved and packed into 3 buffers. This could deinterleave the color components of RGB pixels.
Similarly, a single channel or 3 channels can be used.

Thank you

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In addition to this presentation, you can refer to the other presentations on the GPDMA and LPDMA:

- DMA overview
- DMA transfers hardware and software views
- Autonomous DMA & low power mode
- DMA Circular buffering & double buffering
- DMA Register file
- DMA Error reporting
- DMA Linked list
- DMA Input-output LLI control.