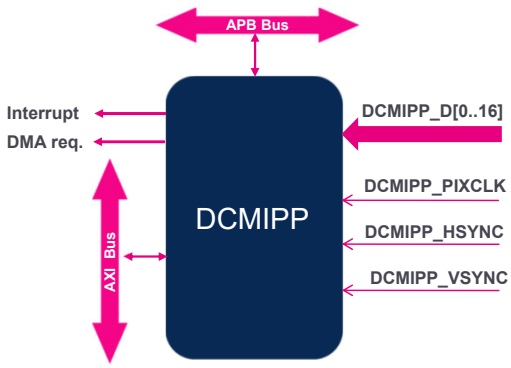
Hello, and welcome to this presentation of the STM32 digital camera interface pipe processing. It covers all features of this interface

Overview



- The DCMIPP provides a communication interface with external parallel camera sensor module (up to 16-bit data)
  - Configurable data formats
  - Continuous or snapshot capture mode
  - Crop and decimation features
  - AXI Master to speed-up data extraction to memory

Application benefits

- High-speed uncompressed image capture
- Compressed images in JPEG format capture

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DCMIPP stands for Digital Camera Interface Pipe Processing. The DCMIPP interface is used to connect a parallel camera module to the product. The camera generates a parallel data flow together with a pixel clock signal (DCMIPP_PIXCLK) which allows the interface to capture the incoming data flow. Two optional signals (HSYNC and VSYNC) may be used to synchronize the image frame between the camera and the product. The DCMIPP supports also embedded line/frame synchronization code in the data flow.

The DCMIPP allows to perform continuous grabbing. This process starts on application request and continues until the CAPTURE bit is cleared. Alternatively, Snapshot mode allows to capture a single frame upon an application request.
With the crop feature, the camera interface can cut and store a rectangular portion of the received image.
The decimation allows to reduce the picture resolution in both

direction X and Y independently.

Embedded AXI master module allows to transfer the data to the targeted memory for further processing operation (image processing functions or display purpose), without any external DMA or CPU operations).

Key features

Flexible operating modes to efficiently support most of // camera sensors

- 6-, 8-, 10-, 12-,14 or 16-bit parallel interface
  - Pixel rate : 120 Mpixels/s with a clock line DCMIPP_PIXCLK max at 120 MHz
  - Max pipe resolution : 5 Mpx at 15 Fps with a maximum at 4094x4094 with degraded Fps
- Supports the following data formats:
  - 8/10/12/14-bit progressive scan (monochrome/raw Bayer)
  - YUV422, YUV444
  - RGB 565, RGB888 progressive video
  - Others format like RGB444, RGB555, RGB666, Raw6, Raw7 may be processed like 8bpp or 16bpp or 24bpp by replicating sensor MSB pins to input missing LSB pins of DCMIPP
  - Compressed data: JPEG

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The camera interface has a configurable parallel data interface from 8 to 16 data lines, together with a pixel clock line DCMIPP_PIXCLK with a programmable polarity, rising/falling edge configuration and a maximum DCMIPP_PIXCLK of 120MHz. So this camera interface can achieve a data transfer rate up to 240 Mbyte/s using a 120 MHz pixel clock and 16-bit of data (2 pixels by data transfer in 8-bit data format or Jpeg thanks to external bridge for instance to speed-up the rate).
It supports color or monochrome cameras using different data formats:

- Uncoded parallel data – also known as progressive scan, which can be either monochrome or color (raw Bayer)
- Luminance/color coded on 8-bit (4/2/2 or 4/4/4 progressive scan)
- RGB 565, RGB888 – red-green-blue information coded on 16-bit or
- Some cameras also use this parallel interface to transmit

compressed images in JPEG format

Key features

Flexible operating modes to efficiently support most of camera sensors

- Snapshot or continuous capture mode
- Crop and decimation with pure sampling ratio 1vs1,2,4,8.
- AXI master to drain out pixel/data from internal FIFOs to accept external memory latencies
- Double buffer mode capability (DBM)
- Sensor statistics data extraction
- Overrun Detection to notify Pixel congestion within the pipe.

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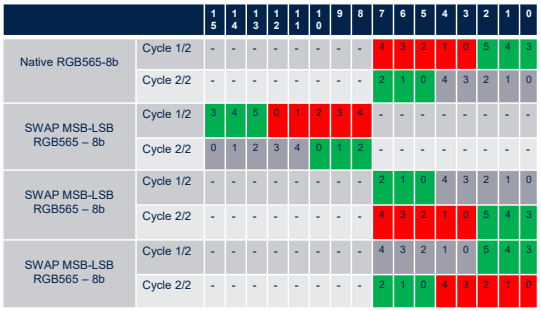
DCMIPP embeds an AXI master bus to drain all the valid data captured into the pipe from the internal FIFO to the targeted memory with the capability to handle double buffer mode (DBM). This last mode will be synchronized with the start of frame.
The pipe is also named pipe dump, since it does not really handle complex image processing operations, but more data dump without real transformation from the camera sensor data flow.
Thanks to the crop registers, it is possible to filter out statistics if these lasts are located from the first line till line x and or from the line y till the end of frame.
As already mentioned, the capture can be done in snapshot mode, meaning a single frame, or in continuous mode.
Decimation and crop operations are stand for reducing the image resolution and to extract only a part of the picture. Crop area is defined by a square or a rectangle.

Parallel interface

16-bit per pixel managed in one DCMIPP_PIXCLK cycle

- HV synchronization
  - HSYNC/VSYNC managed by physical IO
  - HSYNC/VSYNC coded into the the data flow (CCIR601)
- Flexible input
  - MSB can be swapped with LSB bits to ease PCB placement
  - For 2 cycles long pixel, cycle 0 and cycle 1 may be swapped



		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Native RGB565-8b	Cycle 1/2	-	-	-	-	-	-	-	-	4	3	2	1	0	5	4	3
	Cycle 2/2	-	-	-	-	-	-	-	-	2	1	0	4	3	2	1	0
SWAP MSB-LSB RGB565 – 8b	Cycle 1/2	3	4	5	6	7	2	3	4	-	-	-	-	-	-	-	-
	Cycle 2/2	0	1	2	3	4	0	1	2	-	-	-	-	-	-	-	-
SWAP MSB-LSB RGB565 – 8b	Cycle 1/2	-	-	-	-	-	-	-	-	2	1	0	4	3	2	1	0
	Cycle 2/2	-	-	-	-	-	-	-	-	4	3	2	1	0	5	4	3
SWAP MSB-LSB RGB565 – 8b	Cycle 1/2	-	-	-	-	-	-	-	-	4	3	2	1	0	5	4	3
	Cycle 2/2	-	-	-	-	-	-	-	-	2	1	0	4	3	2	1	0

- Wide input pixel formats sampled in single, double or triple-cycle data

IO Pin	1 cycle	2 cycles	3 cycles
Byte	X	-	-
Raw 8	X	-	-
Raw 10	X	-	-
Raw 12	X	-	-
Raw 14	X	-	-
Monochrome 8	X	-	-
Monochrome 10	X	-	-
Monochrome 12	X	-	-
Monochrome 14	X	-	-
RGB 565 -16b	X	-	-
PCB sensor444 to DCMIPP RGN565	X	-	-
PCB sensor555 to DCMIPP RGN565	X	-	-
RGB565 - 8b	-	X	-
RGB888 – 12b	-	X	-
RGB888 -8b	-	-	X
PCB sensor RGB666 to RGB888	-	-	X

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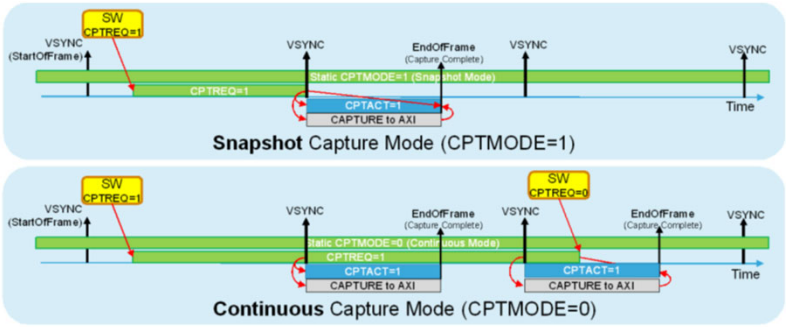
HSYNC and VSYNC synchronization signals can be connected by hardware connecting the physical signals from the camera sensor to the DCMIPP. In addition, these synchronization signals may also be software and embedded into the camera data flow (CCIR601 compliancy).
The input formats handled by the DCMIPP are wide and may be based on 1 pixel clock cycle for the pixel capture (it also could be 2, or even 3 clock cycles depending on the input data format). The DCMIPP offers possibility to swap the cycle in input in order to increase compatibility with camera sensors having some particular data order. It also allows to swap data from MSB to LSB to ease the PCB development if it is more convenient to map the parallel camera outputs to the DCMIPP physical parallel input. These two last features are only possible with a data format requiring 2 clocks cycles to capture 1 pixel.

DCMIPP capture modes

Flexible capture modes

- The DCMIPP interface supports two types of capture
  - Snapshot mode (single frame captured)
  - Continuous grab



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The DCMIPP allows to capture only the needed frames depending on the application. It is a way to optimize the memory accesses, AXI bus occupation and also power consumption. The applicative software may request to get continuous frame from the camera sensor, or only one frame in snapshot mode. These two differents modes are selected thanks to the bit CPTMODE inside the register DCMIPP_P0FSCR register.

In continuous mode, the frames will be processed continuously by the DCMIPP. The software needs to arm the bit CPTREQ = 1, and the next VSYNC will trig the data acquisition until the de-assertion of this bit. The bit CPTACT remains high indicating this continuous mode operation.

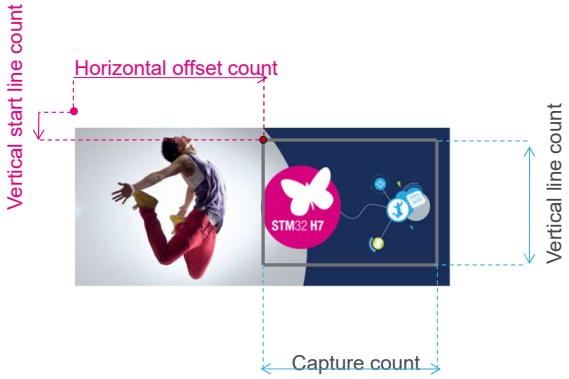
In snapshot mode, the software trigs the bit CPTREQ to launch the acquisition from the next start of frame for a single frame only. The bit CPACT remains high only for one frame. It is de-asserted at the end of the active frame. At the same time,

the bit CPTREQ is cleared by hardware to be ready for the future request, some others snapshot acquisitions, or even continuous one after modifying CPTMODE bit in such case.

DCMIPP Crop/Decimation features

Capturing only what needed

- The DCMIPP can select a rectangular window from the received image
  - The window size and coordinates are specified by two 32-bit registers DCMIPP_P0SCSTR and DCMIPP_P0SCSZR.
  - The size and position of the window is specified in number of data bytes (horizontal dimension) and in number of lines (vertical dimension)
- DCMIPP decimation block reduces the image resolution
  - Vertically : All line captured or 1 out of 2
  - Horizontally : all bytes, or 1 data out of 2 or 1 byte out of 2, or 2 bytes out of 4 (YUV)



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Cropping is another way to reduce the image size, in addition to reducing the pixel resolution as mentioned previously. This option is valid for both single frame capture and in continuous mode, but it is not supported for JPEG format.
Decimation allows to reduce the image size in both direction, in order to help for having smaller image for neural network for instance, in conjunction with the Crop feature.

DCMIPP counters

Memory protection and frame identification

- Dump counter:
  - Goal : Limit the number of 8-bit words to be received within a frame to protect memory allocation
  - 26-bit counter saturates at 0x03FF_FFFF
  - 32-bit words LIMIT set in configuration register. The counter continues to count even if the limit is reached to know how much data has been rejected
  - Interrupt generated when the limit has been reached.
- Frame counter:
  - 32-bit counter to identify frame as tag purpose with a loop time around 4.5 years @ 30 fps.

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The DCMIPP offers the capability to count the number of 8-bit data dumped within a frame for input data format with unkown length, like the JPEG for instance. It avoids to dump greater number of data which would compromize memory integrity if the reserved area for the dump is smaller than the number of data under capture. The limit is fixed by the software into the register DCMIPP_P0DCLMTR register. The granularity is 8-bit data. When reaching the limit, an interrupt may be generated to inform the software that the data after the limit will be rejected and so the frame will not be complete in acquisition. The counter is still incremented after the limit crossing to inform about the number of data which have been kicked off. The counter saturates at 0x03FF_FFFF.
The DCMIPP also proposes a way to know the frame tag number thanks to a 32-bit counter allowing to identify a frame with an unique ID until 4.5 years at 30 Frames Per Second.

DCMIPP Output pixel format

Multiple output formats with memory

- No format conversion into the pipe, only padding operations performed to optimize software processing from memory storage

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte/mono/Raw 8 bpp	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Pixel N+3								Pixel N+2								Pixel N+1								Pixel N							
PAD = 0 Mono/Raw 10 bpp							9	8	7	6	5	4	3	2	1	0							9	8	7	6	5	4	3	2	1	0
	Pixel N+1																						Pixel N									
PAD = 0 Mono/Raw 12bpp					11	10	9	8	7	6	5	4	3	2	1	0					11	10	9	8	7	6	5	4	3	2	1	0
	Pixel N+1																						Pixel N									
PAD = 0 Mono/Raw 14 bpp			13	12	11	10	9	8	7	6	5	4	3	2	1	0			13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pixel N+1																						Pixel N									
PAD = 1 Mono/Raw 10 bpp	9	8	7	6	5	4	3	2	1	0							9	8	7	6	5	4	3	2	1	0						
	Pixel N+1																						Pixel N									
PAD = 1 Mono/Raw 12bpp	11	10	9	8	7	6	5	4	3	2	1	0					11	10	9	8	7	6	5	4	3	2	1	0				
	Pixel N+1																						Pixel N									
PAD = 1 Mono/Raw 14 bpp	13	12	11	10	9	8	7	6	5	4	3	2	1	0			13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	Pixel N+1																						Pixel N									
RGB/YUV 16 bpp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pixel N+1																						Pixel N									
RGB/YUV 24 bpp Words 0 to 2	7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pixel N+1																Pixel N															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
	Pixel N+2																Pixel N+1															
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16
	Pixel N+3																								Pixel N+2							

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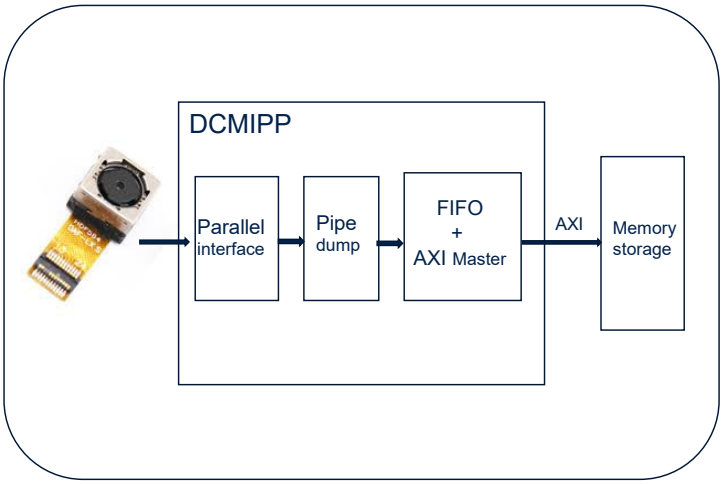
There is no format conversion handled by the pipe dump. The format in input is the same on the output. Only some padding operations are done on 10/12/14 bpp (Bit Per Pixel) Raw format in order to ease software processing from the data stored into the memory.

DCMIPP AXI master

Embedded AXI master to speed-up data storage in memory

- Single client on AXI to drain out data from the pipe to the memory for further processing
- No need to have system DMA resource to store data from the camera sensor
- Bus bandwidth performance and speed up data transfer on AXI Bus



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The DCMIPP integers a FIFO connected to the output of the pipe in order to absorbe the memory latency linked to the product platform (MPU or MCU). The AXI master drain out directly the data from the FIFO to the memory storage (external or internal memories) thank to the addresses configured into the DCMIPP pipe configuration registers (DCMIPP_P0PPM0ARx). The double buffer mode is proposed in order to store each data frame in a different memory location using address swapping technic. It is useful to process one buffer whereas the incoming data are stored into another one.

As the DCMIPP has its own AXI master functional block, there is no need to reserve system DMA feature to fill up the function to drain the data from the pipe to the memory storage. It is a mean to preserve system DMA ressources and also to speed-up the data transfer reducing bus arbitration mechanism and bus conflicts.

Performance

Equivalent Pixel Clock

- Relationship between Camera resolution and Pixel clock.
  - Maximum pixel clock DCMIPP_PIXLCK : 120 MHz with a DCMIPP kernel clock ratio greater or equal to 1
  - Camera resolution : 5Mpix @15fps => 75 Mpix/s
    - Considering as best 1 clock cycle per pixel
    - Nb of pixel by frame + blanking phase (considering worst case at 33%)
      - 75Mpix x 1.33 = 99.75 Mpix/s equivalent

        ⇒ DCMIPP_PIXCLK = 100 MHz
  - Camera resolution : 3Mpix @30fps => 90 Mpix/s
    - Considering the blanking phase about 33% max, the maximum pixel clock would be 120MHz according to the above formula

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The DCMIPP offers a connection to camera sensor having 5 Mpix (Mega Pixel) resolution considering 15 frame per second max and 1 clock cycle per pixel. He camera resolution may be greater but considering a lower frame per second rate. The limitation for the camera sensor is linked to the size of the counters used for the cropping operations (4094 pixel in vertical direction, and 4094 32-bit data in horizontal direction). Higher camera resolution may be connected but reducing the number of FPS (Frame Per Second) in order to satisfy the maximum input frequency on the pixel clock. The DCMIPP is able to process data from a 3MPix (Mega Pixel) camera sensor resolution at 30 FPS (Frame Per Second).

Interrupts

Multiple interrupt sources to handle the software application

Interrupt event	Description
IT_LINE	Indicates the end of the selected line
IT_FRAME	Indicates the end of frame capture
IT_OVR_PIPE	Indicates the overrun of data reception in the pipe
IT_VSYNC	Indicates the synchronization frame
IT_ERR	Indicates the detection of an error in the embedded synchronization frame detection
IT_LIMIT	Indicates that the received volume of data is greater than the maximum allowed

- DCMIPP interrupt is the logical OR of previous interrupts

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The DCMIPP contains 6 interrupts to warm the software for reacting to some applicative situations. The interrupt sources are splitted in two parts, the ones linked to the parallel interface, and the other ones linked to the pipe itself.
All the interrupts are Ored in a global interrupt to go to the product interrupt controller.
The 6 interrupt sources are :

- An overrun interrupt coming from the pipe dump including the output FIFO connected to the AXI master.
- An error interrupt condition when there is an error in the synchronization signal
- A start of frame interrupt line based on VSYNC detection (hardware or embedded one in the data flow)
- An end of frame condition which is generated at the end of the last data of a frame dumped from the pipe.
- A line reached condition when the frame reaches the selected line within a frame

- A limit reached from the dump counter to mention that the volume of data is greater than the maximum allowed (configurable by the software)

All of those interruptions are active or not, depending on the state of their respective enable bits.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

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Here is an overview of the status of the DCMIPP module in each of the low-power modes.
DCMIPP operations are not possible when the device is in Stop or Standby mode.

Related peripherals

- Refer to these peripheral training modules linked to this peripheral:
  - RCC (DCMIPP clock control, DCMIPP enable/reset)
  - Interrupts (DCMIPP interrupt mapping)
  - GPIOs (DCMIPP input connected to the external camera sensor)

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You can refer to the training slides related to RCC, interrupts and GPIOs for additional information.

Thank you

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