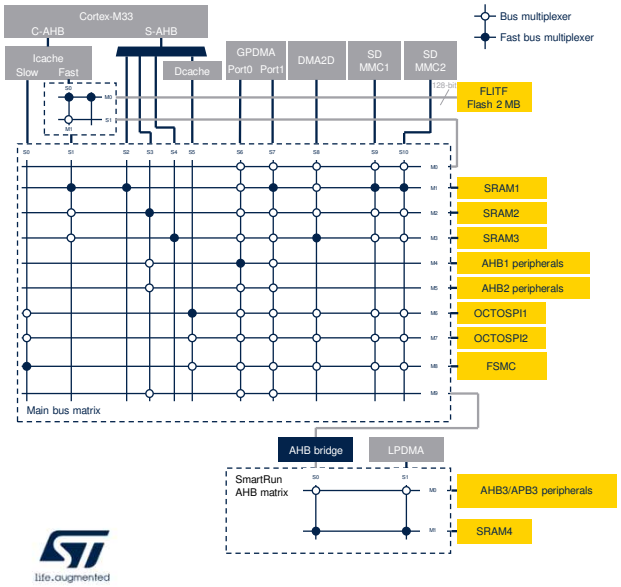
Hello, and welcome to this presentation of the bus matrixes interconnecting masters and slaves in the STM32U5.

Bus matrixes overview



- **Main Bus matrix**:
  - 32-bit multi-AHB bus matrix
  - Made up of 11 AHB slave interfaces (Si) + 10 AHB master interfaces (Mi)
- **Cache re-fill Bus matrix**
  - 128-bit Bus matrix
  - Made of **2 AHB 128-bit** interfaces (1 master + 1 slave) and **2 AHB 32-bit** interfaces (1 master + 1 slave)
- **SRD Bus matrix:**
  - 32-bit Bus matrix
  - Made of 2 AHB slave interfaces + 2 AHB Master interfaces

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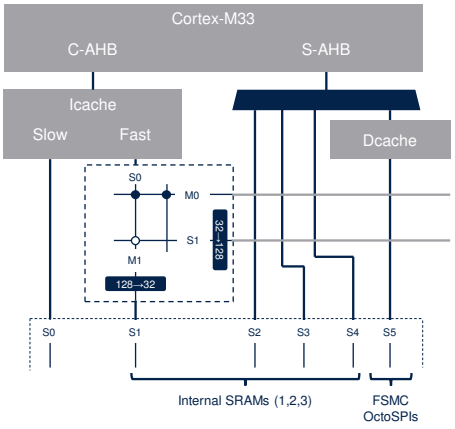
The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.
The STM32U5 Arm® Cortex®-M33 core is optimized for execution thanks to an instruction cache with direct access to Flash through the fast master port.
The main 32-bit AHB5 multilayer bus matrix, in the center of the figure, interconnects 11 masters and 10 slaves.
The 128-bit AHB5 instruction cache refill bus matrix is made up of two 128-bit interfaces and two 32-bit interfaces.
The 128-bit interfaces are the Slave 0 port connected to the instruction cache and the Master 0 port to the flash memory interface or FLITF.

The 32-bit interfaces are the Slave 1 port connected to the main bus matrix, enabling accesses to the flash memory, and the Master 1 port connected to the main bus matrix.
The 32-bit AHB5 Smart Run Domain or SRD bus matrix has two slaves interfaces (main matrix and LPDMA) and two master interfaces (AHB3/APB3 peripherals and SRAM4).
These bus matrices feature a fast bus multiplexer used to connect each master to a given slave without latency. For the same master, other slaves undergo a latency of at least one cycle at each new access.
You can see that a unique fat bus multiplexer is present in any particular column. It selects the default slave for the related master, which is accessed without latency, for instance the FSMC for the ICACHE slow port.

S-Bus



- **S-AHB interconnections (Internal Memories):**
  - Used to access data located in peripheral/SRAMs area
  - 3 Masters connected to internal SRAMs (SRAM1,2,3, SRAM4 and BKPSRAM)
  - For SRAM1,2,3: Zero latency
- **DCACHE S-AHB (external Memories)**
  - External memories are accessed through the data cache (FSMC, OCTOPSPIs)
  - Used for instruction fetch and data access to the external memories mapped in the data region
  - Fetching instructions through this bus is less efficient than fetching through the C-AHB bus and ICACHE slow port

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Accesses to internal SRAM memories initiated by the Cortex-M33 are performed through the S-AHB port. The demultiplexer connected to the S-AHB port selects the slave port in the main bus matrix according to the address:

- S2 in order to access the SRAM1
- S3 in order to access the SRAM2, SRAM4 and backup SRAM
- S4 in order to access the SRAM2.

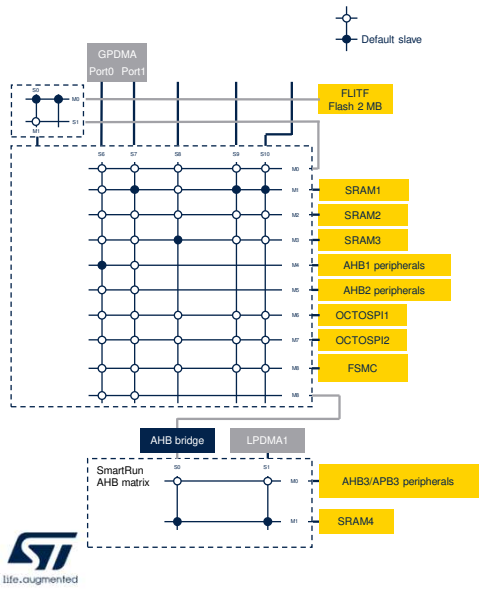
For SRAM1, 2, 3, latency is zero when no other master currently accesses the SRAM.

SRAM1, SRAM2 and SRAM3 are accessible on S-AHB bus with a continuous mapping.

Accesses to external memories connected to FSMC or OctoSPI controllers are done through the DCACHE, even

if requests are marked as non-cacheable.
These accesses can be data requests as well as instruction requests mapped in the external data region of the mapping.
Note that fetching instructions through the S-AHB and DCACHE is less efficient than fetching through the C-AHB bus and ICACHE slow port. This is the reason the ICACHE supports the address remapping capability.

GPDMA-bus



- **GPDMA-bus has:**
  - 2 AHB master interfaces to BusMatrix
- **GPDMA can access :**
  - Internal memories: Flash SRAM1,2,3,4 and BKPSRAM
  - external memories OCTOSPIs + FSMC
  - AHB1 peripherals including the APB1 and APB2 peripherals
  - AHB2 peripherals
  - SRD peripherals
- **Default Slaves:**
  - AHB1 peripherals port 0
  - SRAM1 port1

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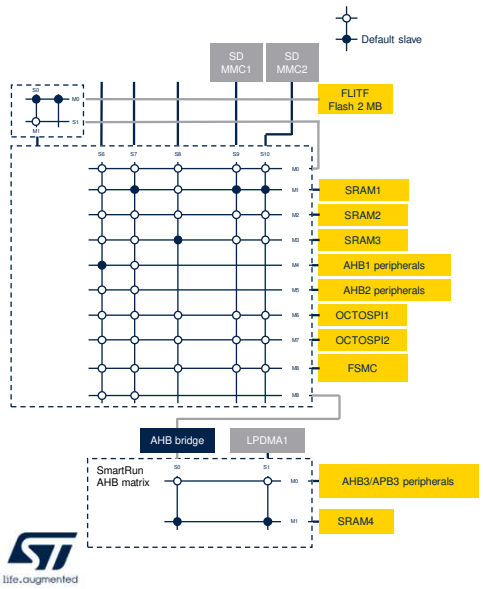
The GPDMA has a dual bidirectional master port: Port 0 and Port1, to support concurrent transfers over these ports.
Both master ports can access any memory-mapped resource in the microcontroller: internal and external memories, internal and external peripherals.
The port 0 is the default slave for AHB1 peripherals access.
The port 1 is the default slave for SRAM1 access.

SDMMC1 and SDMMC2 DMA controllers



- SDMMC1 and SDMMC2 DMA master buses interface the Bus matrix
- Used only by the SDMMC1 and SDMMC2 DMA to load/store data from/to the memory.
- These buses target the data memories:
  - Internal Flash memory
  - Internal SRAMs (SRAM1, SRAM2 and SRAM3)
  - External memories through FSMC or OCTOSPIs
- Default Slaves:
  - SRAM1 for both

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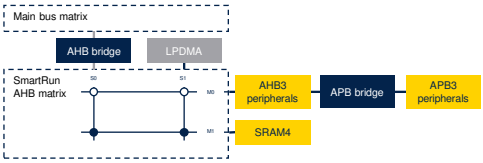
The SD and MMC controllers are master modules.
They can access any memory, internal or external, because data written to SD/MMC is read from buffers in RAM and data read from SD/MMC is stored buffers in RAM.
The default slave is SRAM1 for both controllers.

Smart run domain (SRD) bus matrix



- GPDMA is used only in CPU domain (when system clock is available)
  - GPDMA can access to all SRD slaves when system clock is available
- LPDMA has only access to SRAM4 and AHB3/APB3 peripherals
  - Relies on DMA allowing autonomous operations during LP modes down to Stop 2
- A 32-bit AHB bus matrix that interconnects:
  - 2 masters:
    - The main AHB bus matrix
    - LPDMA (low-power DMA featuring one master port)
  - 2 slaves:
    - AHB3 and APB3 peripherals
    - Internal SRAM4 (16 Kbytes)

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Some peripherals support autonomous mode. They remain active while the microcontroller is in a low power stop mode.
These peripherals generate a kernel clock request and an AHB/APB bus clock request when they need, in order to operate and update their status register even in Stop mode.
If the autonomous peripheral is configured with DMA requests enabled, a data transfer is performed thanks to the AHB/APB clock.
The autonomous peripherals mapped on AHB1, AHB2, APB1 and APB2, belong to the CPU domain, also called CD, and are autonomous in Stop 0 and Stop 1 only with the GPDMA and SRAM1, SRAM2, SRAM3 or SRAM4.

The main matrix belongs to the CD.
The autonomous peripherals mapped on AHB3 or APB3 belong to the SmartRun domain, also called SRD, and are autonomous in Stop 0, Stop 1 and Stop 2 with the LPDMA and SRAM4.
The LPDMA only has access to SRAM4 and AHB3/APB3 peripherals.

Arbitration

- Arbitration:
  - All Bus matrix arbitration schemes are round-robin
  - Start with lowest-numbered requestor
- Arbitration is done on allowed arbitration points
  - Any initiated burst should be finished before a new arbitration can occur
  - In the case of unspecified burst lengths, arbitration is done every 4 beats
- Each arbitration-change costs 1 clock cycle to be effective
  - Total latency in the case of a non-default slave = 1 cycle
- No latency in the case of a Default slave = 0 cycle

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The bus matrix manages the access arbitration between masters.
The arbitration uses a Round-Robin algorithm, which starts with the lowest-numbered requestor.
Arbitration is done on allowed arbitration points to ensure that bursts cannot be pre-empted.
This bus matrix features a fast bus multiplexer used to connect each master to a given slave without latency.
For the same master, other slaves undergo a latency of at least one cycle at each new access.

Thank you

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In addition to this presentation, you can refer to the following presentations:

- Instruction cache (ICACHE)
- Data cache (DCACHE)
- Power management (PWR)
- Reset and clock controller (RCC).