



Hello, and welcome to this presentation of the STM32U5  
Extended Interrupts and Events Controller.  
We will be presenting the features of the EXTI controller.

## EXTI

EXTI line	Line source	Line type
0-15	GPIO	Configurable
16	PVD output	Configurable
17	COMP1 output	Configurable
18	COMP2 output	Configurable
19	VDDUSB voltage monitor	Configurable
20	VDDIO2 voltage monitor	Configurable
21	VDDA voltage monitor 1	Configurable
22	VDDA voltage monitor 2	Configurable

- All events can wake up the system from Stop 0, 1, 2 modes.
  - Selectable active trigger edge
- No more “direct” lines from peripherals
  - Peripherals with wakeup capability request the AHB/APB clock
  - When the system clock is present, the peripheral generates an interrupt if enabled
  - The interrupt wakes-up the device, and is directly connected to NVIC
- Individual secure and privilege configuration for each event



life.augmented

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The extended interrupts and event controller (EXTI) manages the individual CPU and system wakeup through configurable event inputs.

It provides wakeup requests to the power control and generates an interrupt request to the CPU NVIC and events to the CPU event input.

The table provides the list of all the events supported by the STM32U5, that can wake up the system from Stop 0, 1, 2 modes.

Unlike previous versions of EXTI, the STM32U5 no longer supports direct peripheral events, that are generated by peripherals supporting interrupt requests.

Peripherals with wakeup capability request the AHB/APB clock and when the system clock is present, the peripheral

generates an interrupt if enabled. This interrupt wakes-up the device, and is directly connected to NVIC.

The EXTI is TrustZone aware. The access to control and configuration bits of secure input events can be made secured and or privileged. When a non-secure master attempts to access a secure resource, the EXTI illegal access is reported to the Global TrustZone controller, GTZC.

# Thank you

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Thank you for attending this presentation on EXTI.  
You can also refer to the following presentations for more information if needed:

- Arm Cortex-M33 core
- Nested Vectored Interrupt Controller (NVIC).