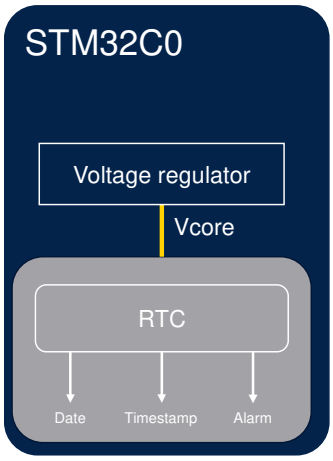
Hello, and welcome to this presentation of the STM32C0 Real-Time Clock. It covers the main features of this peripheral, which is used to provide a very accurate time base.

Overview



- The RTC provides an ultra-low-power hardware calendar with alarms
- As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status
- RTC events (Alarm, Timestamp) can generate an interrupt and wake the device up from the low-power modes

Application benefits

- Ultra-low power: 1.13 µA per MHz
- 300nA in stop mode
- Hardware BCD calendar to reduce software load

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2

The RTC peripheral features an ultra-low power calendar with alarm, which runs in sleep and stop modes.
As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status,
The RTC consumes only 1.13 µA per megahertz.
The hardware calendar is provided in binary-coded decimal (BCD) format to reduce software load, particularly when the date and time must be displayed.

Key features

- Sub-seconds, seconds, minutes, hours, week-day, date, month, year in BCD format
- On the fly programmable daylight savings compensation
- Programmable alarm with wakeup interrupt function
- A reference clock source (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit to achieve 0.954 ppm accuracy
- Timestamp feature which can be used to save the calendar content with sub-second precision (one event)
- When clocked by LSE, the RTC keeps on running under system reset if the reset source is different from the power-on reset one

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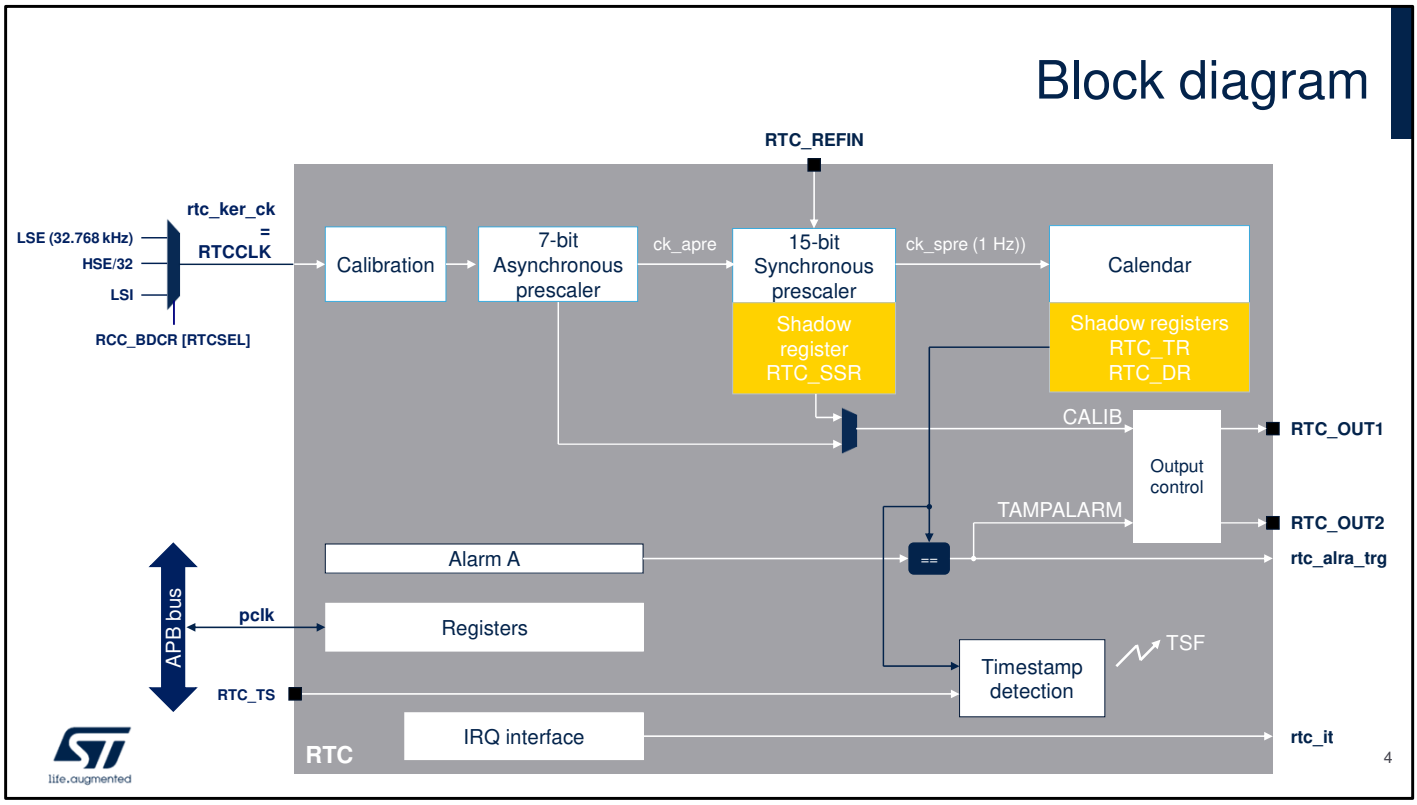
The key features of the RTC are:
Seconds, minutes, hours, week-day, date, month, and year, provided in binary-coded decimal format. Sub-seconds are provided in binary-coded decimal format.
Add or remove one hour on the fly to the calendar, in order to manage daylight savings.
One programmable alarm, which can wake up the microcontroller from sleep and stop modes.
The calendar can be calibrated thanks to a reference clock source which is the mains at 50 or 60 Hz.
A digital calibration circuit allowing compensation of the crystal accuracy, with 0.954 ppm resolution.
A timestamp function to save calendar contents in timestamp registers, depending on an external event.
Regarding reset events, the calendar shadow registers and some bits of the RTC status register are reset to their

default values by all available system reset sources.
The other registers, including the current calendar registers, are reset to their default values by a power-on reset and are not affected by a system reset.
In addition, when clocked by LSE, the RTC keeps on running under system reset if the reset source is different from one of the power-on.



Here is the RTC block diagram.
The RTC has two clock sources: the RTC clock (RTCCLK), used for the RTC timer counter, and the APB clock, used for RTC register read and write accesses.
The RTC clock can use either the high-speed external oscillator (HSE), divided by 32, the low-speed external oscillator (LSE), or the low-speed internal oscillator (LSI).
The RTC clock is first divided by a 7-bit programmable asynchronous pre-scaler, which provides the ck_apre clock. Most of the RTC is clocked at the ck_apre frequency, so, in order to reduce power consumption, it is recommended to set a high asynchronous division value. The default value is 128.
Then, a 15-bit programmable synchronous pre-scaler provides the ck_spre clock.
The ck_spre clock must be 1 Hz in order to update the

time and date BCD registers in 1-second increments.
The sub-second register resolution is defined by the ck_apre frequency. By default, it is 256 Hz when the RTC clock frequency is 32768 Hz. The SSR register resolution is increased by reducing the asynchronous prescaler value.
The asynchronous prescaler can also be bypassed; in this case the sub-second register resolution is defined by the RTC clock frequency.
Current calendar is saved into timestamp registers when a programmable edge is detected on RTC_TS input.
When the current data becomes equal to the time programmed in Alarm A, an alarm event occurs, which can be routed to an RTC_OUT pin.
The 512 Hz or 1 Hz clock can be driven on one of the RTC_OUT pins for calibration purposes.
In this figure, the shadow registers belong to the APB clock domain. This is explained later in this presentation.
Note that RTC_OUT1 and RTC_TS are mapped on the same pin.

RTC register write protection

Secure RTC initialization

- After Power-on reset, some of the RTC registers are write-protected
  - Writing to the protected RTC registers is enabled by writing a key into the Write Protection register, RTC_WPR
- Specific software sequence to enter RTC initialization mode
  - Used for calendar registers and prescaler initialization
  - By setting INIT bit to 1 in the RTC_ICSR register, initialization mode is entered
    - In this mode, the calendar counter is stopped and its value can be updated

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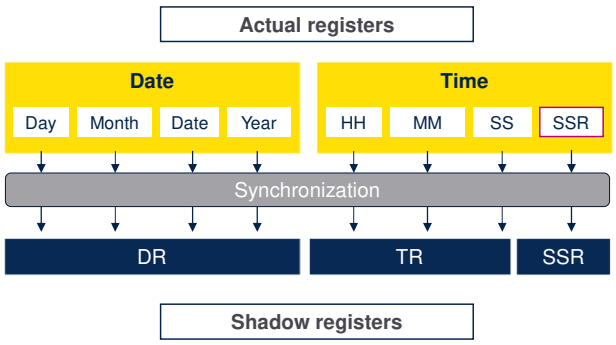
The RTC is initialized using a safe method.
The RTC registers are write-protected to avoid any possible parasitic write accesses.
A specific sequence must be written in the RTC write protection register.
Initialization mode must be entered in order to change the clock prescaler values or the calendar value.

RTC calendar

Active in all low-power modes, VBAT and reset

- Initialization done through shadow registers: time and date registers



- Reading the calendar:
  - BYPSHAD = 0: Read shadow registers
    - Delay up to 1 RTCCLK cycles to update shadow registers when exiting Stop/Standby/Shutdown modes.
    - Reading either RTC_SSR or RTC_TR locks the values in the higher-order calendar shadow registers until RTC_DR is read
  - BYPSHAD = 1: Bypass shadow registers
    - Calendar read directly accesses the calendar counters
    - Software must read all calendar registers twice and compare the results to ensure that the data are coherent and correct

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6

The RTC calendar keeps running in sleep and stop low-power modes, and during reset.
Initialization of the Time and Date registers is performed via their shadow registers, which belong to the APB clock domain. The sub-second register cannot be initialized.
Every RTCCLK period, the current calendar value is copied into the shadow registers
The calendar sub-second, time, and date registers content can be read in two different modes.
When the Bypass Shadow Registers control bit is cleared, the shadow registers are read. The advantage of this mode is that it guarantees that all three registers are consistent. Reading either RTC_SSR or RTC_TR locks the values in the higher-order calendar shadow registers until RTC_DR is read.
The disadvantage of this mode is that when exiting sleep

or stop mode, the software must wait for a synchronization delay to ensure that the shadow registers are updated with the last calendar register values. This synchronization delay can be up to four RTC clock periods. Also, to read the RTC calendar registers properly in this shadow mode, the APB1 clock frequency must be equal to or greater than seven times the RTC clock frequency.
When the Bypass Shadow Registers control bit is set, the actual calendar registers are read directly. The advantage of this mode is that there is no need to wait for the synchronization delay. The disadvantage is that the read values can be false or not consistent due to synchronization issues, so they must be read twice and compared with previous read values to ensure they are correct and coherent.

RTC calendar features

- Daylight savings is managed by automatic addition or subtraction of 1 hour
- Calendar synchronization up to 1 s by adding/subtracting an offset with the sub-second resolution
  - Allows synchronization with remote clock
- Reference clock detection: a more precise second-source clock (50 or 60 Hz mains) can be used to enhance the long-term precision of the calendar:
  - The reference clock is automatically detected and used to enhance the calendar precision
  - The LSE clock is automatically used to update the calendar whenever the reference clock becomes unavailable

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7

This slide presents the main calendar features.
Daylight savings can be managed by software, with automatic 1 hour addition or subtraction.
The RTC can be synchronized to a remote clock with a high degree of precision.
It is possible to synchronize the RTC clock to this remote clock by adding or subtracting an offset to the sub-second register on the fly, with ck_apre clock resolution.
This feature is commonly used in RF applications.
A reference clock, mains at 50 or 60 Hz, can be used to enhance long-term calendar precision.
The reference clock, connected to the RTC_REFIN pin, is automatically detected.
When the 1 Hz clock becomes misaligned due to the imprecision of the LSE clock, the RTC shifts the 1 Hz clock a bit so that future 1 Hz clock edges are aligned.

Thanks to this mechanism, the calendar becomes as precise as the reference clock.
When the reference clock is not available, the LSE clock is automatically used to update the calendar.

Smooth digital calibration

Crystal inaccuracy compensation

- Consists in masking/adding N (configurable) 32 kHz clock pulses, fairly well distributed in a configurable window
- Calibration value can be changed on the fly
- A 1 Hz output is provided to measure the crystal frequency and the calibration result

Calibration window	Accuracy	Total range
8 s	± 1.908 ppm	[-487.1 ppm, +488.5 ppm]
16 s	± 0.954 ppm	[-487.1 ppm, +488.5 ppm]
32 s	± 0.477 ppm	[-487.1 ppm, +488.5 ppm]

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8

The digital calibration is used to compensate crystal inaccuracy and accuracy variations with temperature and aging.
It consists in masking or adding a programmable number of RTC clock cycles, fairly well distributed in a configurable window.
The calibration value can be changed on the fly, depending on detected temperature changes for instance.
A 1 Hz calibration output signal is provided to measure the crystal frequency before and after applying the calibration value.
The accuracy shown here is the resolution of the digital calibration. The calibration window size is configurable, between 8, 16, and 32 seconds.
For a 32 second calibration window, the accuracy is plus or minus 0.477 ppm.

The total correction range is from -487 to 488 ppm.
The accuracy resolution scales with the calibration window size.
Final accuracy in the application will depend on the crystal parameter precision, temperature detection precision, how often the software calibration procedure is launched, etc.
In order to reach the precision of the calibration window, the measurement window must be a multiple of the calibration window.

RTC calendar features

- Timestamp
  - The calendar is saved in the timestamp registers when a timestamp event is detected on the RTC_TS pin
  - By setting the TSIE bit in the RTC_CR register, an interrupt is generated when a timestamp event occurs
- If a new timestamp event is detected while the timestamp flag (TSF) is already set, the timestamp overflow flag (TSOVF) flag is set

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9

A timestamp function is available: the sub-second, time, and date values are saved in timestamp registers when an event occurs on the timestamp I/O.
If a timestamp event occurs while the timestamp flag is set, the timestamp overflow flag is set.
In this case, timestamp registers maintain the timestamp of the previous event.

RTC programmable alarm

Flexible alarm based on calendar value

- The Alarm flag is set if the calendar sub-seconds, seconds, minutes, hours or date matches the value programmed in the alarm registers
  - An alarm causes the exit from sleep and stop low-power mode
- Alarm event can also be routed to the specific output pin RTC_OUT, with configurable polarity
- Calendar sub-second, seconds, minutes, hours or date fields can be independently selected (masked or not masked)
  - Masks allow configuration of periodic alarm interrupts

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10

The RTC embeds one flexible alarm, based on comparison with the calendar value.
The alarm flag is set if the calendar sub-seconds, seconds, minutes, hours or date matches the value programmed in the alarm registers.
The alarms events can wake up the device from sleep and stop modes.
The alarms event can also be routed to the specific output pin RTC_OUT, with configurable polarity.
The calendar alarm sub-second, seconds, minutes, hours or date fields can be independently masked or not masked for the comparison.
When the masks are used, periodic alarms are generated.

Interrupts

Interrupt event	Description
Alarm A	Set when the calendar value matches the Alarm A value
Timestamp	Set when a timestamp event occurs

- The event flags are in the RTC_SR register
- The interrupt masked flags are in the RTC_MISR register

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Two RTC events can generate an interrupt.
These interrupt events can wake up the microcontroller from sleep and stop modes.
The Alarm A interrupt is set when the calendar value matches the Alarm A value.
The timestamp interrupt is set when a timestamp event occurs.

Low-power modes

Mode	Description
Run	Active
Sleep	Active • RTC interrupts cause the device to exit sleep mode
Stop	Active when clocked by LSE or LSI • RTC interrupts cause the device to exit the stop mode
Standby	The RTC is powered down and must be re-initialized after exiting Standby mode
Shutdown	The RTC is powered down and must be re-initialized after exiting Shutdown mode

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The RTC peripheral is active in run, sleep, and stop modes
RTC interrupts cause the device to exit sleep and stop modes.
In stop mode, only the LSE or LSI clocks can be used to clock the RTC.
In standby and shutdown modes, the RTC is powered-down.

Differences with STM32G0

- The RTC implemented in STM32C0 is a subset of the RTC present in STM32G0:
  - STM32G0 has 2 alarms A & B
    - STM32C0 only supports Alarm A
  - STM32G0 has a tamper functionality integrated in the RTC module
    - STM32C0 does not implement a tamper unit
  - The RTC can remain active in standby and shutdown modes in STM32G0
    - This is not the case for STM32C0

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The RTC of the STM32C0 is a subset of the one present in the STM32G0.
Here are the features, which have been removed for cost and consumption reasons:

- The second alarm B
- The tamper unit
- The backup domain and therefore the capability of maintaining the RTC active in standby and shutdown modes.

Debug information

- DBG_RTC_STOP bit: RTC counter stopped when core is halted

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A bit is available in the MCU Debug interface, in order to stop the RTC counter when the core is halted for debugging.

Related peripherals

- Refer to these peripheral trainings linked to the RTC
  - Reset and clock controller (RCC)
  - Power controller (PWR)
  - Extended interrupt controller (EXTI)

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This is a list of peripherals related to the real-time clock. Please refer to these peripheral presentations for more information if needed.

- Reset and clock controller
- Power controller
- Extended interrupt controller

Thank you

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Thank you for attending this presentation!