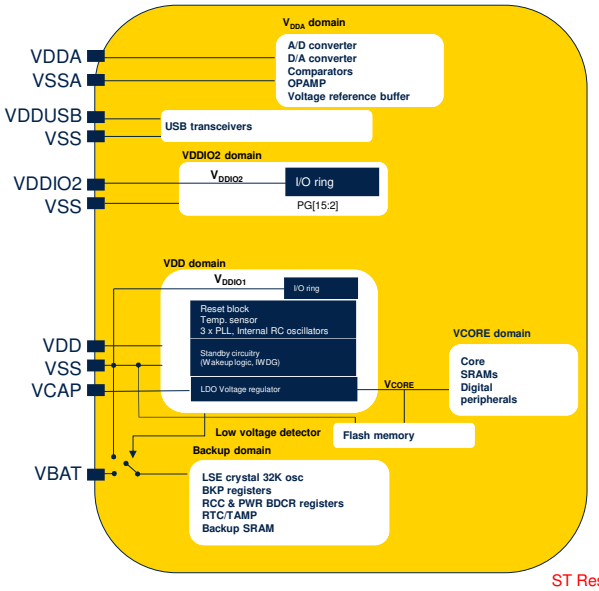
Hello, and welcome to this presentation of the STM32U5 power controller.
The STM32U5's power management functions and all low power modes are also covered in this presentation.

Power supplies – LDO devices

STM32U575xxxx and STM32U585xxxx

- Internal voltage regulator: LDO, requiring external 4.7 µF capacitor
- Independent power supplies:
  - VDD = 1,71V (at power-up) to 3,6 V, down-to BOR0 min around 1.58V
  - VDDA = 1,62 V (ADC, DAC, COMP, OPAMP)/ 1.8V (VREFBUF) to 3.6V
  - VDDUSB = 3 V to 3,6 V
  - VDDIO2 = 1,08 V to 3,6 V
  - VBAT = 1,58 V (BOR min) to 3,6 V



life.augmented

2

ST Restricted

STM32U5 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying almost all I/Os except those part of the VBAT domain and port G pads 15 down to 2.
VDD also supplies the flash memory, the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog.
The STM32U575xxxx and STM32U585xxxx microcontrollers only rely on integrated regulators.
VCORE supplies most of the digital peripherals, SRAMs and Flash memory controller.
VDDA voltage supplies the analog peripherals.

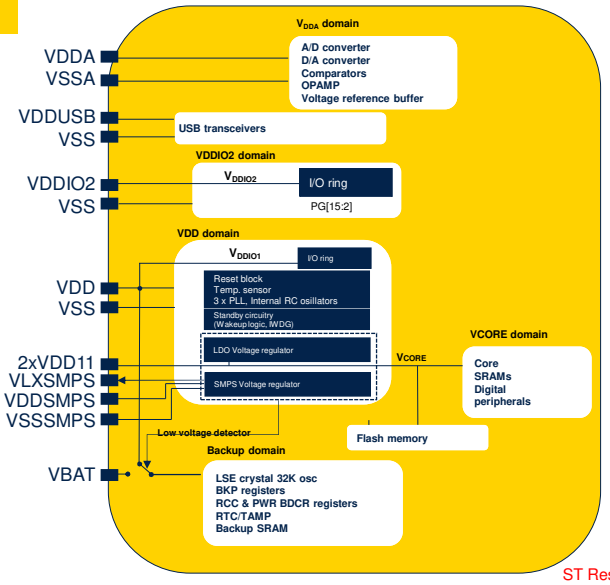
The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters.
It is also the output of the internal voltage reference buffer when enabled.
Additionally USB transceiver and Port G pins 15 down to 2 have their own independent power domains, powered respectively by VDDUSB and VDDIO2.
A backup battery can be connected to VBAT pin to supply the backup domain.

Power supplies – SMPS devices

STM32U575xxxxQ and STM32U585xxxxQ

- Internal voltage regulator: LDO and SMPS, requiring external 4.7 µF capacitor plus external 2.2 µH coil for SMPS
- VDDSMPS= 1,71 V to 3,6 V, must be on the same supply as VDD
- VLXSMPS: switched SMPS step-down converter output

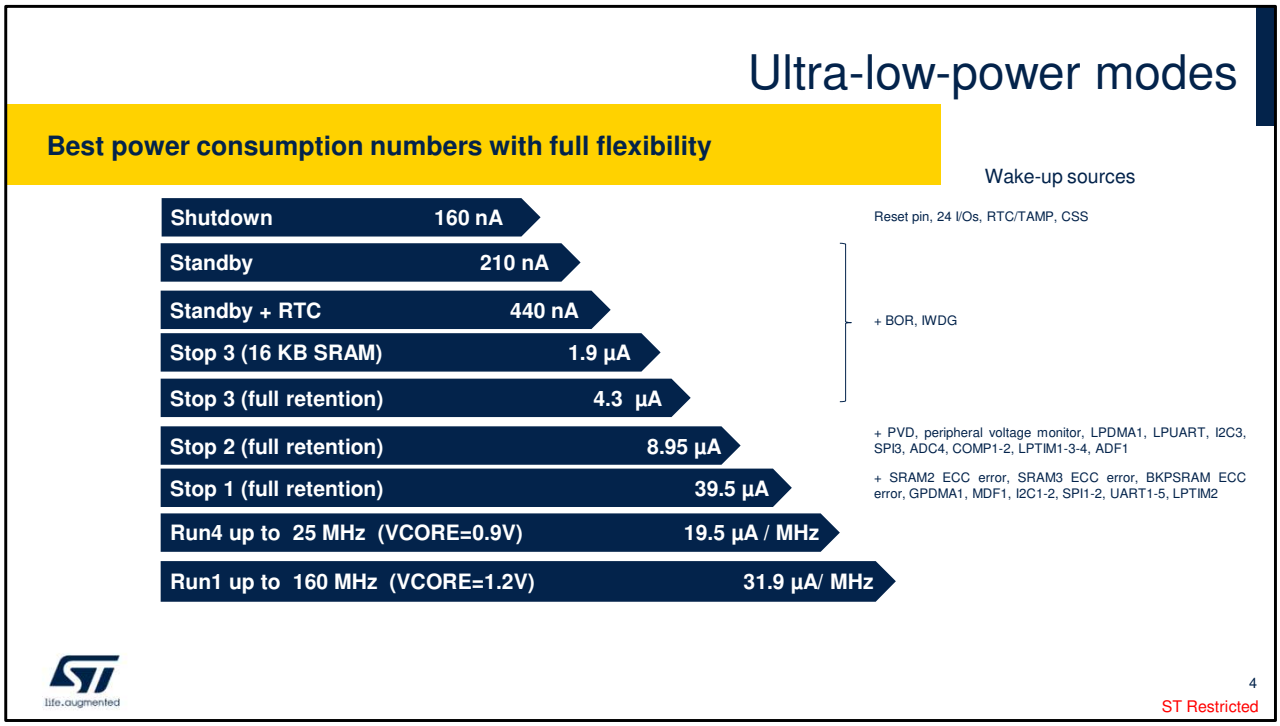
- **SMPS is designed for supplying only internal load (cannot be used for supplying external components)**



3

ST Restricted

The built-in Switched Mode Power Supply (SMPS) step down converter is a power-efficient DC/DC non-linear switching regulator that improves low-power performance. The SMPS generates the VCORE voltage on VDD11 (two pins).
Only STM32U575xxxxQ and STMU585xxxxQ support SMPS.



STM32U5 devices feature a flexible power control, which increases flexibility in power mode management and further reduces the overall application consumption.
This slide details the consumption in some of the power modes for the STM32U585 and the related wake-up sources.
The devices support dynamic voltage scaling to optimize their power consumption in Run mode. The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.
The consumption is even lower when frequency and voltage are decreased.
STM32U5 devices support 7 main low-power modes:

Sleep, Stop 0, Stop 1, Stop 2, Stop3, Standby and Shutdown modes.
Each mode can be configured in many ways, providing several additional sub-modes.
In addition, STM32U5 devices support a battery backup domain, called VBAT.
The high flexibility in power management provides both high performance with a CoreMark score equal to 4.07/MHz, together with an outstanding power efficiency.

BOR/PVD

- BOR and PVD similar to STM32L4/L5
  - 5 BOR thresholds, 7 PVD thresholds
  - In Standby modes, the BOR/PVD voltage reference can be set to “sampled mode” for lowest consumption (PWR_CR1[ULPMEN]=1) but with a high VDD falling minimum slew rate

- An additional BOR is embedded also on VBAT supply, in VBAT mode

	Min	Max	Unit
V(BOR_VBAT)	1.58	1.65	V

life.augmented

5

ST Restricted

A Brown-out reset (BOR) is implemented to ensure safe device operation even during power-on and power-down. This unit resets all registers except those in the backup domain powered by VBAT which contain the RTC and TAMP blocks and the external low-speed oscillator LSE. When exiting Standby mode, all registers powered by the Main regulator are reset.
When exiting Shutdown mode, a Power reset is generated. Five BOR levels can be selected through option bytes. During power-on, the BOR keeps the device under reset until the supply voltage VDD reaches the specified VBOR threshold.
The Brown Out Reset circuit is always On, except in shutdown mode.

During Standby modes, it is possible to set the BOR in ultra-low-power mode to further reduce the current consumption by setting the ULPMEN bit.
VBAT is the power supply for RTC, TAMP, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present. Functionality is guaranteed down to the VBOR_VBAT minimum value, which is 1.58V.

A Power Voltage Detector (or PVD) can generate an interrupt when VDD crosses the selected threshold. The PVD can be enabled in all modes except STOP3, Standby and Shutdown modes. The threshold is selected by software among seven possible values.
In addition, comparisons can be done between VREFINT and the PVD_IN external pin.
The STM32U5 also supports two new features to enhance the power supply supervision:

- Temperature threshold monitor
- Upper VDD threshold monitor.

Whenever these monitors detect an abnormal condition, they can generate an internal tamper event.

Independent power supplies

- After reset, all independent power supplies (VDDA, VDDUSB, VDDIO2) are logically and electrically isolated by default
  - Isolation must be removed by software before using the associated peripherals or I/Os
- Voltage monitors check if power is present
  - Rising edge and falling edge detection with EXTI, with wakeup from Stop capability

AVM1	AVM2	IO2VM	UVM
1.6 V	1.8 V	1.0 V	1.2 V

life.augmented

To improve ADC and DAC conversion accuracy and to extend the supply flexibility, the analog peripherals have an independent power supply that can be separately filtered and shielded from noise on the PCB.
The VDDA, VDDUSB and VDDIO power supplies can be independent from VDD and can be monitored with dedicated Peripheral Voltage Monitoring (or PVM).
The VDDA supply can be monitored by the analog voltage monitors (AVM), and compared with two thresholds (1.6 V for AVM1 or 1.8 V for AVM2).
The IO2 and USB have their own voltage monitors, respectively IO2VM and UVM.
Each PVM output is connected to an EXTI line and can generate an interrupt if enabled through the EXTI

registers.
After reset, these independent power domains are logically and electrically isolated and therefore are not available. The isolation must be removed before using the analog peripherals, by setting a control bit when the related power supply is present.

Internal voltage regulators

- SMPS and LDO are in parallel and can be selected on the fly during application
  - LDO: less noise
  - SMPS: better efficiency
- Support “Soft start mode” to limit inrush current after power-on reset

	FSTEN=0	FSTEN=1
	Limited inrush current : 10 mA	Fast start mode : 120 mA
PRO	Compatible with low drive current batteries	
CONS	High wakeup time	Faster wakeup time

  - Fast start mode:
    => Applied at next system reset or wakeup from low-power mode except Shutdown mode.
    ⇒ Not applied also when exiting VBAT mode or at next power-on.
- Regulator bypass mode is not supported

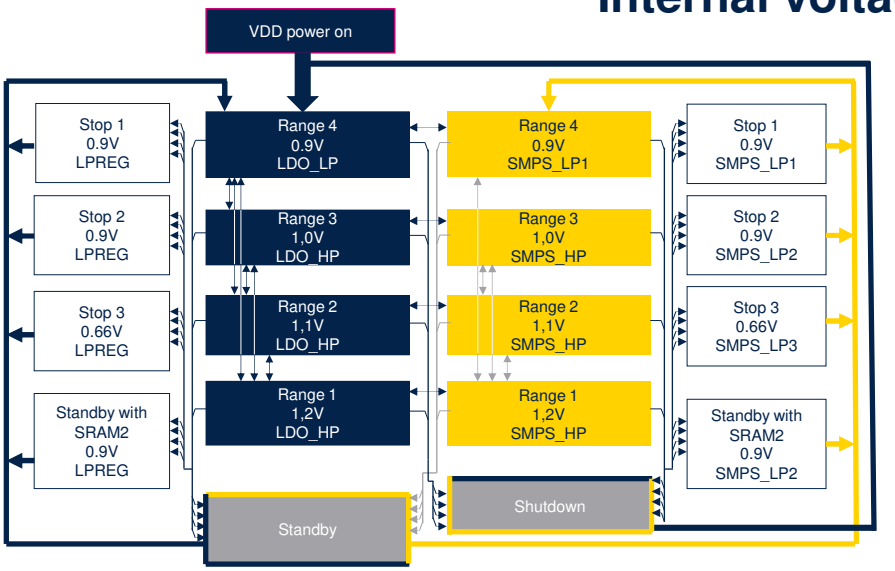
life.augmented

The devices embed two regulators: one LDO and one SMPS in parallel to provide the VCORE supply for digital peripherals, SRAMs (except Backup SRAM) and embedded Flash memory.
Both regulators can provide four different voltages, in order to implement dynamic voltage scaling, and can operate in Stop modes.
It is possible to switch from SMPS to LDO and from LDO to SMPS on the fly.
The SMPS allows the power consumption to be reduced but some applications can be perturbed by the noise generated by the SMPS, requiring the application to switch to LDO

The low-startup feature is selected to limit the inrush current after power-on reset. This increases the wakeup time when exiting Stop or Standby modes. However, it is possible to configure a faster startup on the fly applicable for next startup either after a system reset or wakeup from low-power mode except Shutdown and VBAT modes. The fast startup is selected by setting the FSTEN bit.

Using an external regulator to generate the VCORE power supply externally is not supported.

Internal voltage regulators



All power modes are supported with SMPS and LDO:

- Exit from Stop and Standby modes is done in the selected regulator, always in range 4
- Exit from Shutdown and boot from reset is always done on LDO

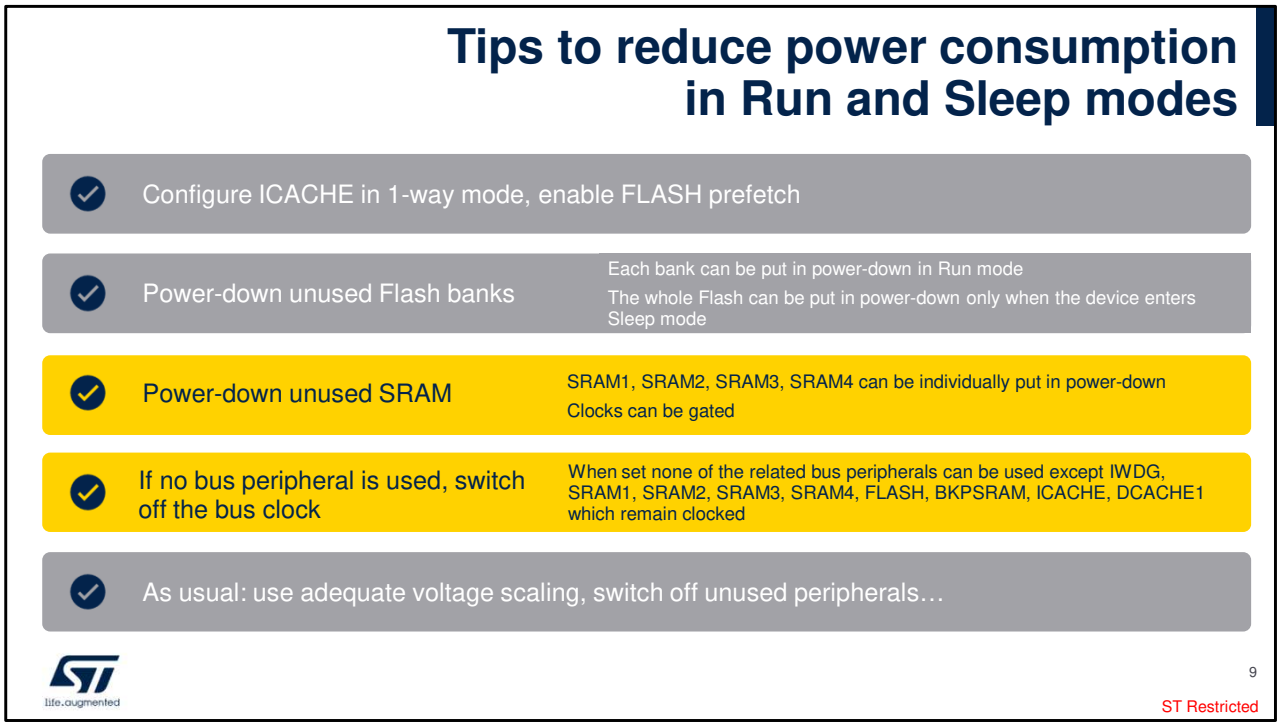
life.augmented

8

ST Restricted

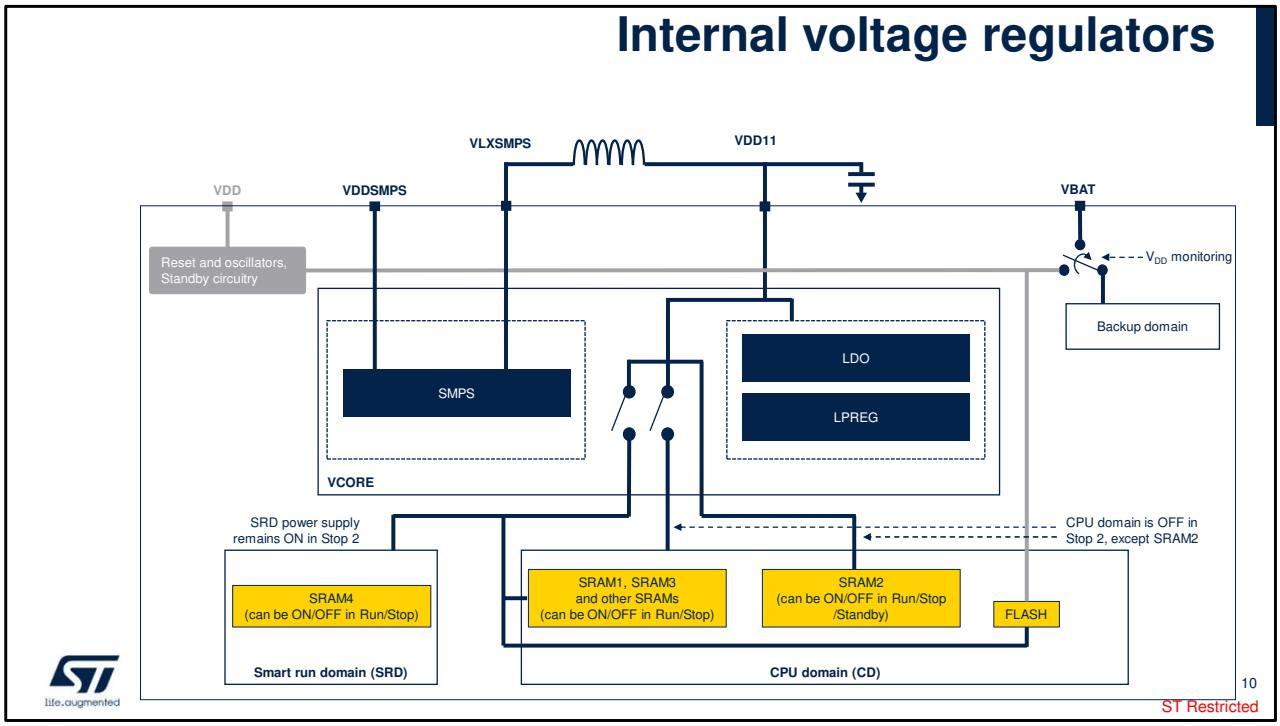
This figure represents all power states and the transitions between them.
The following regulators are implemented: LDO, SMPS and Low power regulator (LPREG).
The LDO and the SMPS regulators have two modes: Main regulator mode (used when performance is needed), and Low-power regulator mode.
LDO or SMPS can be used in all voltage scaling ranges, and in all Stop modes.
After reset, the regulator is the LDO, in range 4. Switching to SMPS provides lower consumption in particular at high VDD voltage. It is possible to switch from LDO to SMPS, or from SMPS to LDO in any range, by configuring the REGSEL bit.

When exiting the Stop or Standby modes, the regulator is the same as when entering low power modes. The voltage range is the range 4.
Exit from Shutdown is always done on LDO.



Here are some tips to reduce the power consumption in run and sleep modes.
By default, the instruction cache is a 2-way set associative cache. For applications needing a very-low-power consumption profile, it can be reconfigured as direct-mapped cache. In this case, no replacement algorithm is required.
After reset, both flash banks are in normal mode. In order to reduce power consumption, each bank can be independently put into power-down mode.
The whole flash can be put in power-down when the device enters Sleep mode.
Five SRAMs are embedded in the STM32U5 devices, each with specific features.

SRAM1, SRAM2, and SRAM3 are the main SRAMs. SRAM4 is in the SRAM used for Low-Power Background Autonomous Mode (LPBAM) peripherals in Stop 2 mode. These SRAMs are made up of several blocks that can be powered down in Stop mode to reduce consumption.
Internal AHB and APB bus clocks can be gated off when the peripherals connected to these buses are all unused. Memories and some modules such as caches and independent watchdog remain clocked when the bus clock is stopped.
Some peripherals support autonomous mode. These peripherals are able to generate a kernel clock request and an AHB/APB bus clock request when they needed, in order to operate and update their status register even in Stop mode.
As a general recommendation, the voltage range should be adapted to the target performance level and any unused peripheral should be switched off.



SMPS and LDO regulators provide, in a concurrent way, the VCORE supply depending on application requirements. However, only one of them is active at the same time.
When SMPS is active, it feeds the VCORE on the two VDD11 pins supplied by the filtered SMPS VLXSMPS output pin.
A 2.2 microhenrys and a 2.2 microfarad capacitor on each VDD11 pin are then required.
When LDO is active, it supplies the VCORE and regulates it using the same decoupling capacitors on the VDD11 pins.

The LDO and the SMPS regulators have two modes: Main

regulator mode (used when performance is needed), and Low-power regulator mode. LDO or SMPS can be used in any voltage scaling ranges, and in all Stop modes.

The SmartRun Domain (SRD) architecture relies on a DMA allowing autonomous operation during low-power modes down to Stop 2.
This power domain features a 32-bit AHB bus matrix that interconnects two masters: the main AHB bus matrix and the LPDMA1 and two slaves: AHB3 peripherals including AHB to APB bridge connected to APB3 and internal SRAM4.

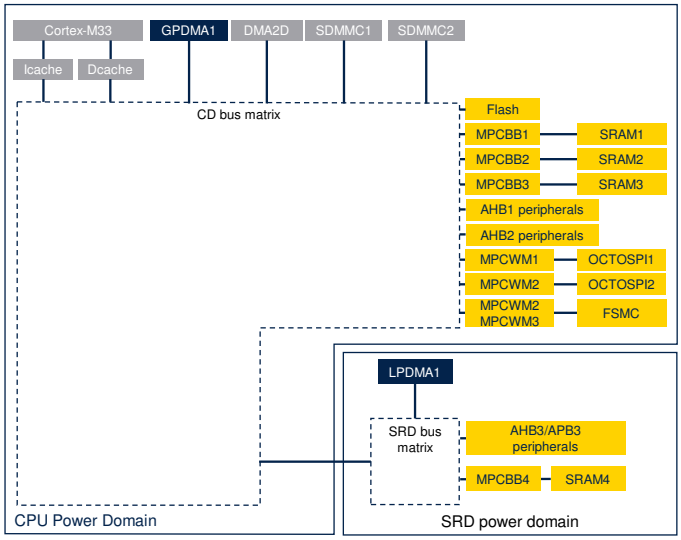
After entering Standby mode, SRAMs and register contents are lost except for registers and backup SRAM in the Backup domain and Standby circuitry. Optionally, the full SRAM2 or 8 Kbytes or 56 Kbytes can be retained in Standby and Stop 3 modes, supplied by the low-power regulator (standby with RAM2 retention mode).

The regulators are OFF in Standby and Shutdown mode.

To retain the content of the backup registers and supply the RTC function when VDD is turned off, the VBAT pin can be connected to an optional backup voltage supplied by a battery or by another source.
The VBAT pin powers the RTC unit, the LSE oscillator and the PC13 to PC15 I/Os, allowing the RTC to operate even when the main power supply is turned off.
The switch to the VBAT supply is controlled by the power down reset embedded in the Reset block.

VBAT also powers the backup SRAM when the main power supply is turned off.

CPU domain (CD) and Smart run domain (SRD)



- Stop 0 & Stop 1:
  - CD & SRD fully powered => all autonomous peripherals are functional, thanks to GPDMA1 and LPDMA1
- Stop 2:
  - CD in retention (lower leakage mode) => no dynamic activity possible
  - SRD fully powered => SRD autonomous peripherals are functional thanks to LPDMA1

life.augmented

11

ST Restricted

The devices support a Low-Power Background Autonomous Mode (LPBAM), that allows peripherals to be functional and autonomous in Stop 0, Stop 1 and Stop 2 modes. Autonomous means that no software runs to control these peripherals.
The autonomous peripherals mapped on AHB1, AHB2, APB1 and APB2, belong to the CPU domain, and are autonomous in Stop 0 and Stop 1 thanks to GPDMA1 and SRAM1, SRAM2, SRAM3 or SRAM4.
The autonomous peripherals mapped on AHB3 or APB3 belong to the SmartRun domain and are autonomous in Stop 0, Stop 1 and Stop 2 thanks to the LPDMA1 and SRAM4.
While in stop 2 mode, the CPU domain is not active,

however background tasks can be in progress in the SmartRun domain, including data movement thanks to the low power DMA.

Low-power modes: Stop modes

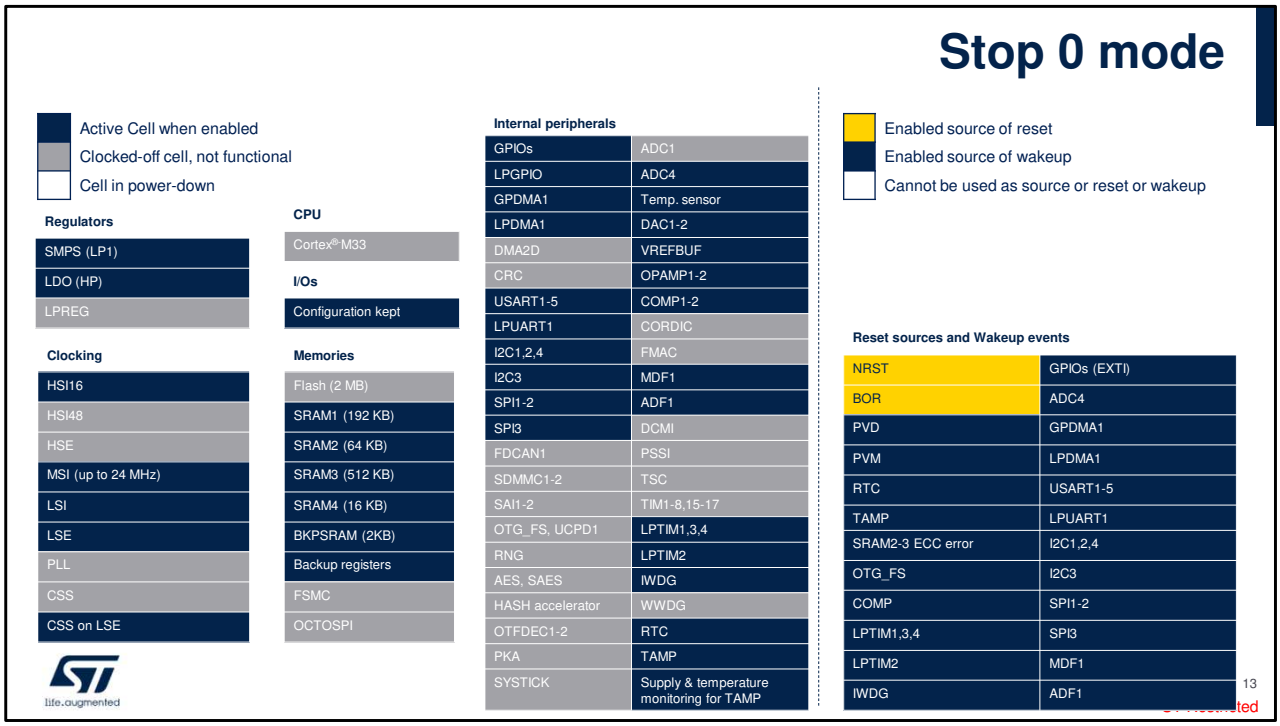
Lowest power mode with full retention and peripheral activity (LPBAM)

- Full retention of SRAM and peripherals registers, with capability to individually power down SRAM pages in Stop 0,1,2,3:
  - SRAM1 : 3 x 64KB-pages
  - SRAM2 : 8KB and 56KB pages
  - SRAM3 : 8 x 64KB-pages
  - SRAM4
  - ICACHE, DCACHE1, DMA2D SRAM, FMAC/FDRAM/USB SRAM, PKA SRAM
- Wakeup clock is HSI16 or MSI up to 24 MHz (range 4 only)
  - FLASH low-power /fast wakeup modes in Stop 0/1
  - SRAM4 low-power /fast wakeup modes in Stop 0/1/2

life.augmented

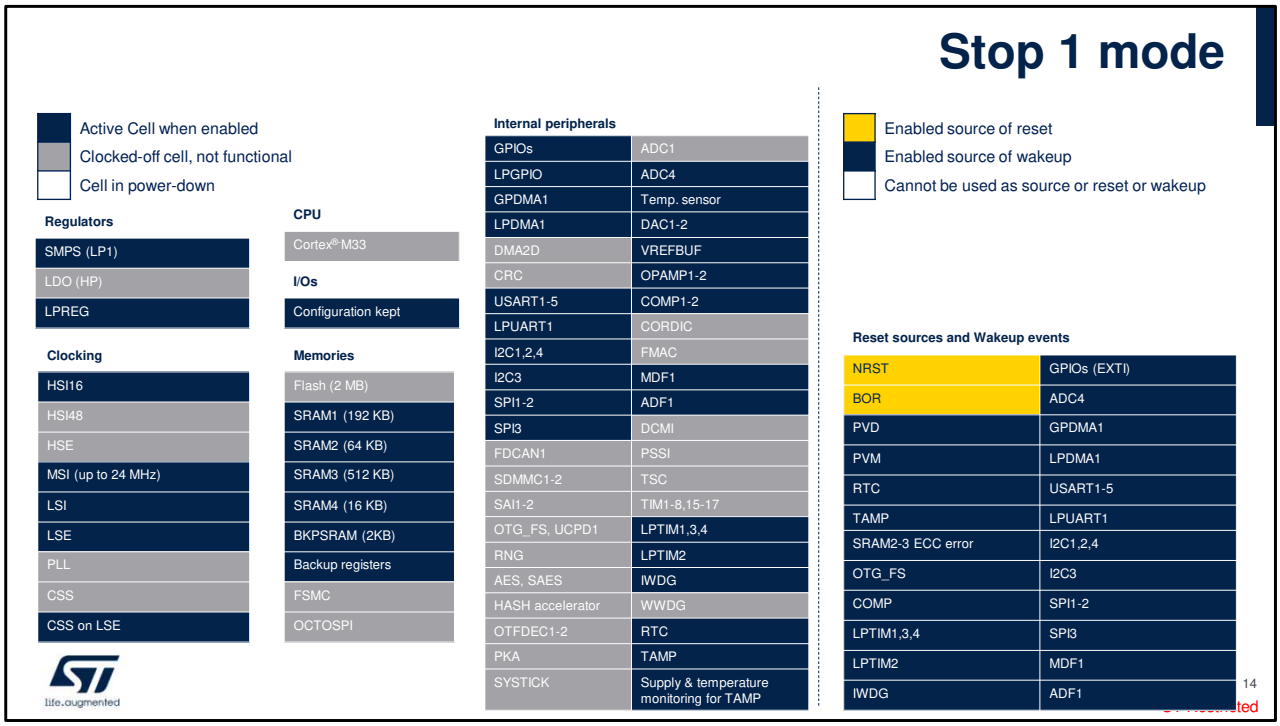
Stop mode achieves the lowest power consumption whilst retaining the content of the SRAM and registers.
All clocks in the core domain are stopped.
In Stop 0 mode, the regulator remains in main regulator mode, allowing a very fast wakeup time but with much higher consumption.
Stop 3 is the lowest power mode with full retention, but the functional peripherals and sources of wakeup are reduced to the same as those in Standby mode.
Sub-blocks or full SRAM1 and SRAM3, full SRAM2 and SRAM4 can be powered-off to save power consumption.
The contents of SRAMs embedded in caches and peripheral units can also be powered-off through control bits.

The system clock when exiting from Stop mode can be either MSIS up to 24 MHz or HSI16, depending on software configuration.
To reduce consumption, the Brown-Out Reset can be configured to operate in discontinuous ultra-low power mode in Standby modes.



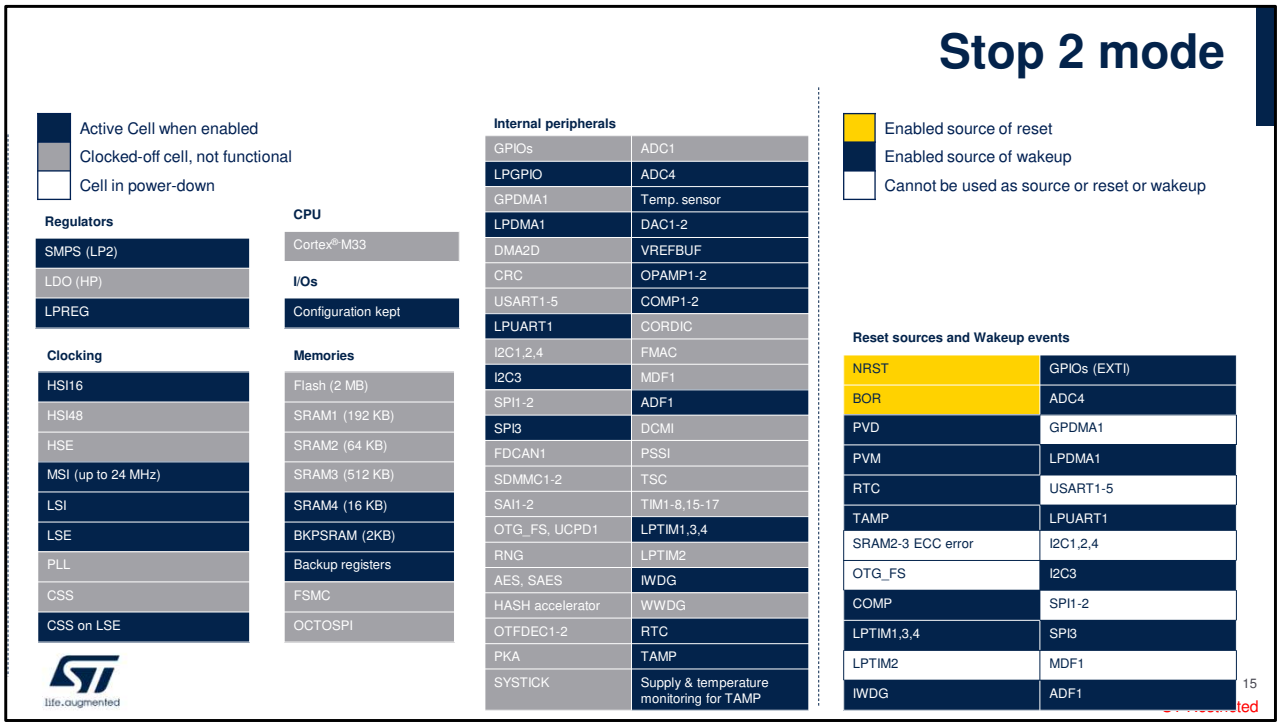
The voltage regulator is configured in main regulator mode
All clocks in the VCORE domain are stopped; the PLL, MSIS, MSIK, HSI16 and HSE oscillators are disabled.
The RTC, clocked by the internal or external low-speed oscillator, can remain active.
The brown-out reset is always enabled. Most of the peripheral clocks are gated off.
The events from all I/Os can wake up from Stop 0 mode, as well as the interrupt generated by the active peripherals.
The system clock, when exiting from Stop 0, can be either MSIS up to 24 MHz or HSI16, depending on the software configuration.

Stop 1 mode

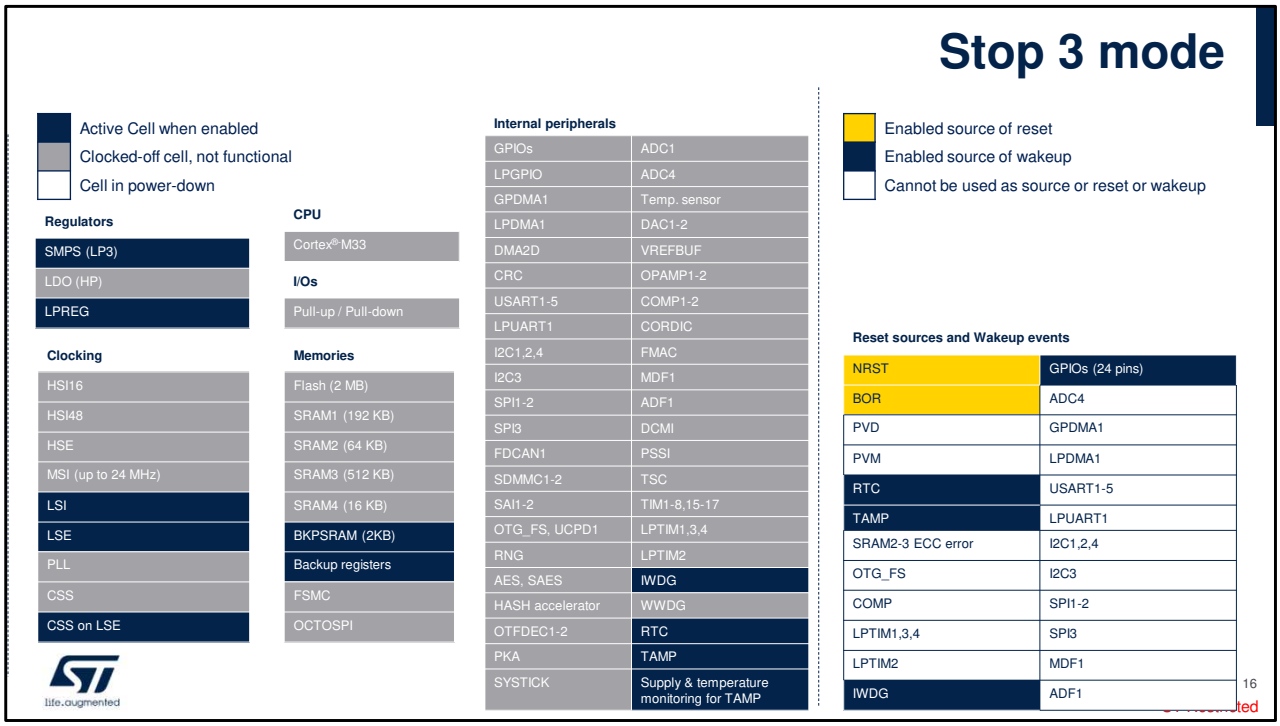


Stop 1 mode is very similar to Stop 0 except that the power figures are much lower as the main regulator is stopped and replaced by the Low Power Regulator.

Stop 2 mode



In Stop 2 mode, most of the VCORE domain is put into a lower leakage mode.
All clocks in the core domain are stopped. The PLL, MSIS, MSIK, HSI16 and HSE oscillators are disabled.
Some peripherals with LPBAM capability can switch on HSI16, MSIS or MSIK for transferring data.
All SRAMs and register contents are preserved, but the SRAMs can be totally or partially switched off to further reduced consumption. The BOR is always available in Stop 2 mode.



The BOR is always available in Stop 3 mode.
In the Stop 3 mode, the I/Os are in floating state by default. The I/Os can be configured with either a pull-up, or a pull-down, or can be kept in analog state.
Some I/Os are used for JTAG/Serial Wire debug and can only be configured to their respective reset pull-up or pull-down state during Stop 3 mode, or configured to floating state.
The RTC outputs on PC13 and PB2 are functional in Stop 3 mode.
PC14 and PC15 used for LSE are also functional.
The 24 wakeup pins multiplexed on eight events (Wakeup 1 to 8) and the eight RTC tampers pins are available.
When exiting the Stop 3 mode, the microcontroller is in

Run mode, Range 4.

Low power background autonomous mode (LPBAM)

Smart way to implement complex applicative scenario in Low-Power mode

- No need for CPU – everything is based on the DMA (LPDMA & GPDMA)
  - Peripheral configuration & activity can be chained thanks to DMA linked-list, down to Stop 2 mode
    - DMA can be used to emulate software and reconfigure peripherals
  - Hardware triggers can start peripheral activity (i.e. ADC conversion, communication peripheral transfer, DMA transfer…)
- Power gain:
  - Most of the product can be shut-down in Stop mode
  - Clock is provided to IP only when necessary in Stop mode
  - Analog peripherals / oscillators are powered-on only when necessary in Stop mode

life.augmented

17

ST Restricted

The Low Power Background Autonomous Mode (LPBAM) is an important new feature of the STM32U5.
While the Cortex-M33 is asleep, some parts of the microcontroller remain active and can perform background tasks that do not require software assistance.
The two DMA controllers LPDMA and GPDMA not only transfer data but can also be initialized to access control registers in order to implement complex sequences involving peripherals and memory.
For example, a timer can trigger a periodic task, that consists of acquiring samples from ADC, moving these samples to memory and monitoring the sampled signal to detect any abnormal condition.
Some peripherals with autonomous mode and wakeup

from Stop capability can request HSI16, MSIS or MSIK to be enabled. In this case, the oscillator is woken up by the peripheral, and is automatically switch off when no peripheral needs it.

Autonomous peripherals features

Autonomous peripheral	
Down to Stop 0/1	**Down to Stop 2**
GPDMA1	
LPDMA1	LPDMA1
USART(1,2,3,4,5)	
LPUART1	LPUART1
I2C(1,2,4)	
I2C3	I2C3
SPI(1,2)	
SPI3	SPI3
ADC4 (12-bit)	ADC4 (12-bit)
DAC	DAC
LPTIM(1,3,4)	LPTIM(1,3,4)
LPTIM2	
MDF1	
ADF1	ADF1

- Peripheral activity is independent from MCU power mode (Run, Sleep, Stop)
- DMA transfers supported in Stop mode
  - Thanks to kernel and AHB/APB clocks requests
- Peripheral activity can be started with an asynchronous trigger in Stop mode:
  - Communication peripherals start of transfer
  - ADC/DAC start of conversion
  - DMA start of transfer

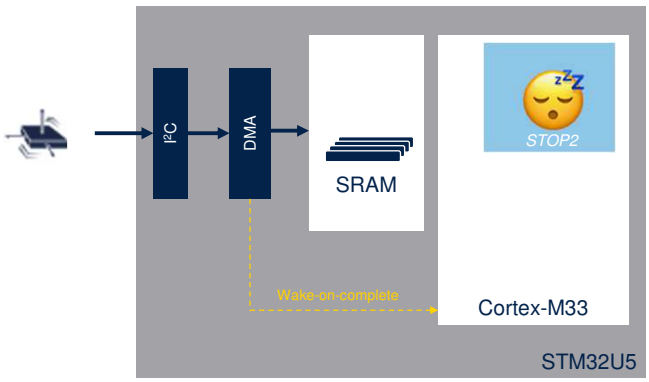
  ➢ Triggers can be selected between LPTIM output, comparator output, I/O…
- Autonomous peripheral interrupts wake up from Stop

life.augmented

The table indicates which peripherals are functional and autonomous in Stop 0 and Stop 1 modes and also highlights those that remain functional in Stop 2 mode.
In Stop mode, asynchronous triggers can be used to automatically start a communication transfer, a conversion sequence, or a DMA transfer.
These hardware triggers can be the low power timer timeout, a comparator output or the detection of an edge on an IO pad.

LPBAM Use-cases

- **I²C slave transfer: SPI / UART reception**
- I²C master transfer: SPI / UART transmission
- ADC conversion
- DAC conversion
- Voice Activity Detection
- LPTIM PWM ratio change, input capture, pulse counter…
- I/O control (input, output)
- Peripheral chaining
- ….-



life.augmented

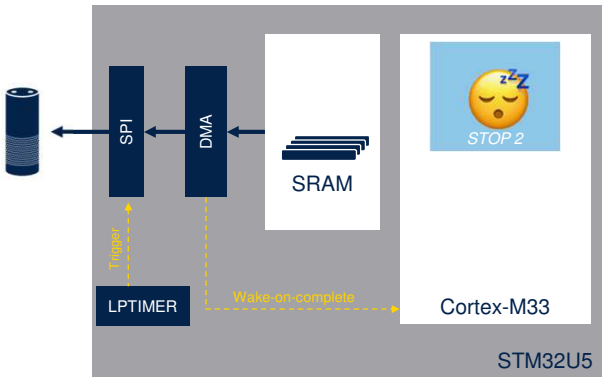
This slide and the following ones provide some implementation examples of Low-power background autonomous mode.
These are background tasks involving modules that remain active while the Cortex-M33 processor is in STOP 0, 1 or 2 low power states.

In this first example, a communication module, such as I2C, receives data that are written to a memory buffer through a DMA channel.
Only I2C number 3 supports this capability in stop 2 mode.
When the DMA channel completes the transfer, it wakes-up the Cortex-M33.
The same approach can be used with SPI and UART

reception.

LPBAM Use-cases

- I²C slave transfer: SPI / UART reception
- **I²C master transfer: SPI / UART transmission**
- ADC conversion
- DAC conversion
- Voice Activity Detection
- LPTIM PWM ratio change, input capture, pulse counter…
- I/O control (input, output)
- Peripheral chaining
- ….

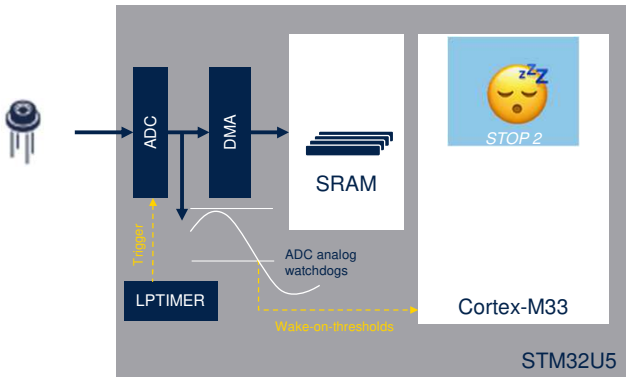


life.augmented

In this second example of LPBAM, a low-power timer periodically triggers a transmission of data from a communication module, such as SPI.
The data are transferred from a memory transmission buffer to the SPI FIFO by a DMA channel.
When the DMA channel completes the transfer, it wakes-up the Cortex-M33.
Asynchronous triggers can be other sources, such as an edge detection on an general purpose input, or a voltage comparator output assertion.
Only SPI number 3 supports this capability in stop 2 mode.

LPBAM Use-cases

- I²C slave transfer: SPI / UART reception
- I²C master transfer: SPI / UART transmission
- **ADC conversion**
- DAC conversion
- Voice Activity Detection
- LPTIM PWM ratio change, input capture, pulse counter…
- I/O control (input, output)
- Peripheral chaining
- ….



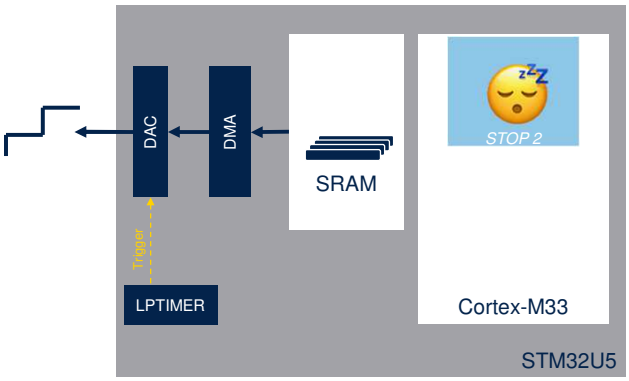
life.augmented

In this scenario, the low-power timer periodically triggers a sample acquisition. A DMA channel automatically transfers these samples to a memory buffer.
A wakeup of the Cortex-M33 is requested on the condition that the ADC analog watchdog detects a conversion result exceeding programmed thresholds.
Temperature sensor, VBAT, VCORE, internal reference voltage, or external channels can be monitored sequentially.
Up to three channels can be monitored in stop mode thanks to three analog watchdogs.
As long as the monitored voltages remain within the programmed thresholds, no wakeup is requested, which enables periodic voltage monitoring while the

microcontroller is in stop 0, 1 or 2 modes.
Only ADC number 4 supports this capability in stop 0, 1 or 2 modes.

LPBAM Use-cases

- I²C slave transfer: SPI / UART reception
- I²C master transfer:SPI / UART transmission
- ADC conversion
- **DAC conversion in sample&hold**
- Voice Activity Detection
- LPTIM PWM ratio change, input capture, pulse counter…
- I/O control (input, output)
- Peripheral chaining
- ….

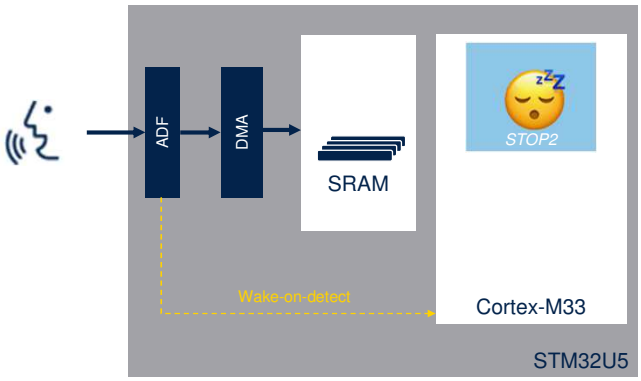


life.augmented

A DMA channel is triggered periodically by a low power timer. It transfers samples from memory to the digital-to-analog converter.
This background task does not require the processor's intervention as long as the waveform to be generated does not change.
Note that an ADC analog watchdog can be used to monitor the conversion result and wake-up the Cortex-M33 whenever the analog voltage is out of programmed thresholds.
This is achieved through the interconnect matrix that internally loops back the output of the DAC to an analog input channel of the ADC.

LPBAM Use-cases

- I²C slave transfer: SPI / UART reception
- I²C master transfer: SPI / UART transmission
- ADC conversion
- DAC conversion
- **Voice Activity Detection**
- LPTIM PWM ratio change, input capture, pulse counter…
- I/O control (input, output)
- Peripheral chaining
- ….



life.augmented

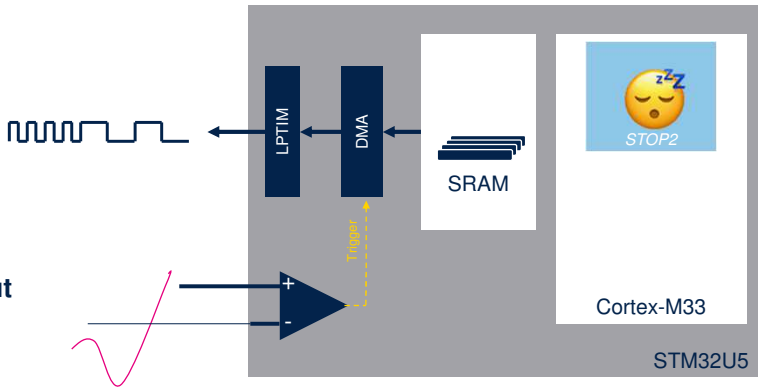
23

ST Restricted

In this example, the audio digital filter, connected to external sigma-delta modulators, processes voice samples and transfers the filtered stream to a memory buffer through a DMA channel.
The audio digital filter can be programmed to wake up the Cortex-M33 when voice activity is detected.

LPBAM Use-cases

- I²C slave transfer: SPI / UART reception
- I²C master transfer: SPI / UART transmission
- ADC conversion
- DAC conversion
- Voice Activity Detection
- **LPTIM PWM ratio change, input capture, pulse counter…**
- I/O control (input, output)
- Peripheral chaining
- ….

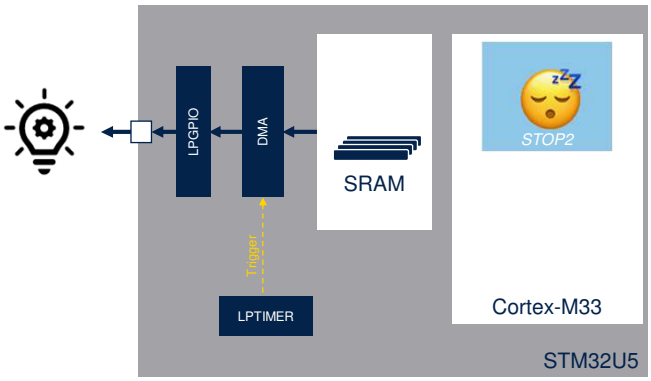


life.augmented

An ultra-low-power comparator COMP1 or COMP2 triggers a DMA transfer from a memory buffer to an LPTIM register, in order to change the duty cycle of a PWM output.
This background task does not require software intervention, so the Cortex-M33 remains in stop 2 mode.

LPBAM Use-cases

- I²C slave transfer: SPI / UART reception
- I²C master transfer: SPI / UART transmission
- ADC conversion
- DAC conversion
- Voice Activity Detection
- LPTIM PWM ratio change, input capture, pulse counter…
- **I/O control (input, output)**
- Peripheral chaining
- ….



life.augmented

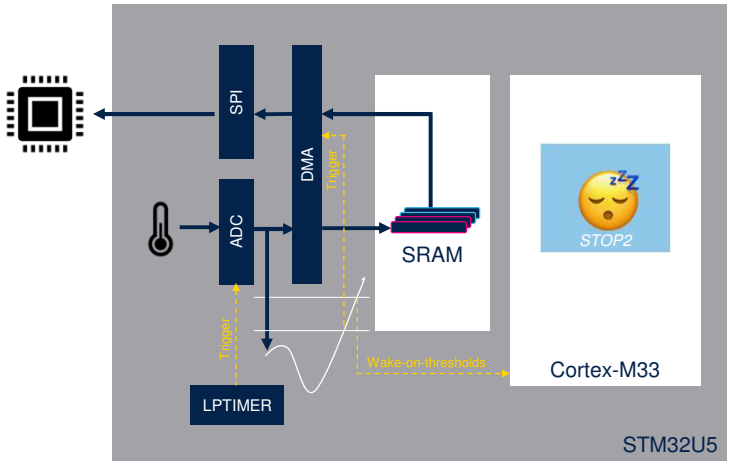
25

ST Restricted

The low power timer periodically requests a DMA transfer from a memory buffer to the low power general purpose input / output module.
For instance a LED can blink while the Cortex-M33 remains in stop 2 state.

LPBAM Use-cases

- I²C slave transfer ; SPI / UART reception
- I²C master transfer ; SPI / UART transmission
- ADC conversion
- DAC conversion
- Voice Activity Detection
- LPTIM PWM ratio change, input capture, pulse counter…
- I/O control (input, output)
- **Peripheral chaining**
- ….



life.augmented

This last scenario demonstrates the collaboration of multiple units without involving the Cortex-M33.
The low power timer periodically triggers an acquisition sequence in the ADC that relies on a DMA channel to transfer the samples to a memory buffer.
When a particular threshold is exceeded, an analog watchdog triggers another DMA channel, that automatically transfers the latest samples to an SPI controller.
For example, these samples can be stored in a non-volatile memory connected to the SPI controller.
Another analog watchdog is programmed with a second threshold, that once exceeded, causes a wakeup of the Cortex-M33.

Stop modes summary

	Stop 0	Stop 1	Stop 2	Stop 3
Regulator	Same as Run mode	Low-power	Low-power	Low-power
Functional peripherals & wakeup sources	From CPU and SRD domains		SRD domain	Same as Standby
Clocks	LSE / LSI / HSI16 / MSI up to 24MHz			LSE / LSI
I/Os	State kept Dynamic control with GPDMA1 Wakeup with all I/Os		State kept Dynamic control of up to 16 I/Os with LPDMA1 Wakeup with all I/Os	Pull-up / pull-down 24 Wakeup pins
Consumption on SMPS all SRAM retained (µA)	41.5		8.95	4.3
Wakeup time (µs) ➢ Wakeup in flash, range 4 with MSI 24 MHz ➢ All SRAM retained	11	22	23	28.5

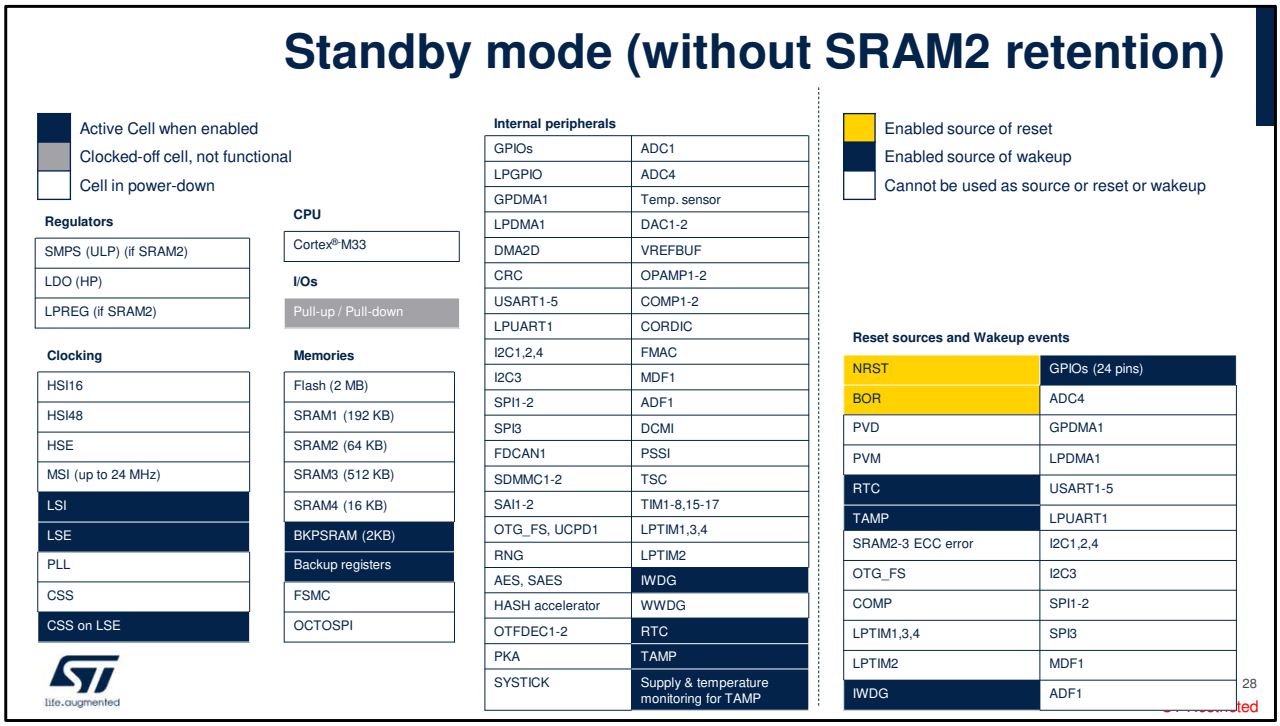
life.augmented

27

ST Restricted

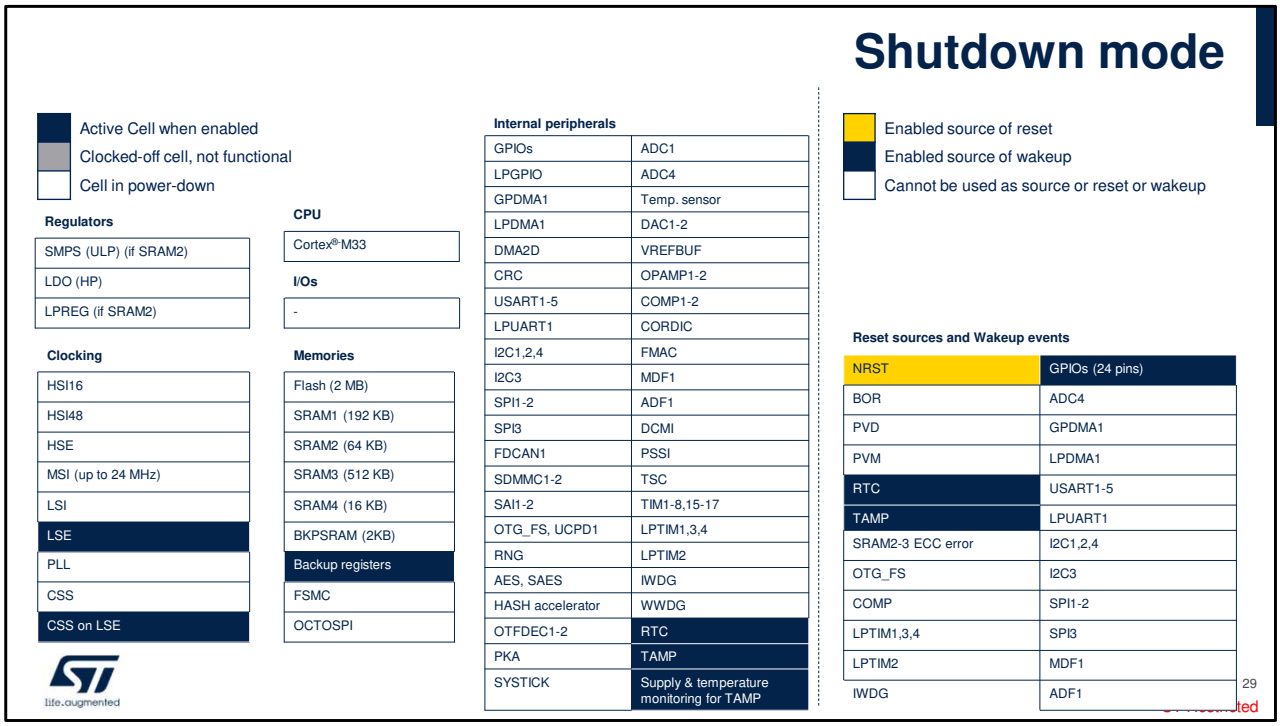
This table summarizes the differences between the four stop modes.
The main regulator is active in stop 0 mode, while the low-power regulator is active in stop 1, 2 and 3.
Functional peripherals in stop 0 and 1 modes belong to the CPU and Smart Run domains.
Only peripherals in the Smart Run domain remain active in stop 2 mode.
Active peripherals in Stop 3 are the same as in standby mode.
All I/Os are active and can be used for wakeup in stop 0, 1 and 2 modes. However only 16 I/Os are accessible by LPDMA1 in stop 2 mode.
In stop 3, 24 pins can be used for wakeup.

The microcontroller consumption is drastically reduced when entering stop 2 and stop 3 modes, although the wakeup time is not much more than in stop 1 mode.



In Standby mode, both main and low power regulators are powered down.
The PLL, HSI16, MSIS, MSIK and HSE oscillators are switched off.
The RTC, clocked by the internal or external low-speed oscillator, may remain active .
The brown-out reset is always enabled. The independent watchdog can also be enabled in Standby mode.
Reset, brown-out reset, RTC and tamper detection, independent watchdog and any event on the wakeup pins can exit the microcontroller from Standby mode.
I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
The 24 wakeup pins multiplexed on eight events and the

eight RTC tampers pins are available.
This slide describes the state of the microcontroller when standby mode without SRAM2 retention is active.
SRAM2 content can be partially or fully preserved. In this case, the low-power regulator is ON and provides the supply to SRAM2 only.



The shutdown mode is the lowest power mode of the STM32U5, with only 110 nano Amperes.
In Shutdown mode, the main regulator and the low-power regulator are powered down.
The SRAMs and register contents are lost except for registers in the Backup domain.
The RTC can remain active.
The brown-out reset is deactivated. Only the external low-speed clock can be enabled.
The wakeup events are the RTC and tamper events, the reset and the 24 wakeup pins.
I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Low-power modes: Standby and Shutdown modes

- Wakeup from Standby clock is MSI 1 to 4 MHz
- Standby:
  8 KB + 56 KB SRAM2 (total 64 KB) can be individually retained
  2 KB BKPSRAM can be retained
- ULPMEN=1 to reduce Standby consumption
- 24 wakeup pins multiplexed on 8 events, together with internal wakeup events
  - WUSELx must be configured to 11 to wakeup with RTC or TAMP
  - If WUSELx=11: WUFx is cleared by hardware when all internal wakeup sources are cleared

Wakeup event	(WUSELx = 00)	(WUSELx = 01)	(WUSELx = 10)	(WUSELx = 11)
WKUP1	PA0	PB2	PE4	-
WKUP2	PA4	PC13	PE5	-
WKUP3	PE6	PA1	PB6	-
WKUP4	PA2	PB1	PB7	-
WKUP5	PC5	PA3	PB8	-
WKUP6	PB5	PA5	PE7	RTC_ALRA_S or RTC_ALRB_S or RTC_WUT_S or RTC_TS_S
WKUP7	PB15	PA6	PE8	RTC_ALRA or RTC_ALRB or RTC_WUT or RTC_TS
WKUP8	PF2	PA7	PB10	TAMP or TAMP_S

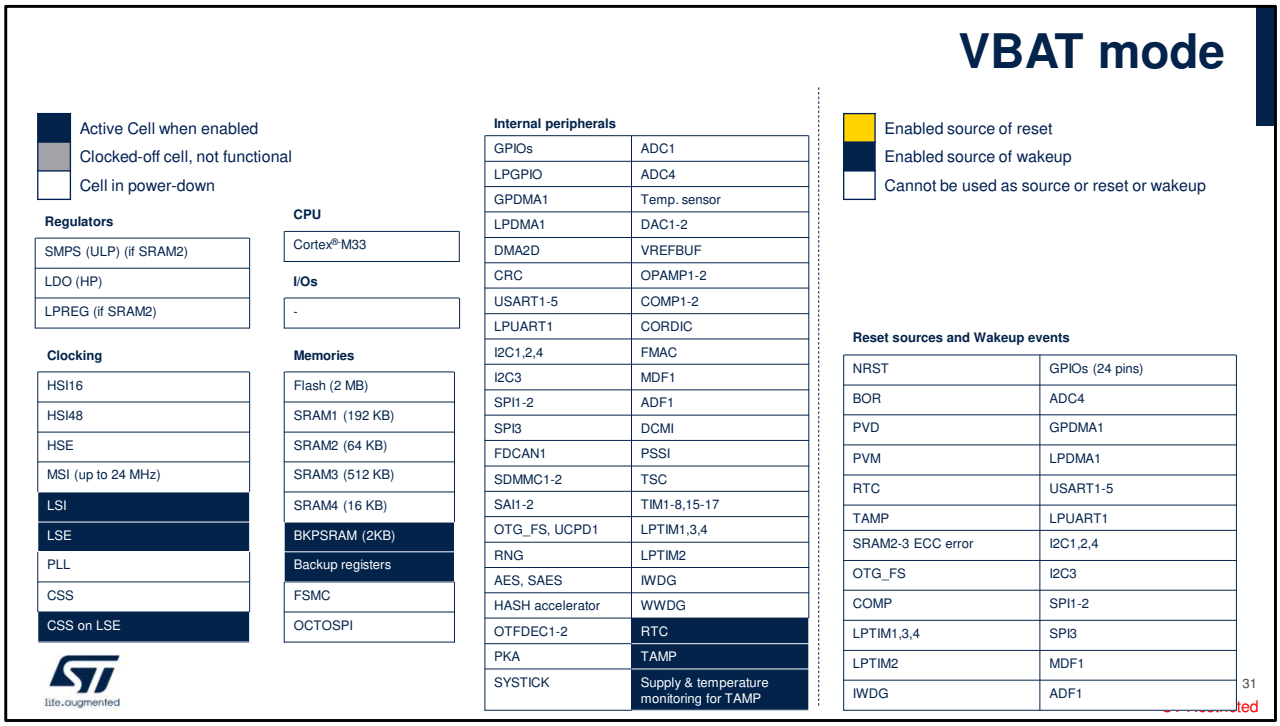
life.augmented

30

ST Restricted

The clock source used to exit standby state is the MSI, from 1 to 4 MHz.
In standby state, two parts of the SRAM2 can be independently retained, one 8-kilobyte part and one 56-kilobyte part.
The 2-KB backup SRAM is preserved in standby mode, but not in shutdown mode.
The table indicates which pins remain active when exiting standby or shutdown modes.
24 wakeup pins and the 8 RTC tamper pins are multiplexed on eight events (Wakeup 1 to 8). The WUSEL bitfields select which pins and events cause a wakeup. WUSEL must be configured to binary 11 to wakeup with RTC or external tamper detection.

VBAT mode



VBAT is the power supply when VDD is not present for RTC, external clock 32 kHz oscillator, backup registers and optionally backup SRAM.
Consumption in VBAT mode without RTC is 120 nano amperes at 1.8 Volt, and 450 nA with RTC.
In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT.
When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery level.

VBAT mode

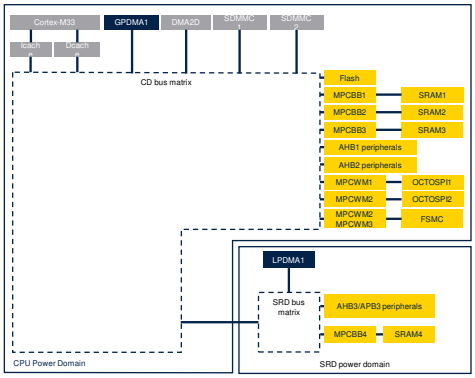
- VBAT battery charging when VDD is present
- VBAT Brownout reset (1.58V)
- 2 KB BKPSRAM can be retained (optionally protected by tamper)
- RTC and TAMP active with LSE or LSI, including 8 tamper pins
- LSE clock security system connected to tamper with:
  - Clock missing detection & Over-frequency detection (2MHz)
  - Glitch filtering (2MHz)
- Temperature and backup domain voltage monitoring connected to tamper

life.augmented

The battery charging feature enables the charging of a super-capacitor connected to VBAT pin through an internal resistor when VDD supply is present.
The charging is enabled by software and is done either through a 5kΩ or 1.5kΩ resistor depending on software.
Battery charging is automatically disabled in VBAT mode.
The VBAT power domain has a dedicated Brown-Out Reset circuit.
Note that the RTC remains active, using either the internal or external low speed oscillator.
Temperature and backup domain voltage monitoring can lead to a tamper, as well as LSE clock missing detection or over-frequency detection.
These tamper events can be programmed to cause the

erasure of the backup SRAM and backup registers.

PWR modes output pins



CSLEEP	CDSTOP	SRDSTOP	MCU power mode
0	0	0	Run mode
1	0	0	Sleep mode or Stop 0 or Stop 1 modes, with AHB/APB clocks running in the CPU domain (CD) and SmartRun domain (SRD)
1	1	0	Stop 0, Stop 1 or Stop 2 mode, with AHB/APB clocks running in the SmartRun domain (SRD)
1	1	1	Stop 0, Stop 1, Stop 2 or Stop 3 modes

life.augmented

In order to help with debug, three signals are available as device pin alternate functions: CSLEEP, CDSTOP and SRDSTOP.
The corresponding 3-bit combination indicates the current microcontroller power mode.
CSLEEP, CDSTOP and SRDSTOP are generated in the core domain, consequently they are not driven in Standby and Shutdown modes.
They can also be used by an external board level power management logic.

Secure and Privilege protections

- Individual security configuration for :
  - Low-power modes
  - Wakeup pins
  - Voltage detection
  - Power monitoring
  - Backup domain
  - I/Os pull-up pull-down configuration
- Additional PWR configuration bits are automatically secure:
  - If System clock selection is secure in RCC:
    - The voltage scaling (VOS) configuration in PWR is secure
  - If a GPIO is configured as secure:
    - Its corresponding bit in PWR for Pull-up/Pull-down configuration in Standby mode is secure
  - If the UCPD is secure:
    - The UCPD_DBDIS bit (USB Type-C and power delivery dead battery disable) and UCPD_STDBY bit (USB Type-C and power delivery Standby mode) in PWR are secure
- Separate privilege protection configuration for secure registers/bits (SPRIV) and non-secure registers/bits (NSPRIV) to support four isolated threads: S/P; S/NP; NS/P; NS/NP

life.augmented

The PWR is a trustzone-aware module. Both the secure attribute and the privilege level of some PWR registers are programmable, enabling four partitions: secure privileged, secure non privileged, non-secure privileged and non-secure non privileged.

The PWR TrustZone security secures the following features through the security configuration register: Low-power mode, Wake-up (WKUP) pins, voltage detection and monitoring, VBAT mode and I/O pull-up/pull-down configuration.
The security of some features is based on an inheritance mechanism:
- When the system clock selection is secure in RCC, the

voltage scaling (VOS) configuration and the regulator booster are secure.

- When a GPIO is configured as secure, its corresponding bit for Pull-up/Pull-down configuration in Standby mode is secure.
- When the UCPD1 is secure in the GTZC, the PWR_UCPDR register is secure.

Thank you

life.augmented

In addition to this training, you can refer to the following presentations:

- Reset and Clock Control
- Real-Time Clock
- Tamper
- STM32CubeMX, focusing on the description of the power consumption calculator.