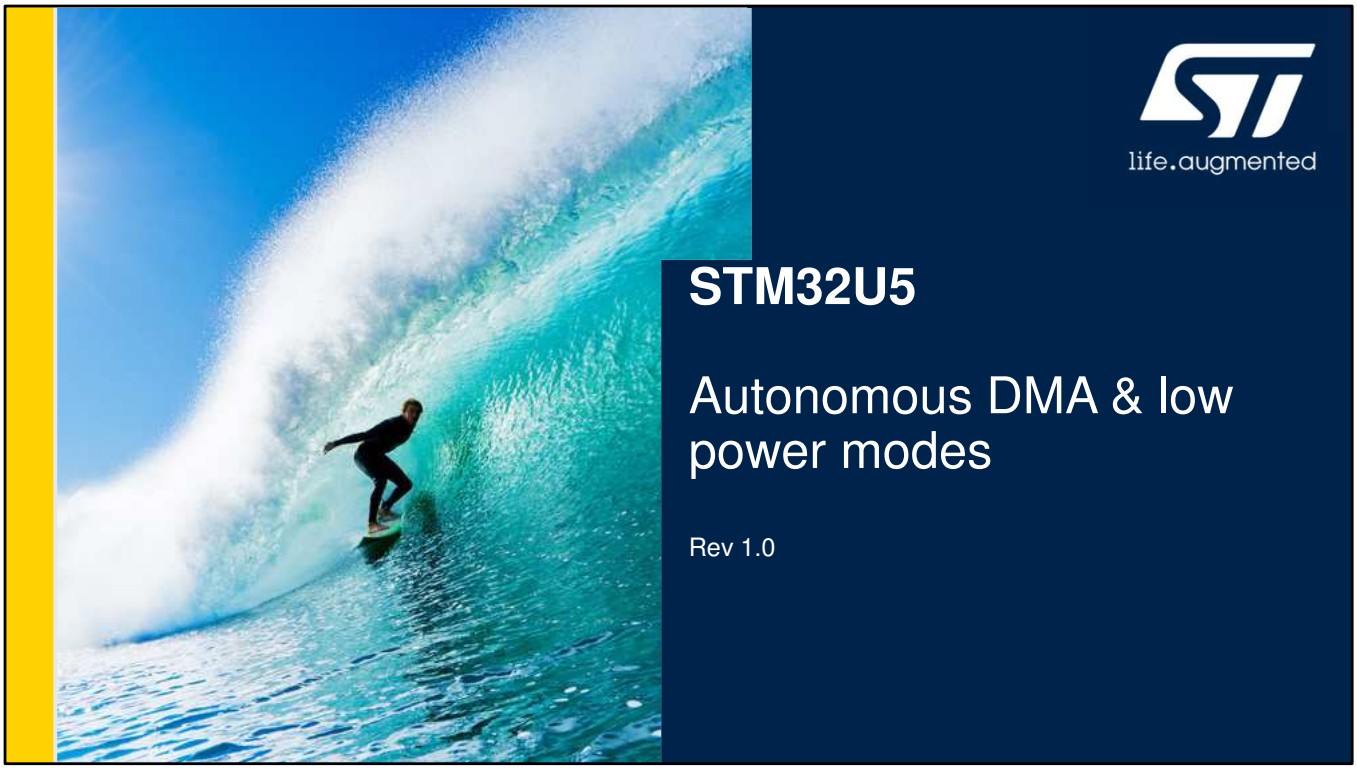

Hello, and welcome to this presentation, which describes the effect of low power modes on GPDMA and LPDMA.

Autonomous LP/GPDMA

- DMA finely manages its own clock gating; requesting its clock from the RCC only when needed in any power mode
- In low power modes, the DMA can be programmed to either:
  - A wakeup CPU on completion of a specific transfer by the enabled interrupt
  - Continue autonomously and perform another LLI_{n+1} transfer

life.augmented

To save power while the LPDMA or GPDMA executes programmed linked-list transfers, the DMA controller hardware automatically manages its own clock gating and generates a clock request output signal to the RCC, whenever the device is in Run, Sleep or Stop mode. When used in low-power modes, a CPU wakeup can be requested on completion of a specific channel transfer. Alternatively, the DMA can autonomously perform a next LLI transfer.

Autonomous LP/GPDMA

Low-power mode	LPDMA/GPDMA	
Sleep	No effect ➢ DMA interrupts cause the device to exit Sleep mode	
Stop 0, Stop 1	The contents of the DMA registers are kept when entering Stop mode ➢ The contents of the DMA registers can be autonomously updated by the next linked-list item from memory, to perform autonomous data transfers ➢ DMA interrupts can cause the device to exit Stop mode	
Stop 2	GPDMA	The GPDMA is powered down
	LPDMA	The contents of the LPDMA registers are kept when entering Stop 2 mode ➢ The contents of the LPDMA registers can be autonomously updated by the next linked-list item from memory, to perform autonomous data transfers ➢ LPDMA interrupts can cause the device to exit Stop mode
Stop 3	The DMA is powered down and must be reinitialized after exiting Stop 3 / Standby mode	
Standby		

life.augmented

3

This table summarizes the effect of low-power modes on the GPDMA and LPDMA.
Sleep mode has no effect on the DMA which remains functional. An interrupt generated by the DMA controller can cause the exit from sleep mode.
In stop 0 and stop 1, both the LPDMA and the GPDMA remain functional. Transfers can occur in low-power background autonomous mode, including link transfers. An interrupt generated by the DMA controller can cause the exit from stop 0 and stop 1 modes.
In stop 2, the GPDMA is powered down while the LPDMA remains fully functional. Transfers can occur in low-power background autonomous mode, within the SmartRun domain.
In stop 3 and standby, the LPDMA and the GPDMA are

powered down. They must be reinitialized when exiting these modes.

Thank you

life.augmented

In addition to this presentation, you can refer to the other presentations on the GPDMA and LPDMA:

- DMA overview
- DMA transfers hardware and software views
- DMA: Circular buffering & double buffering
- DMA linked list
- DMA 2D addressing
- DMA Register file
- DMA Error reporting
- DMA Input-output LLI control.

You can also refer to the presentation on power management.