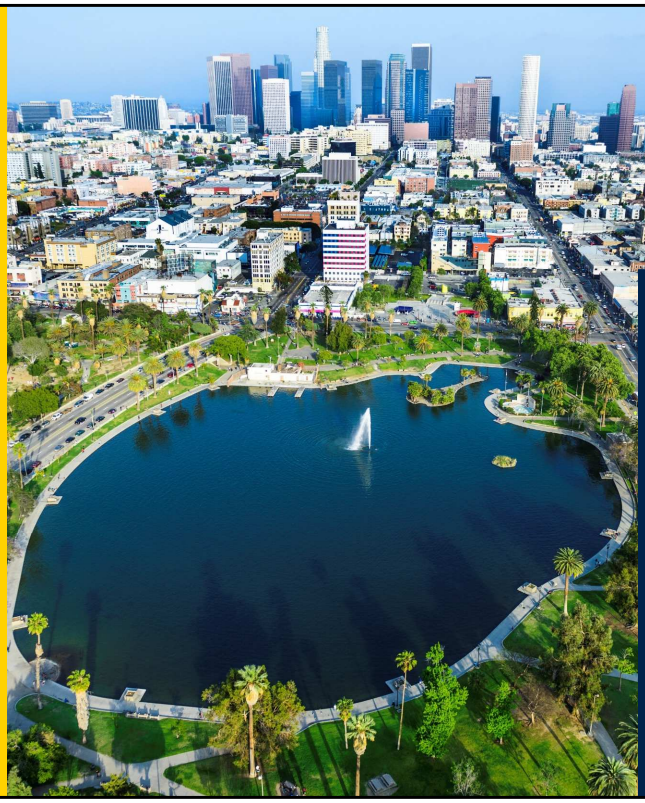


life.augmented

STM32U0 – SYSCFG
System Configuration Controller

Hello, and welcome to this presentation of the STM32U0 System Configuration Controller.

Overview

- STM32U0xx microcontrollers feature a set of configuration registers
- The main purposes of the system configuration controller are the following:
  - Enabling /disabling I²C Fast-mode Plus high-drive
  - Enabling/disabling the analog switch voltage booster
  - Configuring the Infrared Timer (IRTIM) module
  - Configuring the analog inputs of the Touch Sensing Controller (TSC)
  - Remapping the PA11 and PA12 GPIOs to PA9 and PA10
  - Selecting the memory accessible at address 0x0000_0000
  - Indicating pending interrupt events connected to the same NVIC irq line
  - Enabling/disabling safety and security features

life.augmented

STM32U0 microcontrollers feature a set of configuration registers located in the SYSCFG module.
The System Configuration Controller gives access to the following features:

- Enabling /disabling I2C Fast-mode Plus high-drive
- Enabling/disabling the analog switch voltage booster
- Configuring the Infrared Timer (IRTIM) module
- Configuring the analog inputs of the Touch Sensing Controller (TSC)
- Remapping the PA11 and PA12 GPIOs to PA9 and PA10
- Selecting the memory accessible at address 0x0000_0000
- Indicating pending interrupt events connected to the same NVIC irq line
- Enabling/disabling safety and security features

I²C I/Os Fast-mode

- The four I²C controllers of the STM32U0 support three speeds

Mode	Bit Rate	Extra output drive I/Os
Standard-mode (Sm)	≤ 100 Kbps	NO
Fast-mode (Fm)	≤ 400 Kbps	NO
Fast-mode Plus (Fm+)	≤ 1 Mbps	YES

- Extra output drive is controlled by the SYSCFG module
  - It can be enabled even when I²C is not the selected alternate function
- This functionality is kept for legacy purpose. Embedded I²C controllers are now capable to control output drive directly.

life.augmented

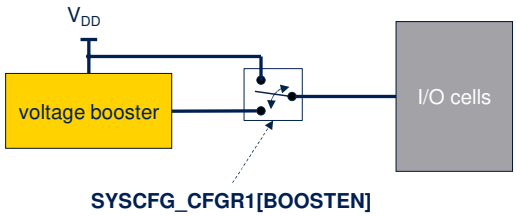
The four I2C controllers present in the STM32U0 support 3 speeds:

- Standard-mode, the maximum bitrate is 100 Kilobits per second
- Fast-mode, the maximum bitrate is 400 Kilobits per second
- Fast-mode Plus, the maximum bitrate is 1 Megabit per second.

Fast-mode Plus requires a high drive capability, which is enabled in I2C_CR1 register of the I2C controller.
For compatibility reasons, high drive capability can also be controlled from SYSCFG_CFGR1 register.

I/O Analog Switch Voltage Booster

- Activating the Voltage Booster is recommended when using the analog inputs in low VDD voltage operation (i.e. lower than 2.4 V)

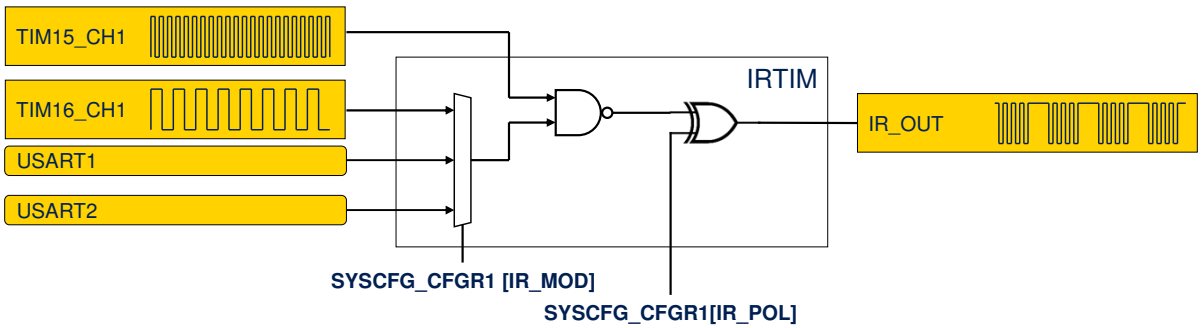


life.augmented

The STM32U0 supports a voltage booster, that should be used when the analog inputs operate in low VDD voltage. It is activated by setting the BOOSTEN bit in the SYSCFG_CFGR1 register.

IRTIM Module Configuration

- The Infrared Timer (IRTIM) module relies on USART and Timer sources to generate the modulation envelope
  - The SYSCFG module is used to select the source signal
  - It is also used to activate an output inverter



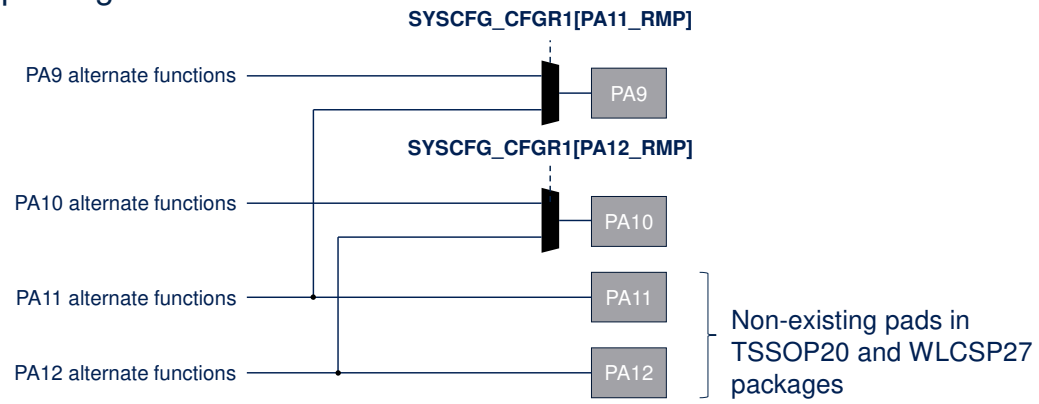
life.augmented

5

The Infrared Timer (IRTIM) unit requires a modulation envelope signal that is provided either by USARTs or by TIM16. The IR_MOD field in SYSCFG_CFGR1 register controls the related input multiplexer.
The IR_POL bit in the SYSCFG_CFGR1 register selects whether or not the output signal is inverted.

GPIO Remap

- Two GPIOs PA12 and PA11 can be remapped by PA10 and PA9 respectively in order to give access to their functions when the Pins are not natively available on the package



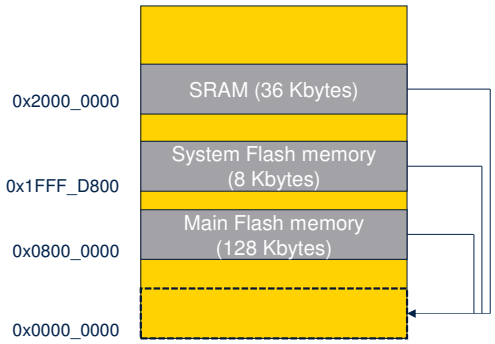
life.augmented

6

When the PA11_RMP bit in the SYSCFG_CFGR1 register is set, the PA11 alternate functions are remapped to pins PA9.
Similarly, when the PA12_RMP bit in the SYSCFG_CFGR1 register is set, the PA12 alternate functions are remapped to pins PA10.
This is useful when these alternate functions are needed while the PA11 and PA12 pins are not available in low pin-count packages.

GPIO Memory Mapping

- Three memories can be aliased at address 0x0000_0000
  - Main Flash memory
  - System Flash memory
  - Embedded SRAM



SYSCFG_CFGR1[MEM_MODE]
=0bX0: Main Flash memory
=0b01: System Flash memory
=0b11: SRAM
- Default value depends on the state of BOOT0 pin and, nBOOT0, nBOOT1, nBOOT_SEL, and BOOT_LOCK option bits

life.augmented

7

The MEM_MODE field in the SYSCFG_CFGR1 register selects which memory is accessible at address 0.
Three memories can be aliased to address 0: main flash memory, system flash memory or SRAM.
Note that the default setting of this field depends on boot pin and option bytes.

Safety Features

- The SYSCFG_CFGR2 register controls safety features:
  - Parity error flags:
    - SPF is set when an SRAM1 parity error is detected
    - BKPF is set when a backup SRAM2 parity error is detected
  - The five other bits are used to enable/disable the assertion of TIM1/15/16 break input when the following events occur:
    - SRAM1 parity error
    - Backup SRAM2 parity error
    - Flash memory ECC error
    - Programmable Voltage Detector rising or falling threshold exceeded
    - Cortex®-M0+ lockup
      - Where a fault or supervisor call occurs at a priority of -1 or above, the Cortex-M0+ enters lockup state

life.augmented

The SYSCFG_CFGR2 register contains the control and status bits linked to safety and robustness. Five control bits direct certain error detection events to the timers break inputs. This allows timer outputs to be placed in a known state during an application crash.
Once programmed, the connection is locked until the next system reset.
These internal events are the power voltage detector event, the Cortex-M0+ LOCKUP state, the SRAM1 parity error, the backup SRAM2 parity error, and Flash ECC error.
The SYSCFG_CFGR2 register also contains flag bits notifying parity error detection, one for SRAM1 and one for backup SRAM2.

Security Features

- The SYSCFG_SCSR and SYSCFG_SKR registers provide a programming interface used to erase the contents of SRAM2:

  1. Program the key into SYSCFG_SKR (0xCA followed by 0x53)
  2. Initiate the erasure by setting SYSCFG_SCSR[SRAM2ER]
  3. Wait until erasure is complete by polling SYSCFG_SCSR[SRAM2BSY]
  4. Program a wrong key into SYSCFG_SKR to reactivate the write protection of SRAM2ER control bit

life.augmented

The SRAM2's erasure requires a dedicated procedure, described in this slide.
First, write access to the control bit used to start the erasure is enabled by programming a key into the key register.
Then the erasure can be launched.
Software polls a busy status bit to determine when erasure is completed.
At the end, writing a wrong key value locks the access to the control bit used to start the erasure.

Touch Sensing Controller (TSC)

- The SYSCFG_TSCCR configures the analog inputs of the Touch Sensing Controller
  - TSC_IOCTRL control bit can be used to force the I/O configuration as analog when TSC alternate function is selected
  - Five control bits can connect various IO pads to TSC comparators

life.augmented

The SYSCFG_TSCCR configures the analog inputs of the Touch Sensing Controller (TSC).
The TSC_IOCTRL control bit can be used to force the I/O configuration as analog when TSC alternate function is selected.
G7_IO1 enables connection of PA9 to TSC COMP1.
G6_IO1 enables connection of PD10 to TSC COMP1.
G4_IO3 enables connection of PC6 to TSC COMP2.
G2_IO3 enables connection of PB6 to TSC COMP2.
G2_IO1 enables connection of PB4 to TSC COMP2.

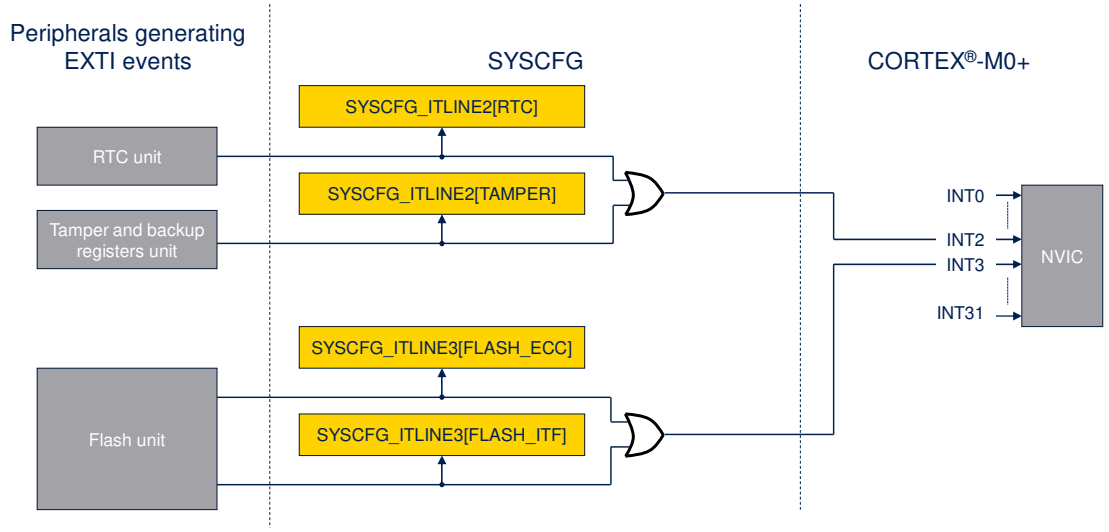
Interrupt Line Status Registers

- A dedicated set of read-only registers is implemented in the SYSCFG module to collect all pending interrupt sources associated with each interrupt line into a single register
  - This allows users to check by a single read operation which peripheral requires service
  - In order to explain the benefit of these registers, the next slide describes the management of interrupt sources steered to NVIC IRQ2 and IRQ3 lines

life.augmented

The SYSCFG module supports 32 interrupt line status registers.
They enable software to easily find the cause of an interrupt, by collecting in the same register all pending interrupt sources associated with a particular interrupt line.
In order to explain the benefit of these interrupt line status registers, the following slide will focus on interrupt events steered to NVIC IRQ2 and IRQ3 lines.

Interrupt Status Registers



life.augmented

12

The left part of the figure represents the peripherals able to assert NVIC's INT2 and INT3, respectively RTC/TAMPER and Flash memory units.
Regarding INT2, RTC and Tamper interrupt requests are ORed together.
Regarding INT3, Flash memory ECC and Flash interface interrupt requests are ORed together.
The source of NVIC's INTx can be found by reading the related SYSCFG_ITLINEx register.

Related peripherals

- Refer to these training modules linked to this peripheral:
  - Inter-Integrated Circuit (I²C)
  - Infrared Timer Interface (IRTIM)
  - Touch Sensing Controller (TSC)
  - General-purpose Input/Output (GPIO)
  - Flash memory (Flash)
  - Interrupts (NVIC-EXTI)
  - Timers (TIM)

life.augmented

In addition to this presentation, you can refer to I2C, IRTIM, TSC, GPIO, Flash memory, interrupts and timers presentations.

References

- For more details, please refer to following documentation:
  - AN2606: STM32 microcontroller system memory boot mode

life.augmented

For more details, please refer to application note AN2606: STM32 microcontroller system memory boot mode.

Thank you

life.augmented

Thanks for having attended this presentation.