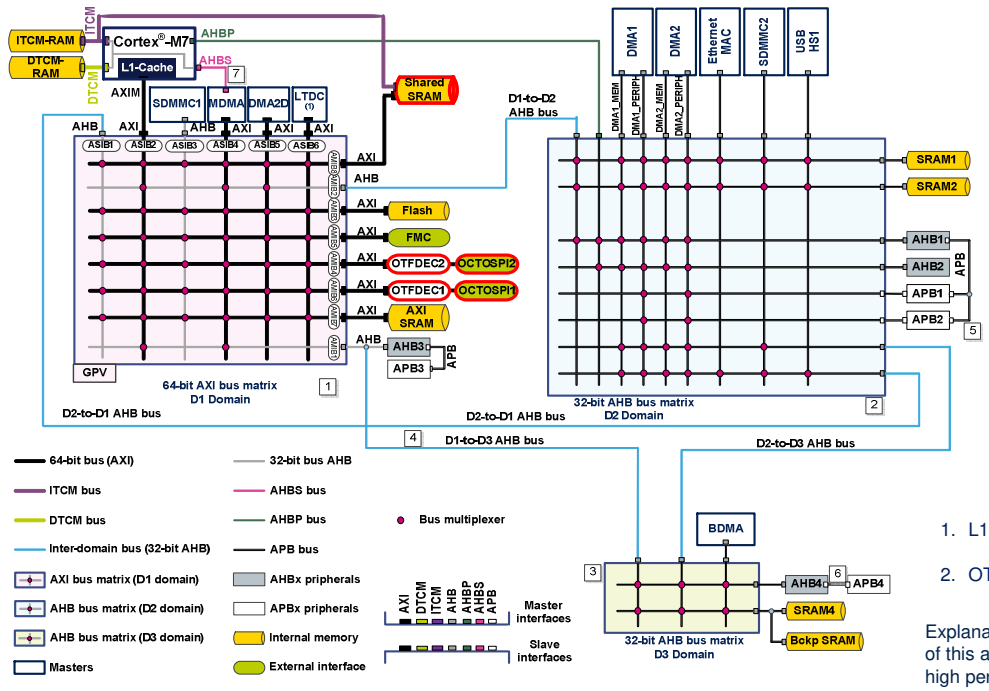
STM32H2x and H73x Expanding STM32H7 Family with higher frequency

Delta STM32H74x/5x and STM32H7Ax/Bx

V1.0

The following slides present an overview of the architecture of the new variants of the STM32H7 family.

Architecture Overview

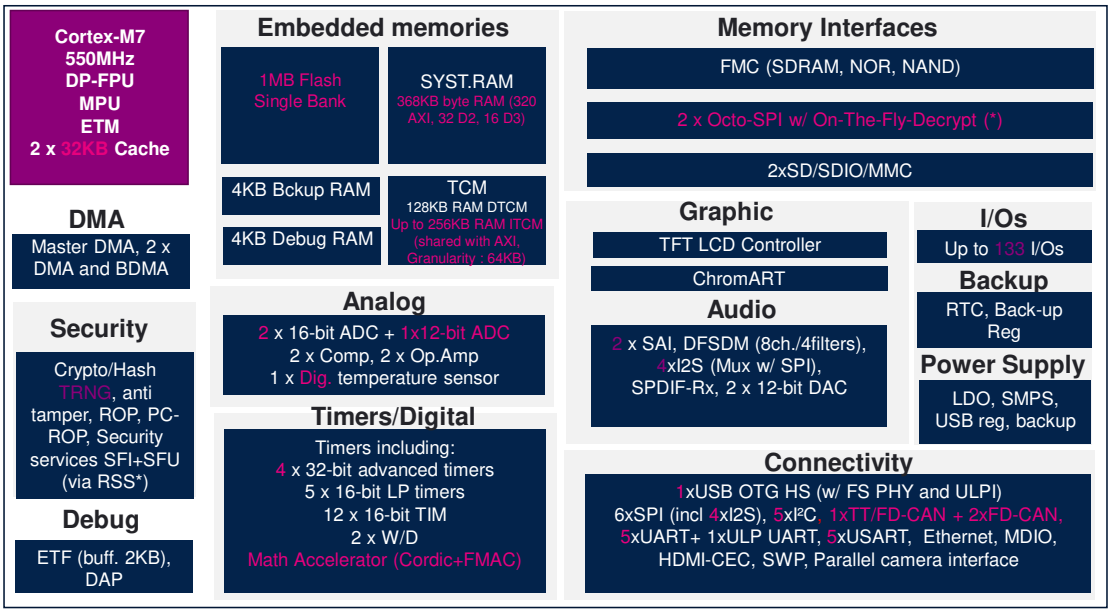


The schematic shows the architecture of the STM32H72/73 lines.
The main differences with STM32H74/75 microcontrollers are highlighted in red.
Only one bank Flash is available compared to the dual bank flash of STM32H74/75 lines. Two OCTOSPI interfaces support most of the serial external memories.
The On-the-fly decryption engine, available in crypto devices (STM32H73), allows the on-the-fly decryption of encrypted content that is then stored in external OCTOSPI memories.
The STM32H72/73 offers 192 Kbytes of RAM split in three 64-Kbyte blocks, those blocks can be connected either to AXI or ITCM.
More explanations on STM32H72/73/74/75 architecture and performance are available in application note AN4891.

STM32H72x/73x

3 x power domains, SMPS and LDO,
compatible with the STM32H74x/75x on common packages

Key features
- ✓ Performance
- ✓ RAM re-map
- ✓ ECC on all memories
- ✓ Multiple high perf ADC
- ✓ Graphic
- ✓ Security
- ✓ Math accelerators
- ✓ Memory interfaces
- ✓ Connectivity
- ✓ Power supply scheme
  (SMPS or LDO.
  Except QFN68-SMPS only)
- ✓ STM32 DNA
  (Compatibility, packages, Ecosyst)
- ✓ Extended Temp range support 125C (option**)



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(*) : on STM32H73x CPN (Crypto)

(**) : CPN in "3" (Ex STM32H725ZGT**3**)

The size of the RAMs are globally decreased compared to the STM32H74/75 line.
To increase processing performance, the size of both data and instruction caches have been increased from 16 Kbytes to 32 Kbytes.
Thanks to the shared RAM, the ITCM, accessible at CPU max frequency, can be increased from 64 Kbytes to 128, 192 or 256Kbytes.
Two accelerators have been added: The Cordic coprocessor accelerates certain mathematical functions, mainly trigonometric ones, and the FMAC accelerator performs arithmetic operation on vectors.
The product is available with three different Flash sizes: 1Mbytes, 512 Kbytes and 128 Kbytes configuration.

H72/73 vs H7A/7B vs H74/75 features

		STH32H74x/75x	STH32H7Ax/7Bx	STH32H72x/73x
Core		ARM Cortex-M7, DPMPU, FPU, L1 16KB-D/16KB-I ARM Cortex-M4, SPMPU, FPU, ART	ARM Cortex-M7, DPMPU, FPU, L1 16KB-D/16KB-I -	ARM Cortex-M7, DP FPU, MPU, L1 32KB-D/32KB-I -
Operating range		1.62 to 3.6 V and Tj –40 to +125 °C Upto +140°C with SMPS VOS1 limited to 125° C Vcore @VOS0: Tj limited to 105C, VDD min 1.7V No SMPS	1.62 to 3.6 V and Tj –40 to +130 °C Vcore @VOS0: Tj limited to 105C VDD min 1.7V	1.62 to 3.6 V and Tj –40 to +125 °C Up to 140°C with SMPS VOS1 up to 140° C Vcore @VOS0: Tj limited to 105C VDD min 1.7V LDO VDD min 2.2V SMPS
ARM M7 Frequency / DMIPS		480MHz / 1027DMIPS in VOS0 400MHz / 856DMIPS in VOS1	280MHz / 599DMIPS in VOS0 225MHz / 481DMIPS in VOS1	550MHz / 1177DMIPS in VOS0 400MHz / 856DMIPS in VOS1
AXI and AHB max frequency		240MHz	280MHz	275MHz
APB max frequency		120MHz	140MHz	137.5MHz
GPIO		Up to 168	Up to 168	Up to 133
Embedded Memories	FLASH	2M	2M	1M
	SRAM On AXI	512KB	**1024KB**	**320KB (inc. 192KB shared with ITCM)**
	SRAM On AHB (D2 Domain)	288KB	**128KB**	**32KB**
	SRAM On AHB (D3 Domain)	64KB	**32KB**	**16KB**
	ITCM / DTCM	64KB / 128KB	64KB / 128KB	256KB (inc. 192KB shared with AXISRAM) / 128KB
	Backup SRAM	4KB	4KB	4KB
	RAMECC	ECC for all SRAMs	ECC only on ITCM, DTCM and L1 cache	ECC for all SRAMs (disabled in TCM above 520MHz)

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This and the following tables, show a comparison between the STM32H72/73, STM32H7A/7B and STM32H74/75 lines. The main differences are indicated in pink.
When the internal temperature does not exceed 105°C, the CPU can run at a frequency up to 550 MHz. At higher temperature, up to 140°C, the CPU can run up to 480 MHz.
To reach 550 MHz, the LDO can be used in the same way as for STM32H74/75 devices, but the STM32H72/73 microcontrollers can also use the SMPS regulator instead to improve power efficiency.
The STM32H72/73 line has only one bank of flash.
The total size of the RAMs connected to the

AXI bus matrix can reach 320 KBytes if the whole 192-KByte memory space shared with ITCM is dedicated to AXI RAM.
The size reduction comparisons for the RAMs connected to the AHB bus matrix located in D2 and D3 domain are shown in this table.
The RAM error code correction (ECC) is available on all L1 cache, TCM, AXI and AHB RAM. Note that, when the CPU is running above 520 MHz, the ECC on TCM RAM needs to be disabled.

H72/73 vs H7A/7B vs H74/75 features

		STH32H74x/75x	STH32H7Ax/7Bx	STH32H72x/73x
Exr. Mem.	FMC	1	1	1
	x-SPI	1x QuadSPI	2x OctoSPI/OTFDEC	2x OctoSPI/OTFDEC
Clock manag.	Int. Oscillators HSI / RC / CSI / LSI	64 MHz / 48 MHz / 4 MHz / 32kHz	64 MHz / 48 MHz / 4 MHz / 32kHz	64 MHz / 48 MHz / 4 MHz / 32kHz
	Ext. Oscillators HSE / LSE	4-50 MHz / 32.768 kHz	4-50 MHz / 32.768 kHz	4-50 MHz / 32.768 kHz
	PLLs	3	3	3
Reset and Power Ctrl	Power Domain	3	2	3
	SMPS	●	●	●
	Low Power modes	sleep, stop, standby, vbat	sleep, stop, retention, standby, vbat	sleep, stop, standby, vbat

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STM32H72/73 products embed also up to two OCTOSPI interfaces. An I/O manager supports the multiplexing of two external OCTOSPI memories on a single memory interface. For STM32H73, information protection data can be stored encrypted in the external OCTO SPI memory. When read, those data can de decrypted on the fly.
The three power domains are kept identical to STM32H74/75 devices.

H72/73 vs H7A/7B vs H74/75 features

		STH32H74x/75x	STH32H7Ax/7Bx	STH32H72x/73x
Timers	Basic / General Purpose / PWM / RTC	2 / 10 / 2 / 1	2 / 10 / 2 / 1	2 / 10 / 2 / 1 + 2 32-bit
	High Res / Low Power / Systick	1 / 5 / 2	0 / 3 / 1	0 / 5 / 1
Display / Graphics	TFT LCD controller	1	1	1
	MIPI-DSI / GFX-MMU/JPEG codec	1 / 0 / 1	0 / 1 / 1	0 / 0 / 0
	Chrom-ART Accelerator™ (DMA2D)	1	1	1
DMA	MDMA / Basic DMA / Dual port DMA	1 / 1 / 2	1 / 2 / 2	1 / 1 / 2
Communication interface	USART / UART / LPUART	4 / 4 / 1	5 / 5 / 1	5 / 5 / 1
	I2C	4	4	5
	SPI / I2S	6 / 3	6 / 4	6 / 4
	SAI	4	2	2
	SPDIFRX	4 inputs	4 inputs	4 inputs
	SWPMI	1	1	1
	MDIO	1	1	1
	SDMMC	2	2	2
	FDCAN / TT-CAN	1 / 1	1/ 1	2 / 1
	USB OTG	2 (1HS/FS, 1FS)	1 (HS/FS)	1 (HS/FS)
	ETHERNET	1	0	1
	HDMI-CEC	1	1	1
	DCMI (camera) / PSSI	1 / 0	1/1 (PSSI shares same interface w. DCMI)	1/1(PSSI shares same interface w. DCMI)

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Two general-purpose 32-bit timers have been added, the specific high-resolution timer is no more present and only one systick timer is present resulting from the single-CPU architecture.

To enhance display and graphic features, TFT LCD controller and Chrom-ART accelerator are still present. MIPI-DSI and JPEG decoder are not available.

One UART, one USART, one I2C and one FDCAN have been added.

One I2S has been added to one SPI interface, and the parallel synchronous slave interface (PSSI) feature have been added to the Digital camera interface.

The number of Serial Audio Interfaces (SAI)

has been reduced to two, one USB Full speed has been removed, keeping only one USB that can be configured in High Speed or Full Speed mode.

H72/73 vs H7A/7B vs H74/75 features

		STH32H74x/75x	STH32H7Ax/7Bx	STH32H72x/73x
Analog	16-bit ADC	3 (up to 20 channels)	**2 (up to 20 channels)**	**2 (up to 20 channels)**
	12-bit ADC (ADC3)	0	**0**	**1 (up to 19 channels)**
	12-bit DAC	2 channels	**1*2 channels + 1*1 channel**	**2 channels**
	Comparator	2	2	2
	OP amplifier	2	2	2
	Temperature Sensor (connected to ADC)	1(ADC3)	1 (ADC2)	1 (ADC3)
	Digital Temperature sensor (DTS)	0	1	1
	DFSDM	1 (8 ch / 4 filters)	**2 (8 ch / 8 filters, 2 ch / 1 filter)**	**1 (8 ch / 4 filters)**
Copro	FMAC	-	-	●
	CORDIC	-	-	●
Security	AES / HASH	● / ●	● / ●	● / ●
	RNG	1 (seed for NIST standard DRBG module)	1 (NIST certifiable)	1 (NIST certifiable)
	OTFDEC	0	**2**	2
	OSPI memory encryption	0	**2**	2
	RDP, WRP, ROP, PC-ROP	●	●	●
	Passive Tamper / Active Tamper	Up to 3 / -	Up to 3 / Up to 2	**Up to 2** / -
	Security services, RSS, secure only area	●	●	●
Debug wthdg	SWD / JTAG / ETM	● / ● / 4KB	● / ● / 4KB	● / ● / 2KB
	Watchdog	4	**2**	**2**

STM32H72/73 devices embed the same two 16 bits analog to digital converters (ADC) located in D2 power domain. The ADC located in D3 domain has been replaced by a 12bits ADC. The internal temperature can be measured thanks to a sensor connected by default to ADC3 or through a digital sensor to avoid the ADC usage.
Two accelerators have been added: The Cordic coprocessor accelerates certain mathematical functions, mainly trigonometric ones, and the FMAC accelerator performs arithmetic operation on vectors.
The Random Number Generator, RNG, is a NIST SP 800-90B compliant entropy source.
The two embedded On The Fly Decryption

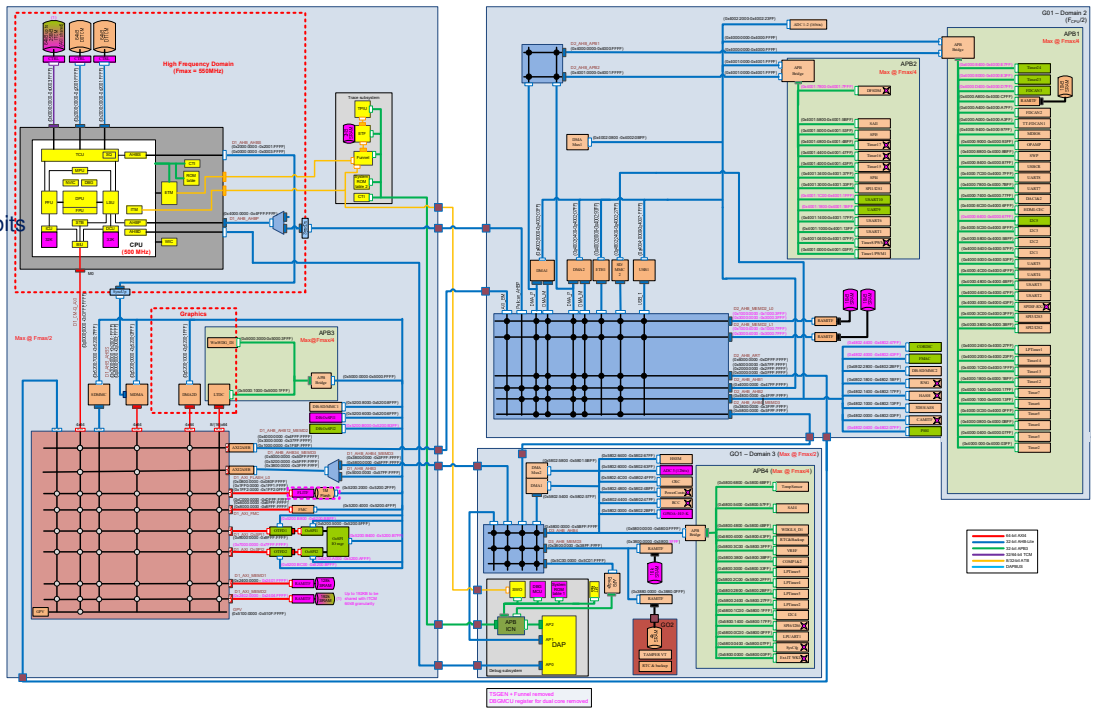
units, OTFDEC, allow the on-the-fly decryption of content stored in external OCTOSPI memories. The procedure to use encrypted data is described in a dedicated application note, AN5281.
The OTFDEC feature is only available for STM32H73 crypto devices.
The STM32H72/73 are single-CPU core devices, so only one independent watchdog and one window watchdog are included.

STM32H72x/73x ARCHITECTURE

Changes STM32H74x/75x versus STM32H72x/73x

New IP or HW in STM32H72x/73x

- FLASH 2MB to 1MB
- L1 cache 2x16KB to 2x32KB
- System RAM size updated
- TIM23 24 added
- QSPI to OcSPI subsys updated
- 1xFDCAN added
- UART9 / USART10 added
- D3 ADC changed from 16 to 12bits
- FMAC & CORDIC added
- ETM 4kB to 2kB
- I2C5 added
- SPI6/I2S6 updated
- CM4/ART removed
- WinWDG_D2 removed
- WDGLS_D2 removed
- 3 down to 2 D2 SRAM layers
- HRTIMER removed
- DSI removed
- USB2 removed
- JPEG removed
- D2 SAI2/SAI3 removed
- GPIO I removed



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The presentation shows in green the implementation of the IPs added to STM32H74/75 devices. They will be detailed in the next slides.

STM32H72x/3x D1 domain, CPU

FLASH 2MB to 1MB
L1 cache 2x16KB to 2x32KB
System RAM size updated
TIM23 24 added
QSPI to OcSPI subsys updated
1xFDCAN added
UART9 / USART10 added
D3 ADC changed from 16 to 12bits
FMAC & CORDIC added
ETM 4kB to 2kB
I2C5 added
SPI6/I2S6 updated
CM4/ART removed
WinWDG_D2 removed
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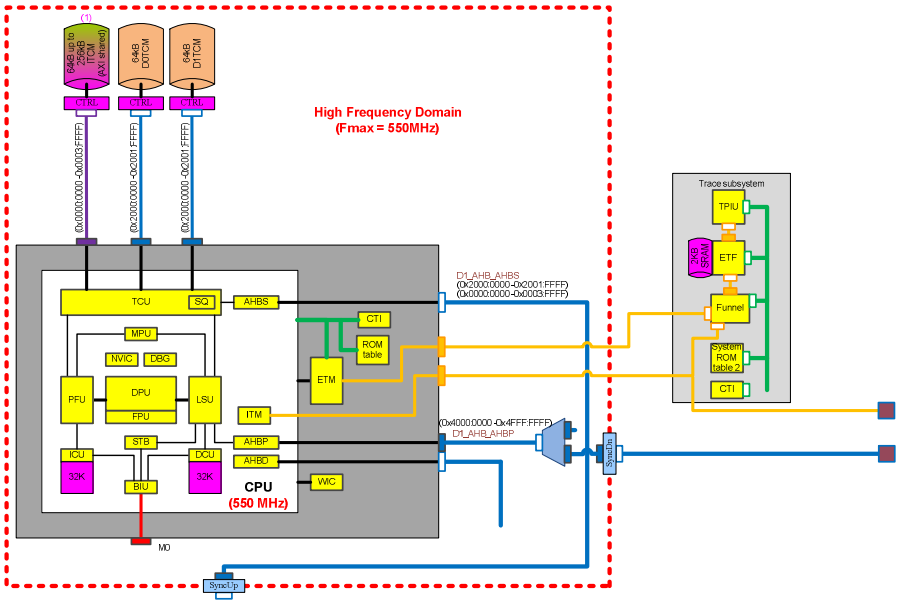
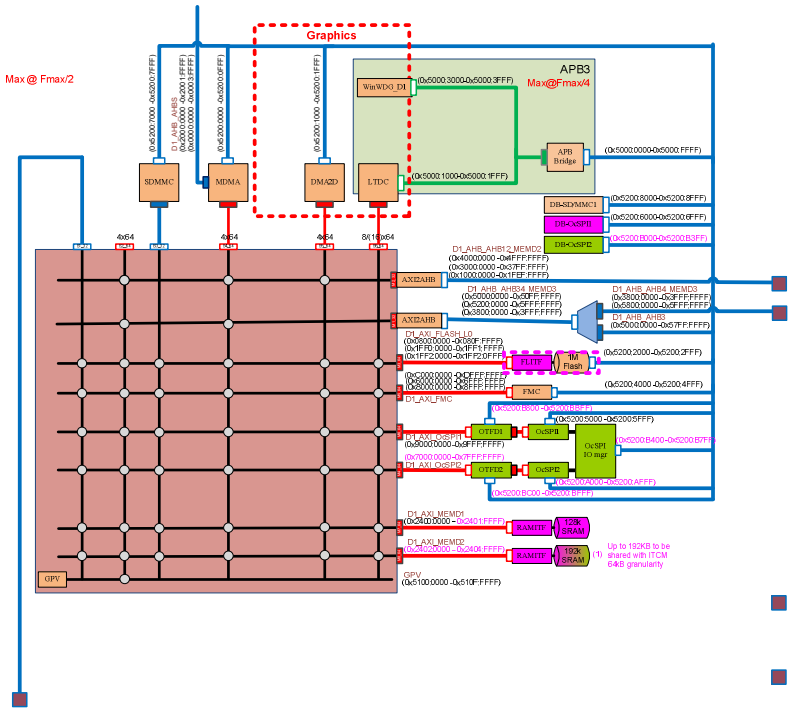
3 down to 2 D2 SRAM layers
HRTIMER removed
DSI removed
USB2 removed
JPEG removed
D2 SAI2/SAI3 removed
GPIO I removed



The size of L1 data and instruction cache closely connected to the core have been doubled to 32 Kbytes.
The ITCM size is flexible. On top of fixed 64 bytes, 192 Kbytes Of RAM can be connected either to ITCM or AXI SRAM.
The CPU and those close RAMs can run up to 550 MHz.
The size of RAM dedicated to the debug trace is reduced from 4 Kbytes to 2 Kbytes.

STM32H72x/3x D1 domain, AXI

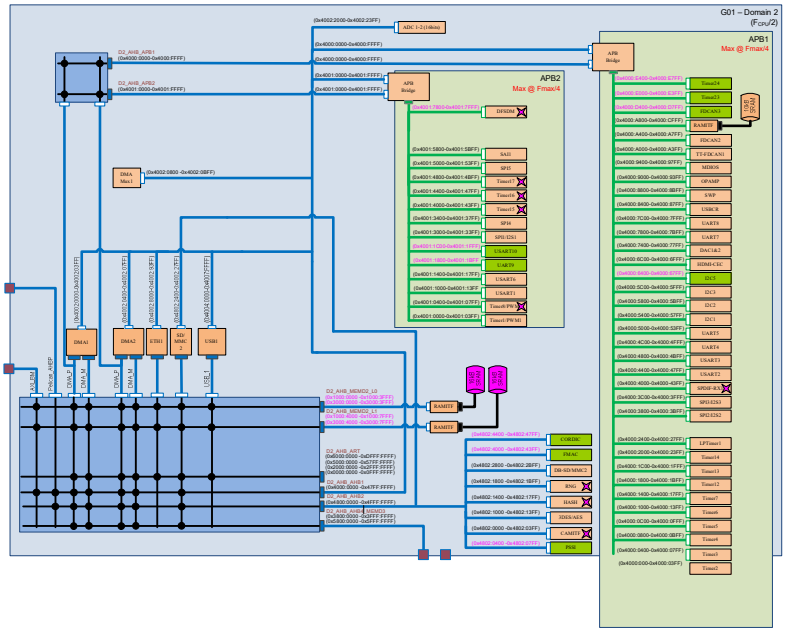
FLASH 2MB to 1MB
L1 cache 2x16KB to 2x32KB
System RAM size updated
TIM23 24 added
QSPI to OcSPI subsys updated
1xFDCAN added
UART9 / USART10 added
D3 ADC changed from 16 to 12bits
FMAC & CORDIC added
ETM 4kB to 2kB
I2C5 added
SPI6/I2S6 updated
CM4/ART removed
WinWDG_D2 removed
WDGLS_D2 removed
3 down to 2 D2 SRAM layers
HRTIMER removed
DSI removed
USB2 removed
JPEG removed
D2 SAI2/SAI3 removed
GPIO I removed



Only one flash memory bank is connected to the AXI matrix.
Two slave ports of AXI matrix are used for OCTOPSPI instead of one for the Quad SPI on STM32H74/75 devices. On crypto STM32H73x devices, the OCTOSPI is connected to AXI through the On The Fly Decryption (OTFDEC), it can be activated or not.

STM32H72x/3x D2 domain

FLASH 2MB to 1MB
L1 cache 2x16KB to 2x32KB
System RAM size updated
TIM23 24 added
QSPI to OcSPI subsys updated
1xFDCAN added
UART9 / USART10 added
D3 ADC changed from 16 to 12bits
FMAC & CORDIC added
ETM 4kB to 2kB
I2C5 added
SPI6/I2S6 updated
CM4/ART removed
Removed WinWDG_D2 & WDGLS_D2
3 down to 2 D2 SRAM layers
HRTIMER removed
DSI removed
USB2 removed
JPEG removed
D2 SAI2/SAI3 removed
GPIO I removed



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In D2 domain, two 32bit timers , one FDCAN and one I2C have been added on APB1 bus.
One USART and one UART have been added to APB2 bus.
The two accelerators CORDIC and FMAC and the PSSI have been added to AHB2 bus

STM32H72x/3x D3 domain

FLASH 2MB to 1MB
L1 cache 2x16KB to 2x32KB
System RAM size updated
TIM23 24 added
QSPI to OcSPI subsys updated
1xFDCAN added
UART9 / USART10 added
D3 ADC changed from 16 to 12bits
FMAC & CORDIC added
ETM 4kB to 2kB
I2C5 added
SPI6/I2S6 updated
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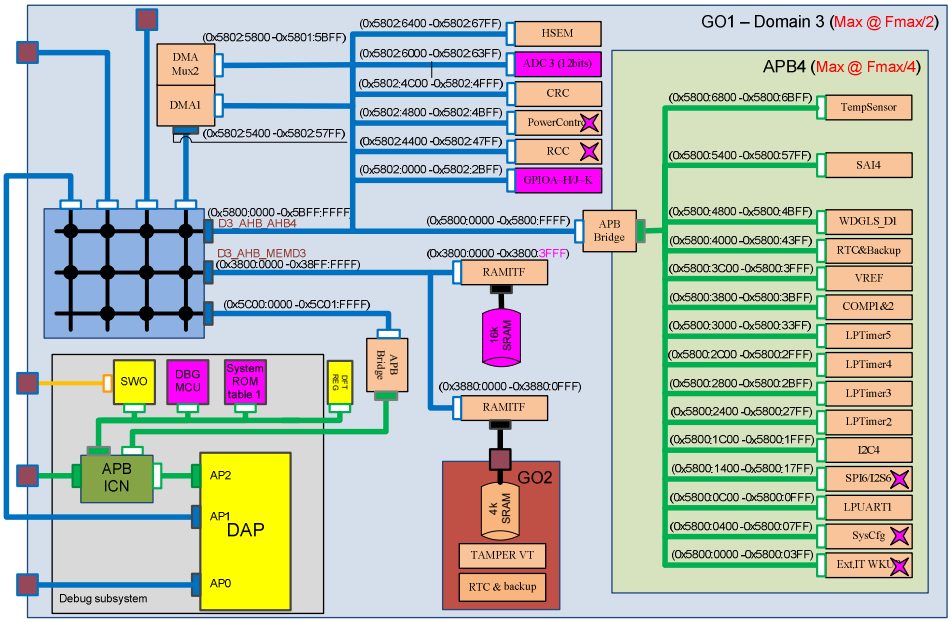

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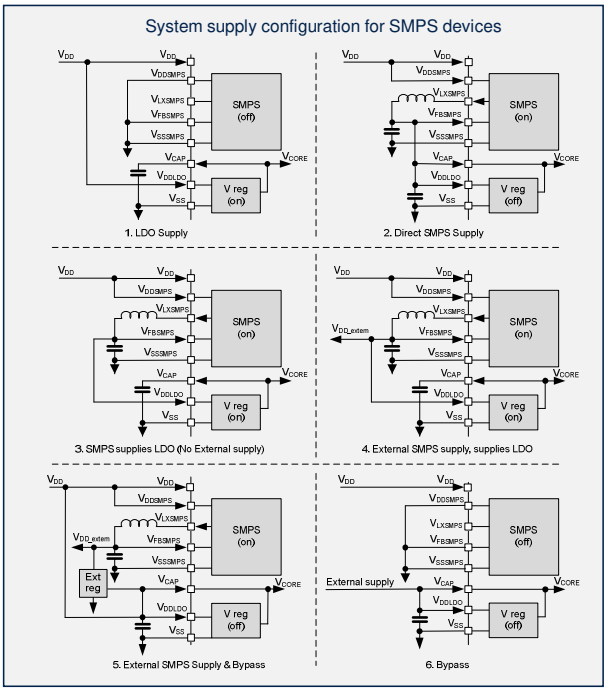
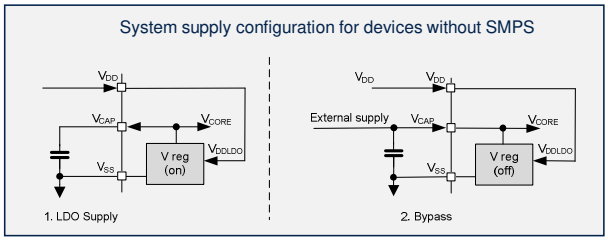
In D3 domain, the 16 bit ADC has been replace by low power 12 bit ADC. The SPI6 has now a I2S feature included.

PWR Supply





VDD: 1.62V – 3.6V (typical 3.3V)

Internal power supervisor:
For power-on: VPOR max: 1.71V (see datasheet)
For power-down: VPDR max: 1.68V
⇒Below 1.71V the internal power supervisor needs to be switched off setting the PDR_ON pin to V_{SS} and an external power supervisor needs to be used.

Note: PDR_ON pin is not available in all packages.
In such cases the internal power supervisor can't be switched off with consequence of a minimum VDD supply of 1.71V

See RM0468

The slide explains how to supply the device, the different possible configurations, the internal generated supplies and the different power modes.
The STM32H72/73 line has the same power supply scheme and power modes as STM32H74/75 line.
The STM32H725/735/730 lines embed also a Switch Mode Power Supply (SMPS) step down converter to improve power efficiency. All STM32H72x/73x devices embed a Low Drop Output (LDO) regulator except for the 68-pin package which embeds only the SMPS.
To provide the core supply, several system supply configurations are possible.
The digital power can be supplied either by the internal linear voltage regulator, the embedded SMPS step down converter or directly by an external supply voltage in regulator bypass mode. The SMPS step down converter can also be cascaded with the linear voltage regulator.

It’s important to connect the device according to these schematics to insure a correct power-up of the device. For devices not supporting the SMPS feature, only the LDO regulator is available. In this case two configurations are possible and the VDDLDO regulator supply is directly provided through VDD without a dedicated package pin.

Power scale extension

Power Scale	CPU max frequency (MHz)
VOS0 & ECC disabled on TCM	550
VOS0	520
VOS1	480
VOS2	300
VOS3	170

Power scale	Vcore source	Maximum Tj	Minimum VDD
VOS0	SMPS	105	2,2
	LDO		1,7
	SMPS supplies LDO		3
	external (Bypass)		1,62
VOS1	SMPS	140	2,2
		125	1,62
	LDO		1,62
	SMPS supplies LDO		2,3
	external (Bypass)		1,62
VOS2	SMPS	140	1,62
	LDO	125	1,62
	SMPS supplies LDO		2,3
	external (Bypass)		1,62
VOS3	SMPS	140	1,62
	LDO	125	1,62
	SMPS supplies LDO		2,3
	external (Bypass)		1,62
SVOS4/SVOS5	SMPS	140	1,62
	LDO	125	2
		105	1,62
	SMPS supplies LDO	125	3
		105	2,3
	external (Bypass)	125	1,62

The STM32H72/73 line domain usage of some power scale has been increased compared to STM32H74/75 line.

SMPS use is available for VOS0. In this domain, the CPU can reach its highest speed, which also means the highest dynamic current consumption. Using the SMPS instead of LDO reduces the power consumption; reducing the power consumption helps reduce the internal temperature, which in turn reduces the internal leakage in a virtuous circle.

In VOS1, the SMPS can be used with a junction temperature up to 140°C, which is possible only from VOS2 for STM32H75. It means that for this high temperature the maximum CPU speed is 480 MHz for the STM32H72/73 line instead of 300 MHz for the STM32H75 line.

SVOS4 and SVOS5 can be used 125°C instead of

105°C, which eases the usage of those low power modes at high temperature.
The maximum frequency in VOS3 is decreased from 200 MHz to 170 MHz.

Consumption

			STH32H74x/75x	STH32H7Ax/7Bx	STH32H72x/73x
RUN(LDO/SMPS)	550 MHz		-	-	**145 / 81 mA**
	480 MHz		148 / - mA	-	**125 / 72 mA**
	400 MHz		110 / 58 mA	-	**90 / 47 mA**
	280 MHz		71 / 35 mA	70 / 34 mA	58 / 29 mA
	60 MHz		16 / 7.5 mA	**12.5 / 5.5** mA	13.5 / 6.5 mA
LP mode (LDO/SMPS)	D1/D2/D3 stop (CD/SRD Dstop2)	SVOS3	2.8 / 1.0 mA	**0.115 / 0.046** mA	1.15 / 0.25 mA
		SVOS5	1.3 / 0,36 mA	**0.09 / 0.032** mA	0.5 / 0.05 mA
	D1/D2/D3 standby (CD/SRD standby)		2,0 µA	2,2 µA	2.5 µA
	VBAT		0.03 µA	0.03 µA	0.02 µA

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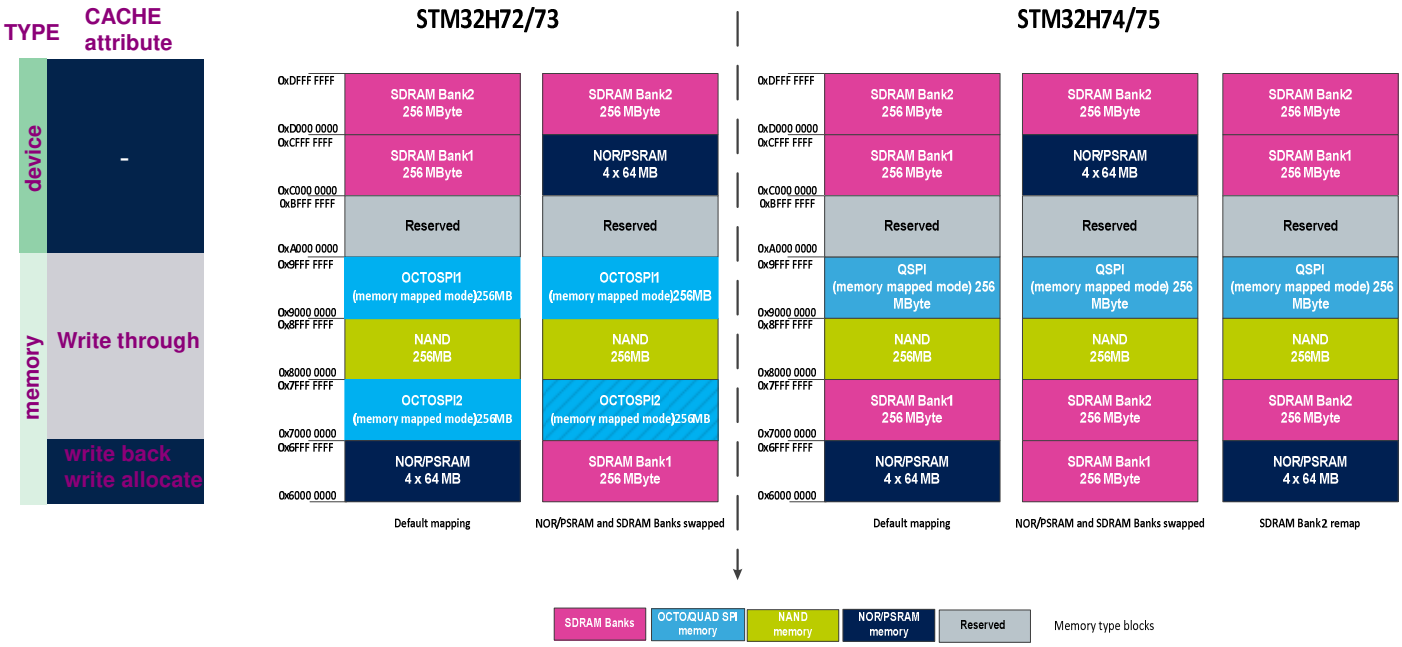
This table shows typical consumption for LDO slash SMPS for voltage supply of 3.3V. Comparison of line 550 MHz and 480 MHz shows that STM32H72/73 line reaches a higher performance with a slight consumption decrease using LDO. This becomes a huge decrease when using SMPS.

Bank swapping for external memory



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Modifications regarding internal RAM memories and peripherals imply a modification of the memory mapping. Due to the presence in default mapping of OCTOSPI2 in place of FMC's SDRAM Bank1, the STM32H72/73 line does not propose the remap of the FMC's SRD bank2. Only the FMC's SDRAM bank1 can be remapped.

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Thank you!