Hello, and welcome to this presentation of the RAM configuration controller which configures the features of the internal SRAMs: SRAM1, SRAM2, SRAM3, and Backup SRAM.

RAM Configuration Overview

- Error code correction
  - ECC on SRAM1/2 & BKPSRAM for STM32H503 devices
  - ECC on SRAM2/3 & BKPSRAM for STM32H563/H573 and STM32H562 devices
- SRAM-ECC software disable with keys
- SRAM software erase with key
- Write protection (1-Kbyte granularity on SRAM2)

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The RAM configuration controller is in charge of:
- Handling the error code correction, or ECC
- Disabling ECC through a software sequence based on a key register
- Performing global SRAM erasure through a software sequence also based on a key register
- Protecting SRAM2 against write accesses for each 1-KB chunk.

The STM32H503 microcontroller differs from STM32H56X and STM32H573 regarding the SRAM features:
- STM32H503 supports ECC on SRAM1, SRAM2 and backup SRAM
- STM32H56X and STM32H573 support ECC on SRAM2, SRAM3 and backup SRAM.

SRAM3 is present only in STM32H56X and STM32H573.

SRAMs Features

X = supported feature	STM32H563/H573 and STM32H562 devices				STM32H503 devices		
	SRAM1 (256 KB)	SRAM2 (64 KB)	SRAM3 (320 KB)	BKPSRAM (4 KB)	SRAM1 (16 KB)	SRAM2 (16 KB)	BKPSRAM (2 KB)
Optional retention in Standby	-	-	-	X	-	-	X
Optional retention in VBAT	-	-	-	X	-	-	X
Erased with product state regression	X	X	X	X	X	X	X
Erased with tamper detection	-	X	-	X (Optional)	-	X	X
Optionally erased with system reset	X	X	X	-	X	X	-
Software erase	X	X	X	X	X	X	X
ECC	-	X	X	X	X	X	X
Write protection	-	X	-	-	-	X	X (Optional)

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This table summarizes the features of the internal SRAMs.
Let us start with the features supported by all internal SRAMs:

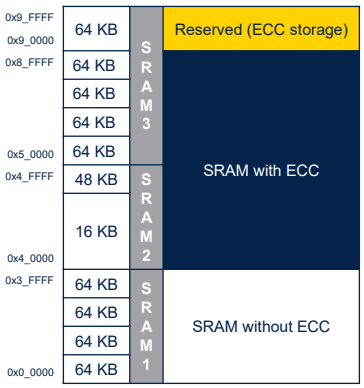
- Automatic erasure when product state regression is performed
- Capability of software-initiated erasure
- All SRAMs, except the backup SRAM, can be erased on a system reset.

The contents of backup SRAM is retained in standby and VBAT modes.
SRAM2 and optionally backup SRAM are protected by the tamper detection circuit and are erased by hardware in case of tamper detection.
The ECC is supported by SRAM1, SRAM2, SRAM3 and

backup SRAM, depending on the exact reference of the microcontroller, when enabled with the related option bits. The SRAM2 is made of 64 1-Kbyte pages. Each 1-Kbyte page can be write-protected by setting its corresponding PxWP bit in configuration registers.

SRAM2/3 memory map with ECC STM32H56X, STM32H573

- STM32H563/H573 and STM32H562 devices
  - The ECC is supported by SRAM2(64KB), SRAM3(256KB) and BKPSRAM
  - ECC Storage:
    - SRAM3: 64 Kbytes area, the upper block
    - SRAM2: the data bus is 39-bits (7-bits for ECC Storage and 32-bits for data) so that the entire SRAM2 is ECC protected
  - SRAM3 ECC specific management:
    - When ECC is enabled, only the first 256KB of SRAM3 are with ECC
    - The next block of 64 Kbytes is without ECC, it is used to store the ECC so it cannot be used for application
- ECC
  - SEDC: Single Error Detection Correction (Interrupt)
  - DED: Double Error detection (interrupt or NMI)



This slide describes the SRAM1, SRAM2 with ECC and SRAM3 with ECC memory map for STM32H56X and STM32H573 devices.
Four 64-KB blocks of SRAM3 and the 64 kilobytes of SRAM2 are ECC protected.
Regarding SRAM3, the ECC codes are stored in a dedicated part of the SRAM: the upper 64-kilobyte part of SRAM3. This area shall not be used by applications.
Regarding SRAM2, the information which is stored is 39-bit wide, 32-bit data +7-bit ECC. Consequently the entire SRAM2 is ECC protected.
ECC error detection is reported to the Cortex-M33 as follows:

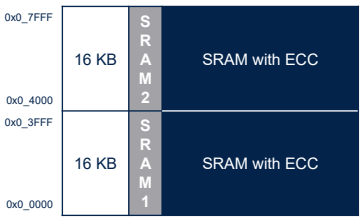
- Single error detection and correction cause a maskable

interrupt request

- Double error detection causes a non-maskable interrupt or a maskable interrupt
- The failing address is latched in a register.

SRAM1/2 memory map with ECC STM32H503

- STM32H503 devices
  - The ECC is fully supported by SRAM1(16KB), SRAM2(16KB) and BKPSRAM
- ECC
  - SEDC: Single Error Detection Correction (Interrupt)
  - DED: Double Error detection (interrupt or NMI)



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This slide describes the SRAM1 and SRAM2, both with ECC, memory map for STM32H503 devices.
The 16-KB SRAM1 and 16-KB SRAM2 are ECC protected, through seven ECC bits added per 32 bits of SRAM.
The error report mechanism is the same as the one implemented in STM32H56X and STM32H743.

Activating/Deactivating ECC by software

- When ECC is enabled (by user option bits), the ECCE bit is automatically set after system reset
- The ECC can be deactivated by executing a software sequence:
  - This helps to check ECC effects on the application
- Only for STM32H563/H573 and STM32H562 devices
  - When ECC is deactivated (ECCE = 0), the SRAM3 ECC storage area can be read and written for ECC user test purposes
  - When the ECC is activated (ECCE = 1), this area is reserved for ECC storage purposes and cannot be read nor written

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ECC can be automatically enabled by programming user option bits in the flash memory.
ECC can be disabled by executing a software sequence that writes keys into ECC key registers.
Since ECC requires a read-modify-write operation when writing partial data (byte or halfword), the performance can be measured with and without ECC.
When ECC is disabled in SRAM3, the last 64 kilobyte block containing the ECC codes is accessible by masters. This can be used for error injection.
When ECC is enabled in SRAM3, this area is reserved and cannot be accessed by masters.

Write protection (SRAM2)

- The SRAM2 is made of
  - 64 x 1-Kbyte pages of granularity for STM32H563/H573 and STM32H562 devices
  - 16 x 1-Kbyte pages of granularity for STM32H503 devices
- Each 1-Kbyte page can be write-protected independently
- Write protection can be enabled on page x by setting the PxWP bit in *RAMCFG_RAM2WPR1* and *RAMCFG_RAM2WPR2*

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The SRAM2 is made of 64 1-Kbyte pages. Each 1-Kbyte page can be write-protected by setting its corresponding PxWP bit in the RAMCFG memory 2 write protection 1 and 2 registers.
Two registers are necessary to form a bitmap of 64 bits.
The consequence of attempting to write to write-protected page is that the SRAM controller returns an error response to the AHB master.
When this master is the Cortex-M33 CPU, this error causes a bus fault exception.
When this master is a DMA channel, this error is interpreted as a DMA transfer error.

Software erase

- SRAM erase can be requested by executing a software sequence
- In case of read/write access to SRAM while ongoing erase to the same address, then wait states (AHB cycles) are automatically inserted until the end of the erase
- Total erase duration :

  N AHB clock cycles, where N is the size of the SRAM in 32-bit words
- Note: not possible to access the RAM during an erase cycle:
  - SRAMBUSY flag is set in the SRAM interrupt status register as long as the erase is ongoing
  - Accesses are blocked
  - Wait states are inserted on the AHB bus until the end of the erase operation

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SRAM erase can be requested by executing a software sequence, based on keys that have to be written to key registers.
SRAMBUSY flag is set in the related SRAM interrupt status register as long as the erase is ongoing.
The total duration of each SRAM erase is equal to N AHB clock cycles, where N is the size of the SRAM in 32-bit word units.
If the SRAM is read or written while an erase is ongoing, wait states are inserted on the AHB bus until the end of the erase operation.
SRAM erase can be requested by executing a software sequence:

1. Write 0xCA in the *RAMCFG SRAM x erase key*

register (RAMCFG_RAMxERKEYR).

2. Write 0x53 in the *RAMCFG SRAM x erase key register (RAMCFG_RAMxERKEYR)*.
3. Write 1 in the SRAMER bit of the *RAMCFG SRAM x control register (RAMCFG_RAMxCR)*.

RAMCFG interrupt

- Interrupts:
  - SEDC with interrupt generation
  - DED with interrupt or NMI generation
  - SEDC and DED status
  - Failing addresses are latched in registers

	Interrupt event	Exit Sleep mode	Exit Stop mode	Exit Standby modes
RAMCFG	ECC single error detection and correction	Yes	No	No
	ECC double error detection when DEIE = 1 and ECCNMI = 0	Yes	No	No
NMI	ECC double error detection when ECCNMI = 1	Yes	No	No

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The RAM configuration controller generates the following interrupt requests:

- A regular interrupt in the event of a single error detection and correction
- The non-maskable interrupt or a maskable interrupt in the event of a double error detection.

Status registers provide the current status of these events, the address at which a correctable error has been detected and the address at which a non-correctable error has been detected.

Note that these addresses are locked until software clears the Address latch enable bit in the control register.

The table indicates the effect of low power modes on the RAM configuration controller.

Sleep mode has no effect, RAMCFG interrupts cause the microcontroller to exit the sleep mode.
In stop mode, the contents of RAMCFG registers and SRAM contents are kept.
However, ECC error interrupt or NMI does not cause the microcontroller to exit the stop mode.
In standby mode, the RAMCFG module is powered down and must be reinitialized after exiting standby.

Thank you

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Thank you for attending this presentation on the RAM configuration controller!
In addition to this presentation, you can refer to the presentation on power management.