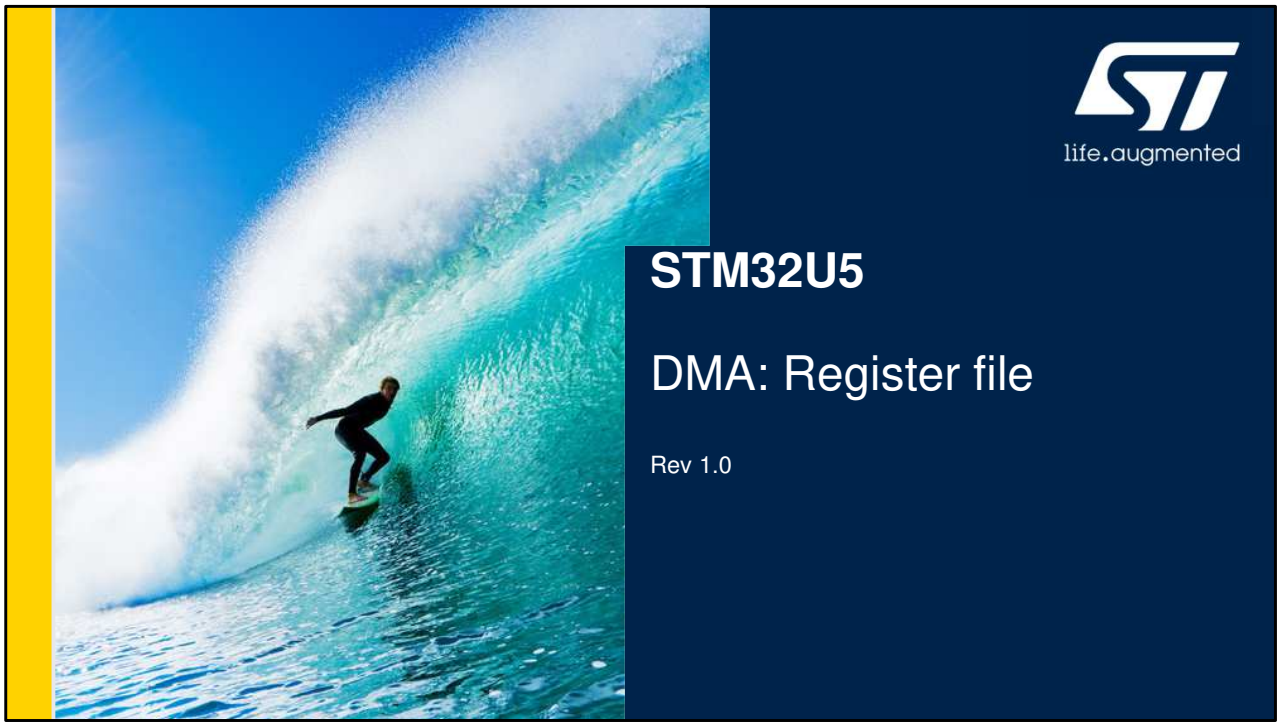
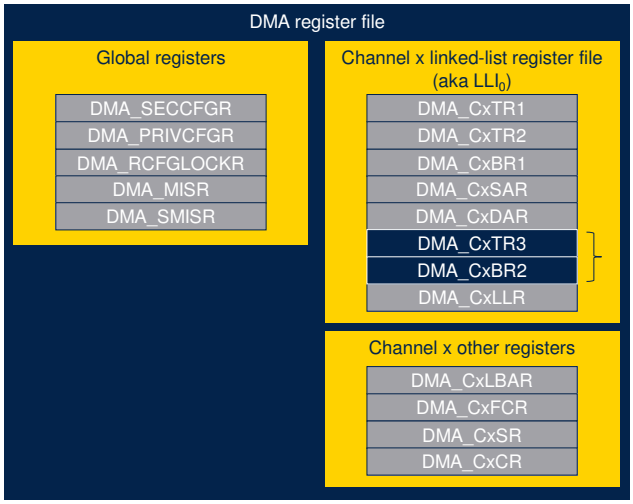


Hello, and welcome to this presentation, that describes the register file of GPDMA and LPDMA.

Register file



Present only in GPDMA channels 12-15

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The register file is composed of global registers applicable to all channels and channel related registers.
The channel related registers are split into the channel linked-list register file that can be updated during a link and the other registers that are not affected by links.
The registers CxTR3 and CxBR2 are only present in the GPDMA channels 12 to 15.
Here is a brief description of the global registers:

- The SECCFGR and PRIVCFGR registers configure the security and privilege attributes of each channel
- The RCFGLOCKR register is used to lock the secure and privilege settings until the next reset
- The MISR and SMISR are interrupt status registers for the non-secure and secure worlds.

Here is a brief description of the channel linked-list register file:

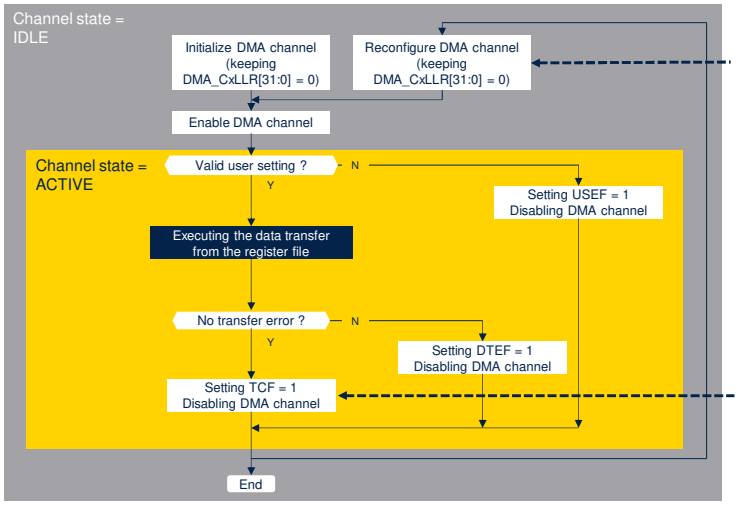
- TR1, TR2 and TR3 are transfer configuration registers
- BR1 and BR2 control the transfer at the block, respectively repeated block level
- SAR and DAR are the source and destination address registers
- LLR controls the link operation.

Here is a brief description of the other channel registers:

- LBAR points to the 64 kilobyte area containing the LLIs
- FCR is a flag clear register
- SR is a status register
- CR is a control register.

Channel direct programming (without linked-list)

(Keeping DMA_CxLLR[31:0]=0)



Direct reconfiguration only when channel is not enabled

- At least the (source and/or destination) memory start address(es) must be reprogrammed for setting up a continuous DMA service with a bounded buffer

Channel completion is at data transfer completion, either at:

- Block completion: BNDT[15:0]=0
- Repeated block completion for GP ch12-15: BRC[10:0]=BNDT[15:0]=0

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This figure describes the direct programming of the GPDMA channel without linked-list.
When GPDMA_CxLLR equals zero, no link occurs.
At the beginning, software initializes the channel by directly programming the channel related registers.
Then software enables the channel.
The DMA hardware checks the configuration and if an error is detected, the USEF flag is set and the channel is automatically disabled.
When there are no configuration errors, the DMA proceeds with the transfer.
If an error is encountered while the transfer is ongoing, the DTEF flag is set and the channel is automatically disabled.
When no transfer error is detected, the transfer completes

successfully and the Transfer Complete Flag or TCF is set. Channel transfer completes when BNDT[15:0] becomes equal to zero. This is the block number of data bytes to transfer from the source.
For channels 12 to 15 of GPDMA, the channel transfer completes when both the block repeat counter and the block number of data bytes to transfer become equal to zero.
A channel reconfiguration is possible only the when channel is disabled. Without link, software is in charge of reprogramming at least the source and or destination address to restart the same transfer.

DMA register file: GP vs LP

GP vs LP	
Regs/Additional Regs	**Additional Reg fields**
CxSR	FIFOL[7:0]: FIFO level
CxCR	LAP: link allocated port
CxTR1	DAP, SAP: source/destination allocated port DHX, DBX, SBX: byte reordering PAM[1]: packing/unpacking DBL_1[5:0], SBL_1[5:0]: source/destination burst length (0 to 64)
CxTR2	DREQ: Hardware request from destination
CxBR1 (ch12-15)	BRC[10:0]: repeated block counter SDEC, DDEC: source/destination increment/decrement (between bursts) BRSDEC, BRDDEC: source/destination increment/decrement (between blocks)
+ CxTR3 (ch12-15)	DAO[12:0], SAO[12:0]: source/destination address offsets (between bursts)
+ CxBR2 (ch12-15)	BRDAO[15:0], BRSAO[15:0]: source/destination address offsets (between blocks)
CxLLR	UT3 (conditional update of CxTR3) UB2 (conditional update of CxBR2)

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This table highlights the difference in terms of register file between the GPDMA and the LPDMA.
The channel status register of the LPDMA has no FIFO level field, because the LPDMA does not support channel FIFOs.
The channel control register of the LPDMA has no field to select the AHB master port used to perform the link transfer, because it supports a unique master port.
Similarly the transfer register 1 of the LPDMA has no field to select the AHB master port used to perform the data transfer, because it supports a unique master port.
Since the LPDMA channels do not include a FIFO, data manipulation such as byte reordering, packing and unpacking operations are not supported.

Unlike the GPDMA, the LPDMA does not implement bursts, only block transfers.
There is no field to select the hardware request from the destination peripheral in the LPDMA, because it only supports requests from the source peripheral.
Only the channels 12 to 15 of the GPDMA have the capability of repeating block transfers and adding a signed offset between consecutive bursts and blocks.
These offsets are programmed in TR3 for the burst offset and BR2 for the burst offset, only present for these channels.
As a consequence, the user can decide to update these registers when a link is performed, by programming the UT3 and UB2 control bits.

Thank you

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In addition to this presentation, you can refer to the other presentations on the GPDMA and LPDMA:

- DMA overview
- DMA transfers hardware and software views
- Autonomous DMA & low power mode
- DMA : Linked list
- DMA Circular buffering & double buffering
- DMA 2D addressing
- DMA Error reporting
- DMA Input-output LLI control.