Hello, and welcome to this presentation of the STM32MP1 series External Memories Overview.
This presentation quickly summarizes some key points for the selection of external memories and the related constrains for an application using STM32MP1 series devices.

Flash memory

Let’s start to see which kind of Flash memories can be used with the the STM32MP1 Series.

Introduction

- Flash memories are non volatile memories used to store code and/or data
- In high speed system based on microprocessors, the external Flash technology and/or external interface are a bottleneck for performances.
  - Need a working memory as intermediate workspace (usually a Dynamic RAM due to size required by Rich Operating Systems like Linux).
- In an Operating System environment (e.g. Linux), Flash memories are always used with a file system driver
  - Support of new Flash devices could require SW/Ecosystem adaptation
- If needed, more than one Flash can be used in a system
  - To get advantage of each technology (e.g. NOR for reliability, NAND for price)
  - To separate content types (e.g. One Flash for Linux kernel, One Flash for data Filesystem)

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Flash memories are used to store code and/or data. Due to the high processing performance required, accessing code and/or data become a bottleneck and an intermediate workspace, such as an external DDR, is always required.
In an Operating System environment, the Flash memory is managed as a file system, so “execute in place” (XIP) is not possible and the Flash memory always needs a specific driver tailored to each particular device.
In most systems, there is more than one Flash to cope with the strength or the weakness of each type of Flash technology or to separate storage to increase performance, security or user-flexibility.

Flash devices Vs Characteristics

Flash Device	Flash Technology	PCB area	Cost Vs Density	Reliability	Read Perf.	Erase/Write Perf.
Serial-NOR	NOR	★★★★	★	★★★★	★★	★
Serial-NAND	SLC-NAND	★★★★	★★	★★★	★★	★★
Raw-NAND	SLC-NAND	★★	★★★	★★★	★★★	★★★
***e*•MMC**	SLC/MLC-NAND	★★★	★★★★	★★★	★★★★	★★★★
Removable Device						
SD-Card	MLC-NAND	★	★★★★	★★	★★★	★★★
USB Stick	MLC-NAND	★	★★★★	★★	★★★★	★★★★

SLC = Single Level Cell
MLC = Multiple Level Cell

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This table summarizes most of the differences between the various Flash technologies that can be used in an STM32MP1 microprocessor system.
Serial-NOR Flash technology has a very good PCB area (due to the low pin count of serial devices) and very good reliability. The cost of high density and the write performances are the bottleneck to the use of NOR Flash memories for large storage.
Serial-NAND Flash technology has a very good PCB area, and better cost and write performances than the Serial-NOR Flash technology. Reliability is often seen as being lower than for the Serial-NOR Flash technology, but error correction is embedded in the HW and transparent to the file system.
Raw-NAND technology has a parallel interface which, if not good for PCB area, does offer a good tradeoff between cost

and performance. Most Raw-NAND memories do not have embedded error correction and therefore need additional HW and file system management, for example, bad block management and wear leveling.
eMMC devices are widely used in the mobile phone market, and therefore offer very good price and performance. eMMC memories embed error correction as well as fully automatic bad block management and wear leveling.
Removable devices such as SD-Cards or USB sticks provide very good cost at large density, but at the expense of lower flexibility and reliability due to user access and mechanical constrains.

Interfaces Vs Flash devices

Flash Device	USBH	SDMMC	FMC	QUADSPI	Number of wires	Comments
Serial-NOR				☑	4 to 6	1 to 4 bits up 2x4 bits devices
Serial-NAND				☑	4 to 6	
Raw-NAND			☑		14 to 22	8 or 16 bits, 8 bits ECC 2xCS for 8 bits devices
e•MMC		☑			3 to 10	1 to 8 bit width
Removable Device						
SD-Card		☑			6 (10 wires for UHS-I)	1 to 4 bit width
USB Stick	☑ (Not Bootable)				2	*For information only as not bootable and cannot be used without another Flash*

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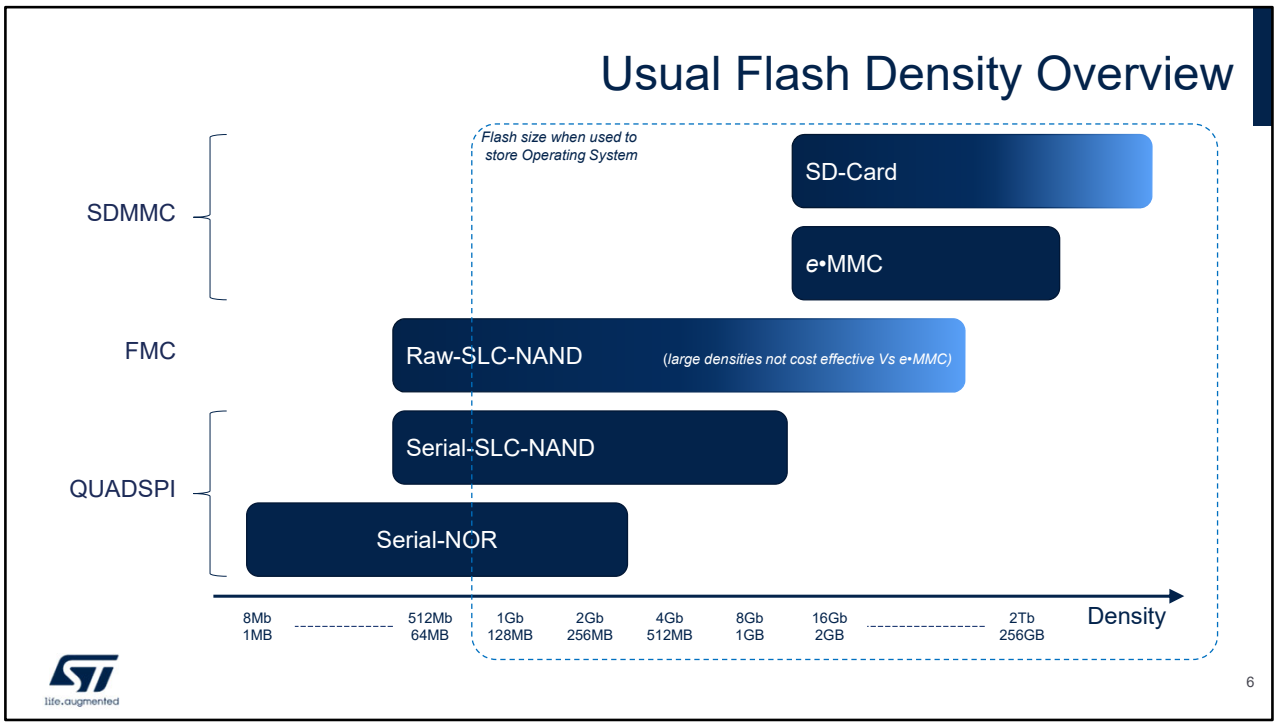
STM32MP1 Series can interface Serial-NOR and Serial-NAND memory devices through the QUADSPI interface, which can support up to two 4-bit devices. STM32MP1 Series can only boot from the first QUADSPI device.
Raw-NAND memories can be connected to the Flexible Memory Controller (FMC). The possible configurations are either one 8-bit or 16-bit device or two 8-bit devices sharing the same data bus. Only SLC devices requiring up to 8-bits ECC are supported. STM32MP1 Series can boot from Raw-NAND memory devices.
eMMC memories can be connected to any of the SDMMC interfaces (SDMMC3 has only 4-databits). eMMC devices support 1, 4 or 8-bit data width. STM32MP1 Series can boot from eMMC memory connected to the SDMMC2 interface.
SD-Card can be connected to any of the SDMMC interfaces.
STM32MP1 Series provides optional control for external level shifter (mandatory for the support of UHS-I mode which requires

3V then 1.8V signaling). STM32MP1 Series can boot from SD-Card connected to the SDMMC1 interface.



This slide shows the usual Flash density available by technology.
Note that a Flash memory with a size less than 1 Gbit (128 Mbyte) cannot be used alone, as such size does not allow storage of the operating system, but can store data anyways when used in conjunction with another, larger Flash holding the operating system itself.

DRAM memory

Let’s continue with DRAM memories supported by the STM32MP1 Series.

DDR fundamentals

- DDR stands for Double Data Rate Synchronous Dynamic Random Access Memory
- DDR technology needs ‘Refresh’
  - Uses ‘dynamic’ memory cell (i.e. a small capacitor), data is lost after some tens of milliseconds if not ‘refreshed’
  - ‘Refresh’ is done automatically by the STM32MP1 Series DDR controller or generated inside the memory when the system is in low power mode (Self-Refresh mode)
- Data are accessed in burst (usually 4 or 8 data of 16 or 32-bits each)
- STM32MP1 Series DDR Controller has the duty to interleave and optimize controls, read/writes/refresh to get maximum performances

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Here are some fundamentals about the DRAM technology. Despite their inherent complexity and constraints, dynamic RAMs are used in many devices as it is the only memory available with a very large density at an affordable price.

DRAM devices Vs Characteristics

DRAM Device	Supply	PCB area	Cost Vs Density	Dynamic Power	Standby Power	Performance
DDR3	1.5V	★★	★★★★	★	★	★★★★
DDR3L	1.35V	★★	★★★★	★★	★	★★★★
LPDDR2	1.2V & 1.8V	★★★★	★	★★★★	★★★★	★★★
LPDDR3	1.2V & 1.8V	★★★★	★★	★★★★	★★★★	★★★

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DDR3 technology has been superseded by DDR3L technology which offers the same performance but consumes less power.
LPDDR2 technology offers smaller packages and fewer signals on PCB than the DDR3/DD3L, and better power consumption, but usually has a higher price and needs two different supply voltages.

Interfaces to SDRAM devices

DRAM Device	Data width	Max Freq.	# of CS	# of ICs	# of wires	Comments
DDR3 / DDR3L	16-bits	533 MHz	1	1	50	DDR3L recommended for new designs
	32-bits	533 MHz	1	2	72	
LPDDR2 / LPDDR3	16-bits	533 MHz	1	1	36	16-bits less popular than 32-bits
	32-bits	533 MHz	1	1	58	

- DDR interface uses dedicated pins which cannot be reused for other purposes
- 32-bit interface only available on LFBGA448 and TFBGA361 packages

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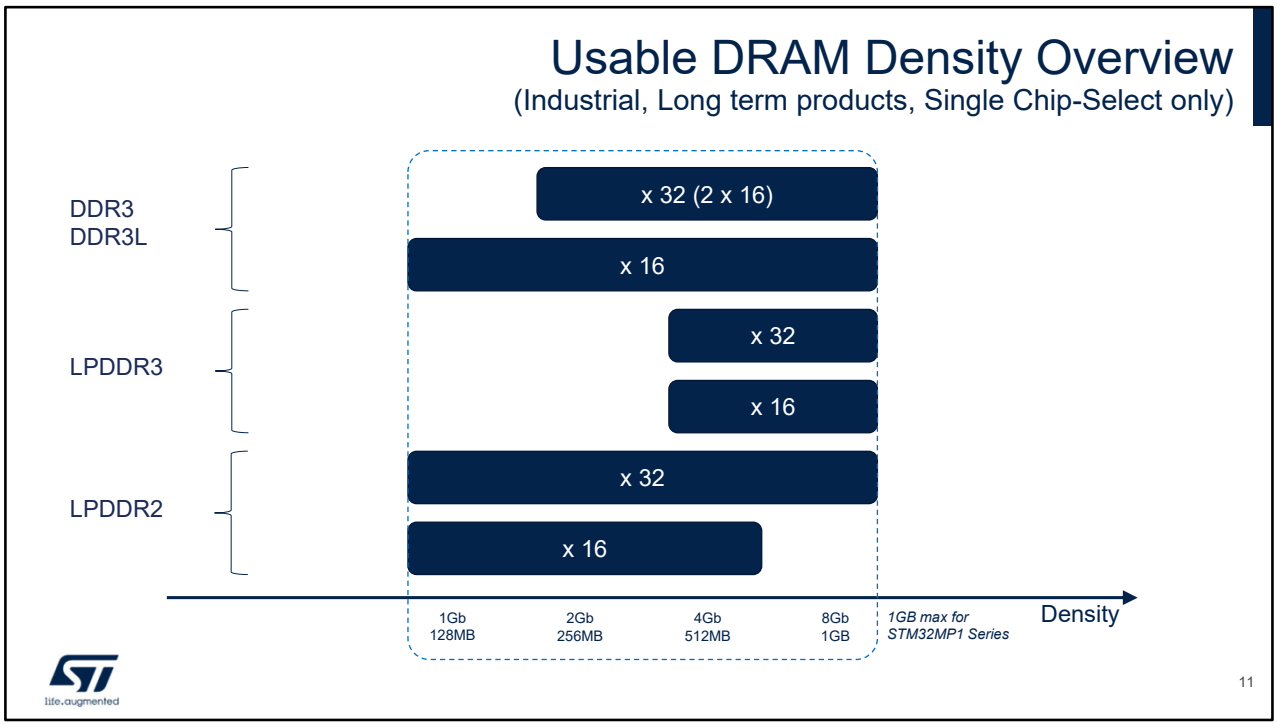
The STM32MP1 Series supports DDR3 or DDR3L memory devices in either 16-bit or 32-bit interface configuration (on some packages only). As neither DDR3 nor DDR3L memory devices exist with a 32-bit interface, this configuration requires two devices, using much more PCB space. Package ball pitch is 0.8 mm which is suited to industrial robustness.
LPDDR2 or LPDDR3 memory devices mostly exist in 32-bit versions and offer a lower signal count than DDR3/DDR3Ls. The package is smaller, but the pitch can be 0.65mm, 0.5mm or below, entailing additional PCB cost.



STM32MP1 Series supports between 1 Gbit (128 Mbytes) and 8 Gbit (1 Gbyte) of DRAM memory.

DDR interface PCB constrains (1/2)

- All DDR DRAM uses rising & falling clock edge for data transmission
  - 533MHz means one data sampled every 938 picoseconds
  - There is a pair of bidirectional data qualifier (DQSP/DQSN) for each 8-bit of data

- DDR3 uses On Die Termination (ODT) to adapt impedance to the PCB connections (stripline)
  - No ODT on LPDDR2 and LPDDR3 to save power, at the expense of additional signal integrity constrains
- DDR3 when used in x32-bits need two x16 devices, so Address/Command are routed to two packages
  - Need termination resistors on Address/Command lines at mid-supply (VTT voltage)
- Both STM32MP1 and memory need a mid-supply reference (VREF)
  - Very sensitive to noise, need to be carefully filtered

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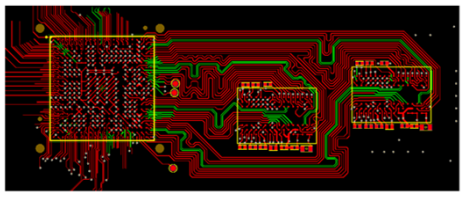
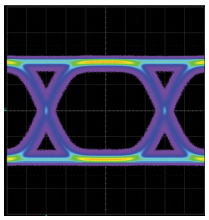
When designing a DDR system, DDR constraints must absolutely be taken into account. Refer to AN5031 and AN5122 for details.

DDR interface PCB constrains (2/2)

- Follow very carefully design guidelines, for example
  - Constrained signals length (e.g. +/-500µm within all signals in a byte including DQS)
  - Controlled impedance of PCB microstrips (e.g. 55 Ω single ended, 100 Ω differential)
  - Differential routing of CLKP/CLKN, DQSP/DQSN
  - Low clock jitter
  - Good supply decoupling and power planes
- STM32CubeMx provides a tool for tuning the DDR parameters as well as checking the signal integrity on the final target





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STM32CubeMx provides a tool that helps with tuning the DDR parameters and checking the DDR signal integrity directly on the final target.
More details are provided in the ecosystem training part.

Standards

- DRAM are specified by the following JEDEC standard
  - Standard interface and commands
  - Standard timings
  - Standard packages and ballout
- DDR3 ➔ JESD79-3F
- DDR3L ➔ JESD79-3-1A (Addendum to DDR3)
- LPDDR2 ➔ JESD209-2B
- LPDDR3 ➔ JESD209-3C

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All related DDR specifications are standardized through JEDEC.

Summary

- Keys points
  - External Flash are required in all SMT32MP1 Series systems
  - DDR SDRAM are complex high speed devices and need careful PCB design
  - DDR3L (1.35V) is recommended for cost and price sensitive solutions, while LPDDR2 or LPDDR3 are recommended when power is a concern
  - LPDDR2 or LPDDR3 x32 are smaller than two DDR3L, but need higher cost PCB due to pitch 0.5mm
  - STM32CubeMx will provide support for DDR parameter tuning on target
- Recommended sizes

Operating system	Flash		SDRAM	
	Minimun	Recommended	Minimun	Recommended
Bare Linux	128 MBytes	2 GBytes or more	128 MBytes	512 MBytes
Weston or Android	4 GBytes	8 GBytes or more	512 MBytes	1 GByte

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The keys points to remember from this presentation are:

- STM32MP1 Series always needs an external Flash memory device.
- External DRAMs such as DDR3/DDR3L or LPDDR2/LPDDR3 devices require careful PCB design and signal integrity analysis
- And STM32CubeMx helps to configure and validate the DDR memory on the final target

The recommended Flash or SDRAM size depends on the operating system configuration.

Thank you

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