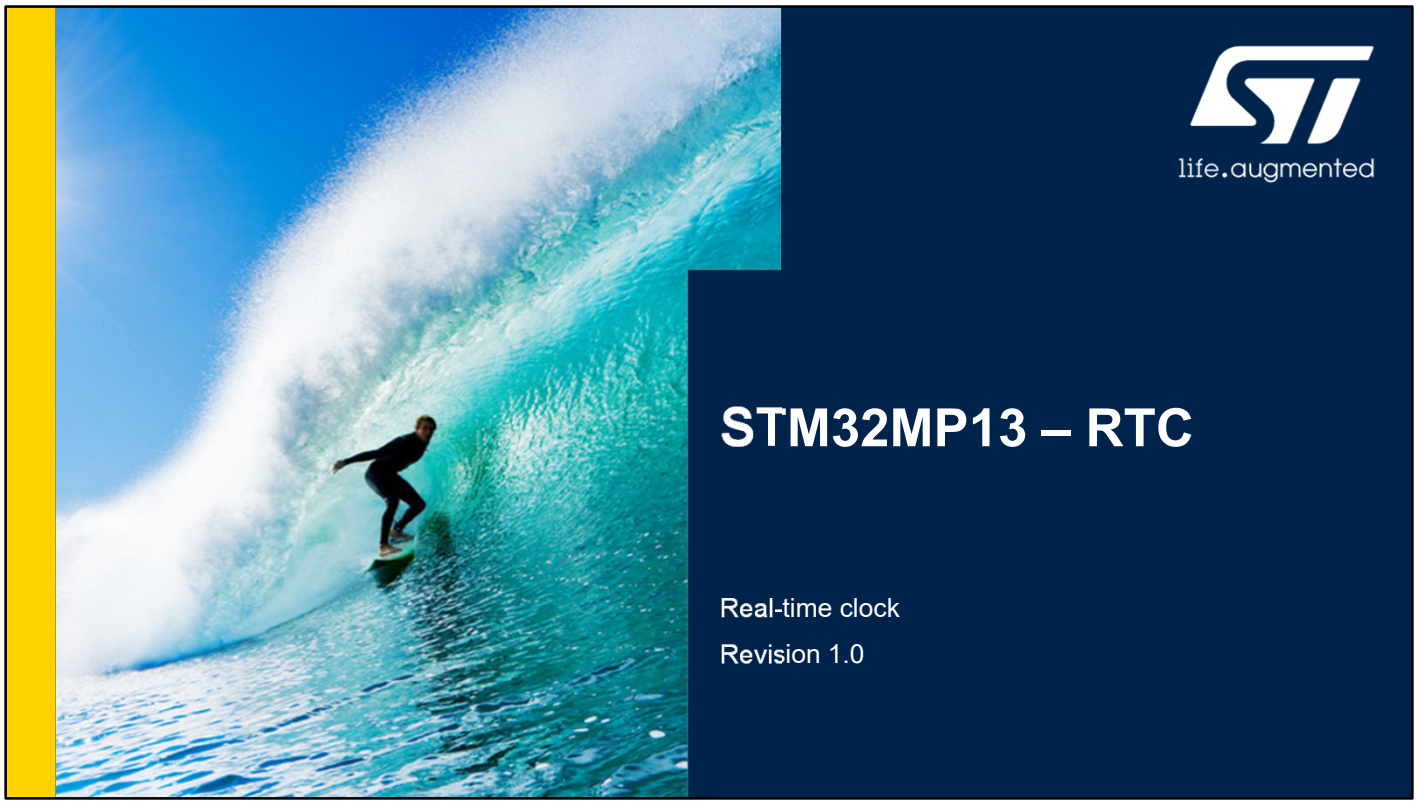
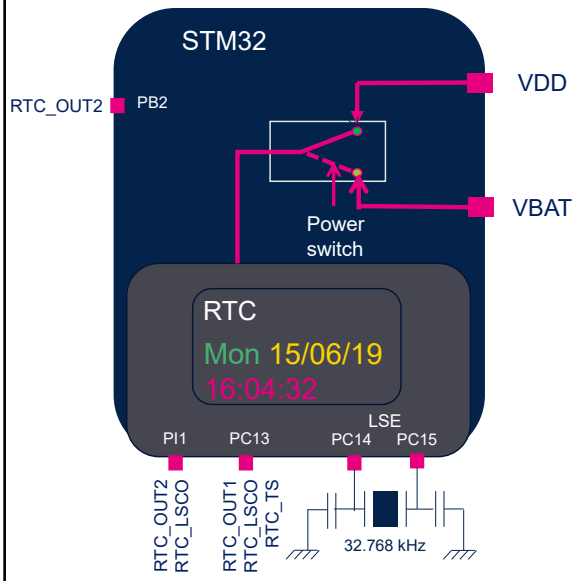


Hello, and welcome to this presentation of the STM32 Real-Time Clock. It covers the main features of this peripheral, which is used to provide a very accurate time base.

Overview



- The RTC provides an ultra-low-power hardware calendar with sub-second accuracy and alarms, available in all low-power modes
- Belongs to the Battery Backup Domain, so it is functional even when the main supply is off
- TrustZone support

Application benefits

- Ultra-low power: 1.5 µA at 3 V (w/ TAMP and LSE)
- Hardware BCD calendar to reduce software load
- Security isolation of each feature

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The RTC peripheral features an ultra-low power calendar with sub-second accuracy, and alarms, which run in all low-power modes.
Additionally, when it is clocked by the low-speed external oscillator (LSE) at 32.768 kHz, the RTC is functional even when the main supply is off and when the VBAT domain is supplied by a backup battery.
The RTC consumes 1.55 µA at 3 V, including the TAMP peripheral with tamper detection active and LSE power consumption. The hardware calendar is provided in binary-coded decimal (BCD) format to reduce software load, particularly when the date and time must be displayed. Each feature of the RTC can be individually configured as secure, allowing different processes to share the peripheral while being protected from other non-secure firmware access.

Key features

- Sub-seconds, seconds, minutes, hours, week day, date, month, and year in BCD format
- “On-the-fly” programmable daylight savings compensation
- Two programmable alarms with wakeup interrupt function
- A periodic flag with programmable resolution, triggering wakeup interrupt
- A reference clock source (50 or 60 Hz) can be used to update the calendar
- Digital calibration circuit to achieve 0.95 ppm accuracy
- Time-stamp function for event saving with sub-second precision (1 event)
- TrustZone support and privilege protection:
  - RTC full protection against non-secure or unprivileged access
  - Alarm A, alarm B, wakeup Timer and timestamp individual protection against non-secure or unprivileged access

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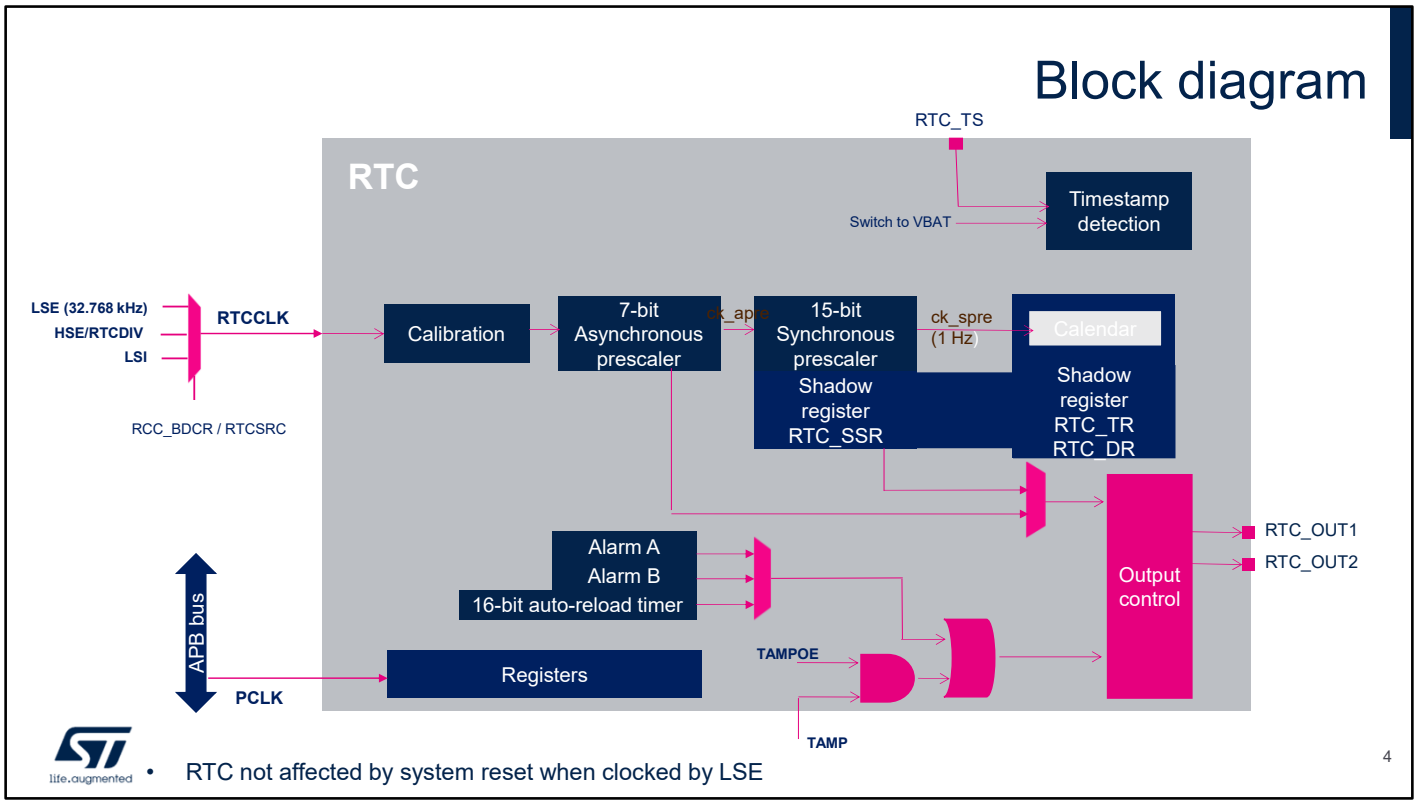
The key features of the RTC are as follows:

- Seconds, minutes, hours, week day, date, month, and year, provided in binary-coded decimal format. Sub-seconds are provided in binary format.
- Adding or removing one hour on the fly to the calendar, in order to manage daylight savings.
- Two programmable alarms, which can wake up the microprocessor from all low-power modes.
- An embedded auto-reload timer, which can be used to generate a periodic flag or interrupt with wakeup capability. The resolution of this timer is programmable.
- The calendar can be calibrated thanks to a reference clock source which is the mains at 50 or 60 Hz.
- A digital calibration circuit allowing compensation of the crystal accuracy, with 0.95 ppm resolution.
- A timestamp function to save calendar contents in timestamp registers, depending on an external event.
- Trustzone support with the possibility of securing each

feature individually in order to protect its registers against non-secure access. The RTC can also be globally configured as secure.

- In the same way, each feature can be individually protected against unprivileged accesses. The RTC can also be globally protected against unprivileged accesses.



Here is the RTC block diagram. The RTC has two clock sources: the RTC clock (RTCCLK), used for the RTC timer counter, and the APB clock, used for RTC register read and write accesses. The RTC clock can use either the high-speed external oscillator (HSE), divided by a programmable factor from 1 to 64, the low-speed external oscillator (LSE), or the low-speed internal oscillator (LSI). To be functional in Stop or Standby mode, the RTC clock must use the LSE or LSI. To be functional in VBAT mode, the RTC clock must use the LSE.

The RTC clock is first divided by a 7-bit programmable asynchronous prescaler, which provides the ck_apre clock. Most of the RTC is clocked at the ck_apre frequency, so, in order to reduce power consumption, it is advisable to set a high asynchronous division value. The default value is 128. Then, a 15-bit programmable synchronous prescaler provides the ck_spre clock. Ck_spre must be 1 Hz in order to update the time, and date BCD registers in 1-second

increments. The sub-second register resolution is defined by the ck_apre frequency. By default, it is 256 Hz. The SSR register resolution is increased by reducing the asynchronous prescaler value. The asynchronous prescaler can also be bypassed; in this case the sub-second register resolution is defined by the RTC clock frequency.

RTC security protection

High configurability to isolate secured, unsecured, privileged, unprivileged firmwares

- The RTC can be globally protected against non-secure access, by setting the SEC bit in the RTC_SECCFGR register. It can be globally protected against unprivileged access, by setting the PRIV bit in the RTC_PRIVCFGR register. Reading the RTC calendar is always possible with non-secure and unprivileged access.
- Each feature can be individually protected against non-secure or unprivileged write access:
  - INITSEC =1 / INITPRIV = 1 protects all registers linked to RTC calendar registers and prescaler initialization
  - CALSEC = 1 / CALPRIV = 1 protects all registers linked to RTC calibration, reference clock automatic calibration, daylight saving feature.
  - ALRASEC = 1 / ALRAPRIV = 1 and ALRBSEC = 1 / ALRBPRIV = 1 protect respectively all registers linked to Alarm A and B.
  - WUTSEC = 1 / WUTPRIV = 1 protects all registers linked to the Wakeup Timer.
  - TSSEC = 1 / TSPRIV = 1 protects all registers linked to TimeStamp.

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The RTC supports the TrustZone protection against any non-secure access, and also a protection against any unprivileged access. The protection can be set for the complete RTC by setting the SEC bit in the RTC secure configuration register, and the PRIV bit in the RTC privilege configuration register. It is also possible to individually configure each RTC feature to be secure or non secure, privileged or unprivileged: This allows, for instance, the allocation of Alarm A to a secur/privileged firmware and Alarm B to another non-secure/privileged firmware.
The features that can be configured as secure or privileged are: Alarm A, Alarm B, the auto-reload wakeup timer and the Timestamps. In addition, the calendar and prescalers initialization can be protected with a dedicated bit, as well as the calibration features. When the total RTC or a specific feature is protected by setting the associated bit in the RTC_SECCFGR and RTC_PRIVCFGR registers, the RTC calendar registers remain accessible in read mode secure or

non-secure, privileged or unprivileged access.

RTC security protection

- After a backup domain power-on reset, all RTC registers can be read or written with secure and non-secure access, except for the RTC secure mode control register (RTC_SECCFGR) which can be written with secure access only. The RTC protection configuration is not affected by a system reset.
- Accessing a secure-protected bit in a register is denied. A notification is generated in TZIC only when the register is globally protected.
- As soon as at least one function is configured to be secured, the RTC reset and clock control is also secured in the RCC.

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After a backup domain power-on reset, all RTC registers can be read or written with secure and non-secure access, except for the RTC secure mode control register which can be written with secure access only. The RTC protection configuration is not affected by a system reset.
Accessing a secure-protected register with non-secure access is done in SILENT mode when only a few bits are protected in the register: the protected bits access is denied without notification. When the register is globally protected, a notification is generated in the TrustZone illegal access controller.
As soon as at least one function is configured to be secured, the RTC reset and clock control is also secured in the RCC.

RTC register write protection

Safe RTC initialization

- The RTC registers are write-protected to avoid possible parasitic write accesses
  - Disable Backup Domain (DBP) bit must be set in the Power Controller control register 1 (PWR_CR1) to enable RTC write access
  - A Key must be written in RTC Write Protection register (RTC_WPR) register
- Specific software sequence to enter RTC initialization mode
  - Used for calendar registers and prescaler initialization

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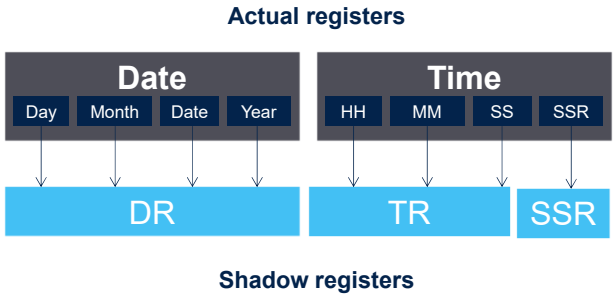
The RTC registers are write-protected to avoid any possible parasitic write accesses.
First, the Disable Backup Domain Protection bit must be set in the Power Controller control register in order to enable RTC write accesses.
Then, a specific sequence must be written in the RTC write protection register.
Initialization mode must be entered in order to change the clock prescaler values or the calendar value.

RTC calendar

Active in all low-power modes, VBAT and reset

- Initialization done through shadow registers: Time and Date registers



- Reading the calendar:
  - BYPSHAD = 0: Read shadow registers
    - Delay up to 2 RTCCLK cycles to update shadow registers when exiting Stop/Standby modes.
    - DR update is frozen after reading TR, and unfrozen when DR is read.
    - TR and DR update is frozen after reading SSR, and unfrozen when DR is read.
  - BYPSHAD = 1: Bypass shadow registers
    - Calendar read directly accesses the calendar counters
    - Software must read all calendar registers twice and compare the results to ensure that the data are coherent and correct.

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The RTC calendar keeps running in all low-power modes, in VBAT mode, and during reset when it is clocked by the LSE. Initialization of the Time and Date registers is performed through their shadow registers, which are in the APB clock domain. The Sub-second register cannot be initialized.
The content of the calendar Sub-second, Time, and Date registers can be read in two different modes.
When the Bypass Shadow Registers control bit is cleared, the shadow registers are read.
The advantage of this mode is that it guarantees that all three registers are consistent: when the Time register is read, the Date register is frozen until it is read. When the Sub-second register is read, the Time and Date registers are frozen until the Date register is read.
The disadvantage of this mode is that when exiting Stop, Standby mode, the software must wait for a synchronization delay to ensure that the shadow registers are updated with the last calendar register values. This synchronization delay

can be up to two RTC clock periods.
When the Bypass Shadow Registers control bit is set, the actual calendar registers are read directly.
The advantage of this mode is that there is no need to wait for the synchronization delay.
The disadvantage is that the read values can be false or not consistent due to synchronization issues, so they must be read twice and compared with previous read values to ensure they are correct and coherent.

RTC calendar features

- “Daylight savings” is managed by automatic addition or subtraction of 1 hour
- Calendar synchronization up to 1 s by adding/subtracting an offset with the sub-second resolution => Allows synchronization with remote clock
- Reference clock detection: A precise second-source clock (RTC_REFIN at 50 or 60 Hz mains) can be used to enhance the long-term precision of the calendar:
  - The reference clock is automatically detected and used to update the calendar
  - The LSE clock is automatically used to update the calendar whenever the reference clock becomes unavailable

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This slide presents the main calendar features.
Daylight savings can be managed by software, with automatic 1 hour addition or subtraction.
It is possible to synchronize the RTC clock to a remote clock by adding or subtracting an offset to the Sub-second register on the fly, with ck_apre clock resolution. This feature is commonly used in RF applications.
A reference clock, mains at 50 or 60 Hz, can be used to enhance long-term calendar precision. The reference clock RTC_REFIN is automatically detected and used to update the calendar when it is present. When the reference clock is not available, the LSE clock is automatically used to update the calendar. This feature is not available in Standby and VBAT modes.

RTC timestamp

- Calendar values
  - RTC_SSR register for the subseconds
  - RTC_TR register for the time
  - RTC_DR register for the date

  are saved in timestamp registers on each external I/O RTC_TS event.
- Internal timestamp detection when a switch to VBAT occurs.
- Timestamp detection on any Tamper event from TAMP peripheral

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A timestamp function is available. The calendar values, RTC_SSR sub-seconds register, RTC_TR time register, and RTC_DR date register are saved in timestamp registers when an I/O RTC_TS event occurs. A timestamp event can also occur when a switch to VBAT occurs. In addition, it is possible to timestamp the RTC counters when an internal or external tamper event occurs. Please refer to the TAMP peripheral training.

Smooth digital calibration

Crystal inaccuracy compensation

- Consists in masking/adding N (configurable) 32 kHz clock pulses, fairly well distributed in a configurable window
- Calibration value can be changed on the fly
- A 1 Hz output (RTC clocked by LSE) is provided to measure the crystal frequency and the calibration result

Calibration window with LSE	Accuracy	Total range
8 s	± 1.91 ppm	[0 ± 480 ppm]
16 s	± 0.95 ppm	[0 ± 480 ppm]
32 s	± 0.48 ppm	[0 ± 480 ppm]

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Digital calibration is used to compensate crystal inaccuracy and accuracy variations with temperature and aging. This calibration is not suitable for the internal oscillators as the digital calibration total range is too small to compensate internal oscillators inaccuracy.
Digital calibration consists in masking or adding a programmable number of RTC clock cycles, fairly well-distributed in a configurable window. The calibration value can be changed on the fly, depending on detected temperature changes, for instance. When the LSE at 32.678 kHz is used as RTC clock, a 1 Hz calibration output signal is provided to measure the crystal frequency before and after the calibration value is applied.
The accuracy shown here is the resolution of the digital calibration. The calibration window size is configurable, between 8, 16, and 32 seconds. For a 32 s calibration window, the accuracy is plus or minus 0.48 ppm. The total correction range is from -480 to 480 ppm. The accuracy resolution scales with the calibration window size. Final accuracy in the application will depend on the crystal parameter precision, temperature detection precision, how often the software calibration procedure is launched, etc.
In order to reach the precision of the calibration window, the measurement window must be a multiple of the calibration window.

RTC programmable alarm

2 flexible alarms based on calendar value

- The Alarm flags are set if the calendar sub-seconds, seconds, minutes, hours or date match the value programmed in the alarm registers
- 2 alarms, which exit the device from all low-power modes
- Alarm event can also be routed to the specific output pin RTC_OUT1 or RTC_OUT2, with configurable polarity.
- Calendar sub-second, seconds, minutes, hours or date fields can be independently selected (masked or not masked)
  - Masks allow configuration of periodic alarm interrupts

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The RTC embeds two flexible alarms, based on comparison with the calendar value. The alarm flags are set if the calendar sub-seconds, seconds, minutes, hours or date match the value programmed in the alarm registers.
Alarms events can wake up the device from all low-power modes.
Alarms event can also be routed to the specific output pins RTC_OUT1 or RTC_OUT2, with configurable polarity.
The calendar alarm sub-second, seconds, minutes, hours or date fields can be independently masked or not masked for the comparison. When masks are used, periodic alarms are generated.

Periodic auto-wakeup

Flexible periodic wakeup interrupt

- The periodic wakeup flag is generated by a 16-bit programmable binary auto-reload down counter (can be extended to 17 bits)
- Able to exit the device from Stop/Standby modes

Wakeup timer (WUT) clock	Wakeup period	Resolution
RTCCLK divided by 2, 4, 8, 16	From 122 µs to 32 s when RTCCLK = 32.768 kHz	Down to 61 µs
ck_spre	From 1 s to 36 hours when ck_spre = 1 Hz	1s

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In addition to the calendar and alarms, another 16-bit auto-reload counter can generate periodic events with wakeup from low-power modes capability. This counter cannot be read.
Depending on the software configuration, the wakeup timer clock can be the RTC clock divided by 2, 4, 8 or 16, or the output of the synchronous prescaler. With the divided RTC clock, the wakeup period can be from 122 microseconds to 32 seconds when the RTC clock frequency is 32.768 kHz. The resolution is down to 61 microseconds in this case. With the ck_spre clock, the wakeup period can be from 1 second to 36 hours when the ck_spre clock is at 1 Hz.

RTC pins functions

- RTC_OUT1 and RTC_OUT2 can output either :
  - The TAMPALRM signal resulting of all tamper flags (from TAMP peripheral) and the Alarm A, B or the WakeUp Timer (WUT) flag
  - The calibration signal (512 Hz or 1 Hz with LSE 32.768 kHz and the prescalers set with default value)
- TAMPALRM configurable polarity, open-drain/push pull mode, internal/external pull-up
- LSCO output provides the LSE

Function	All low-power modes except Standby	Standby	VBAT
RTC_TS	YES	YES	YES
RTC_REFIN	YES	NO	NO
RTC_OUT1	YES	YES	YES
RTC_OUT2	YES	YES	YES
LSCO	YES	YES	YES

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The RTC provides 2 outputs: RTC_OUT1 and RTC_OUT2. Depending on the selected configuration, these outputs can provide the Alarm A flag, or the Alarm B flag, or the Wakeup timer flag. It is possible to combine this output to the TAMP signal being the "OR" of all internal and external tamper detection flags of the TAMP peripheral. The resulting signal is named TAMPALRM. The polarity of TAMPALRM can be configured, as well as the output mode (push-pull or open-drain). It is also possible to apply an internal pull-up to this output.
In addition to the TAMPALRM signal, the RTC_OUT1 and RTC_OUT2 outputs can also provide a calibration output signal, extracted from the prescalers. When the prescalers are set with their default values and the RTC is clocked by the LSE at 32.768 kHz, the frequencies of this signal can be either 512 Hz or 1 Hz.

The RTC uses the RTC_TS pin for external timestamp, and

the RTC_REFIN pin for automatic calibration with reference clock. In addition, another signal named LSCO outputs the LSE clock.

All RTC pins are available in all low-power modes including VBAT, except for the RTC_REFIN input which is not available in Standby and VBAT modes.

Interrupts

Interrupt acronym	Interrupt event	Description
RTC_WKUP_ALARM	Alarm A	set when the calendar value matches the Alarm A value and Alarm A is non-secure
	Alarm B	Set when the calendar value matches the Alarm B value and Alarm B is non-secure
	Wake-up timer	Set when the wakeup auto-reload timer reaches 0 and wakeup timer is non-secure
RTC_TS	Timestamp	Set when a timestamp event occurs and timestamp is non-secure
RTC_WKUP_ALARM_S	Alarm A	set when the calendar value matches the Alarm A value and Alarm A is secure
	Alarm B	Set when the calendar value matches the Alarm B value and Alarm B is secure
	Wake-up timer	Set when the wakeup auto-reload timer reaches 0 and wakeup timer is secure
RTC_TS_S	Timestamp	Set when a timestamp event occurs and timestamp is secure

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Several RTC events can generate an interrupt. All interrupts can wake up the microprocessor from all low-power modes.
The Alarm A interrupt is set when the calendar value matches the Alarm A value.
Similarly, the Alarm B interrupt is set when the calendar value matches the Alarm B value.
The wakeup timer interrupt is set when the wakeup auto reload timer reaches zero.
The timestamp interrupt is set when a timestamp event occurs.
Each of these events generate a non-secure interrupt if the associated feature is configured as non-secure, or a secure interrupt if it is configured as secure.

Low-power and VBAT modes

Mode	Description
Run	Active.
Sleep	Active.
Stop	Active when clocked by LSE or LSI. RTC interrupts cause the device to exit Stop mode.
Standby	Active when clocked by LSE or LSI. RTC interrupts cause the device to exit Standby mode.
VBAT	Active when clocked by LSE

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The RTC peripheral is active in all low-power modes and in VBAT mode and, when triggered, the RTC interrupts cause the device to exit a low-power mode. In Stop and Standby modes, only the LSE or LSI clocks can be used to clock the RTC. Note that only the LSE clock is functional in VBAT modes.

Debug information

- RTC bit in Debug register : RTC counter stopped when core is halted

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A bit is available in the Debug interface, in order to stop the RTC counter when the core is halted for debugging.

Related peripherals

- Refer to these trainings on peripherals related to the RTC:
  - Reset and clock control (RCC)
  - Power control (PWR)
  - Tamper and backup registers (TAMP)
  - Debug support (DBG)

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This is a list of peripherals related to the real-time clock. Please refer to the peripheral trainings for more information if needed.

- Reset and clock control
- Power control
- Tamper and backup registers
- And Debug support

Thank you

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