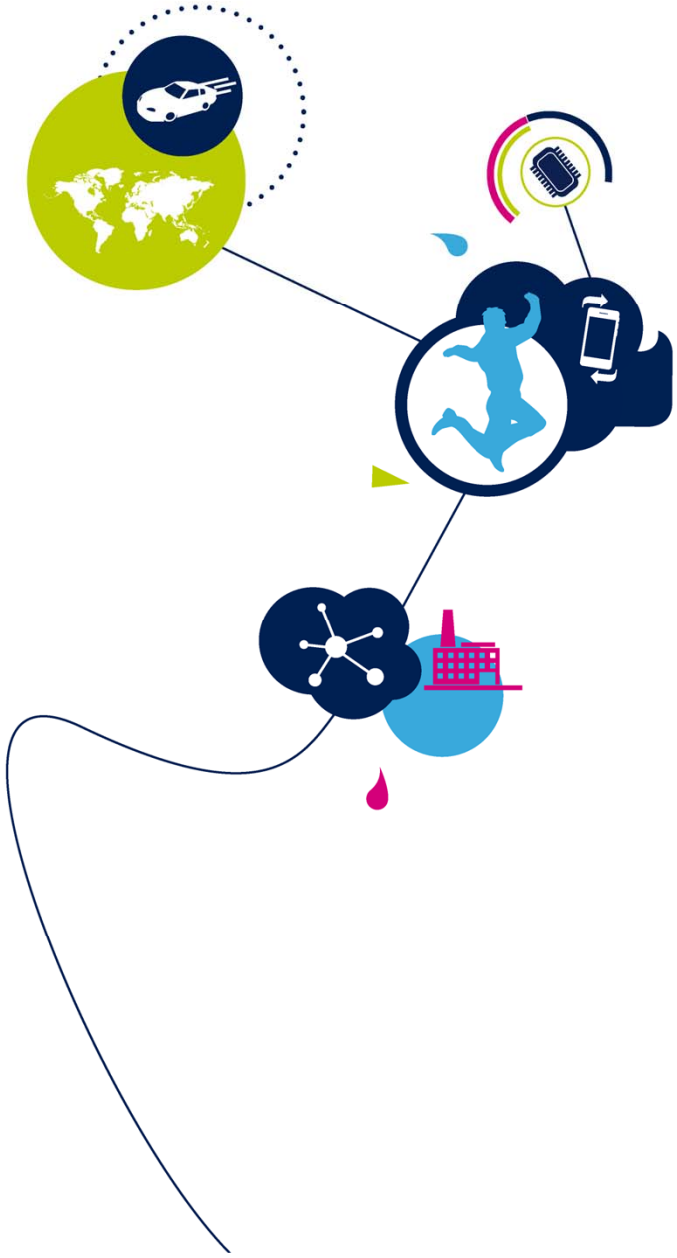
STM32L5 – RTC

Real-time clock

Revision 1.0



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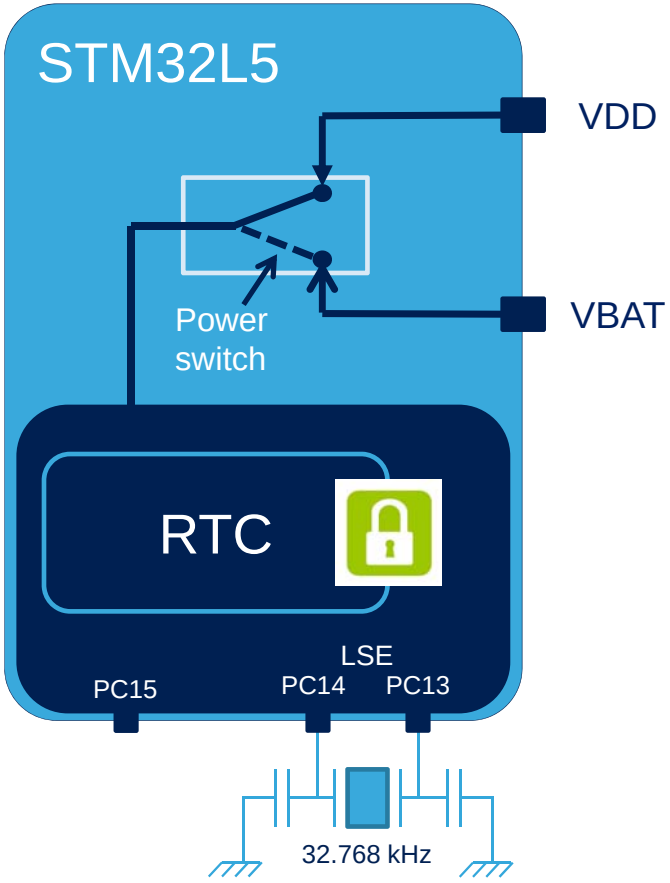
Overview



- The RTC provides an ultra-low-power hardware calendar with alarms, in all low-power modes
- It belongs to the Battery Backup Domain, so it is kept functional when the main supply is off and VBAT is present
- TrustZone®-aware peripheral with privilege access filtering

Application benefits

- Consumption drastically reduced for longer battery life
- Highly flexible security featuring individual isolation from non-secure or non-privilege processes
- Hardware BCD calendar to reduce software load

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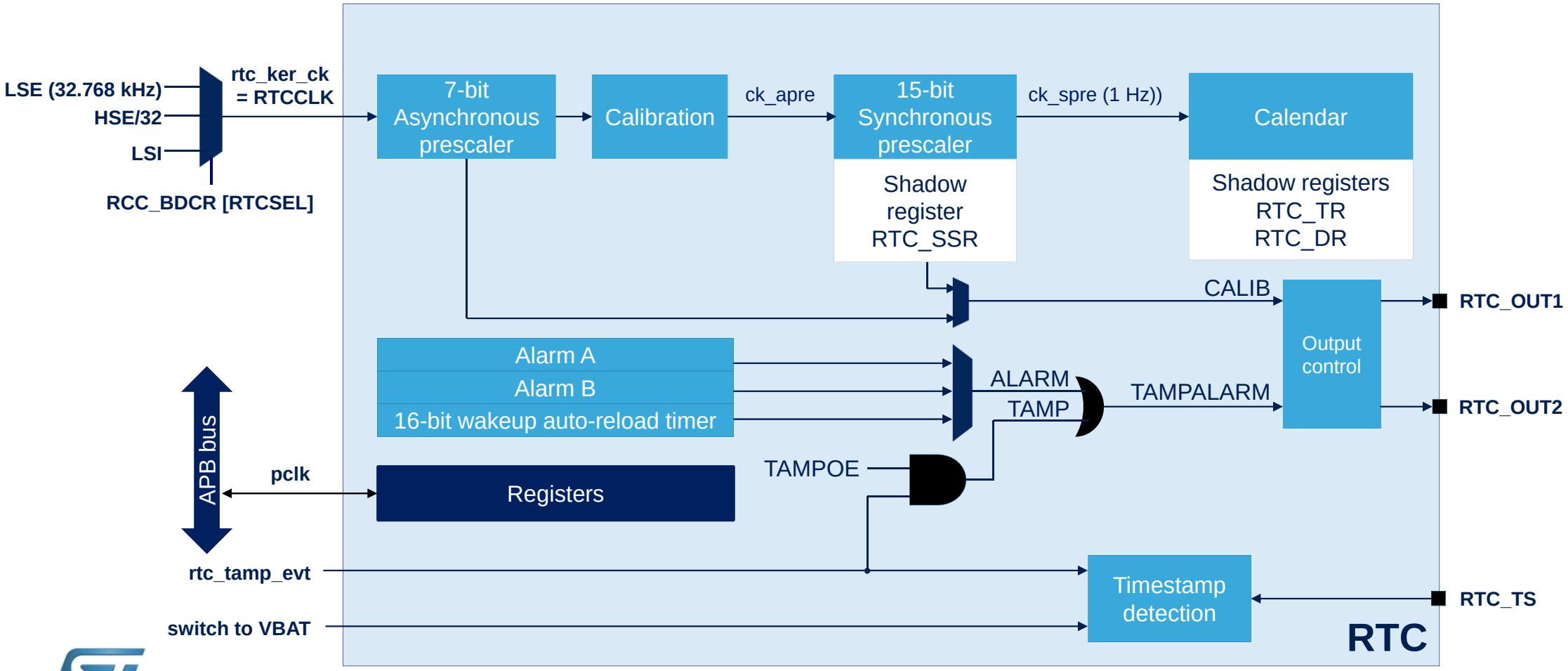
Key features

- Seconds, minutes, hours, week day, date, month, year in BCD format and sub-seconds in binary format
- “On the fly” programmable daylight savings compensation
- Two programmable alarms with wakeup interrupt function
- A periodic event with programmable resolution, triggering wakeup interrupt
- A reference clock source (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit to achieve 0.95 ppm accuracy
- Timestamp feature which can be used to save the calendar content with sub-second precision (one event)

Block diagram

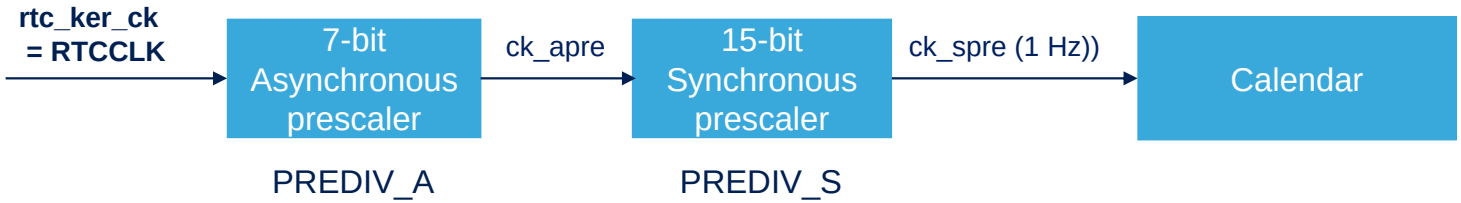


- RTC not affected by system reset when clocked by LSE

Consumption optimization modes

Longer battery life

- The RTC consumption can be minimized by reducing the sub-second resolution:
  - Sub-second register resolution is RTCCLK/(PREDIV_A+1)
    - $F_{CK\_APRE} = F_{RTCCLK} / (PREDIV\_A + 1)$
  - Optimal consumption is with default configuration: $F_{CK\_APRE} = 256$ Hz
    - With $F_{CK\_APRE} = 2048$ kHz => + 30nA
    - With $F_{CK\_APRE} = 8192$ kHz => + 130nA



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Consumption optimization modes

Longer battery life

- The RTC consumption is drastically reduced by setting Calibration Low-power Mode (LPCAL) mode
  - The LPCAL bit is ignored when (PREDIV_A+1) is not a power of 2
  - LPCAL=1 : the whole RTC is clocked only by ck_apre instead of RTCCLK or ck_apre
    - Calibration window is 2^{20} x PREDIV_A x RTCCLK pulses (LPCAL=1) instead of 2^{20} x RTCCLK pulses (LPCAL=0)

Security and Privilege protection

Hardware isolation between secure/non-secure privileged/unprivileged

- RTC can be globally protected against non-secure read and write accesses (DECPROT=0)
  - Calendar, security and privilege configuration registers are not read-protected
- Each RTC feature (Initialization, Calibration, Alarm A, Alarm B, Wakeup Timer, Timestamp) can be placed in its own hardware enforced security domain thanks to individual protection configuration against non-secure
- The same approach is used for privilege protection, either global or per RTC feature
  - A non-privilege access to a privilege-protected register is denied (write ignored, read as 0)
- 2 RTC interrupt vectors :
  - RTC (global non-secure feature interrupts)
  - RTC_S (global secure feature interrupts)

RTC register write protection

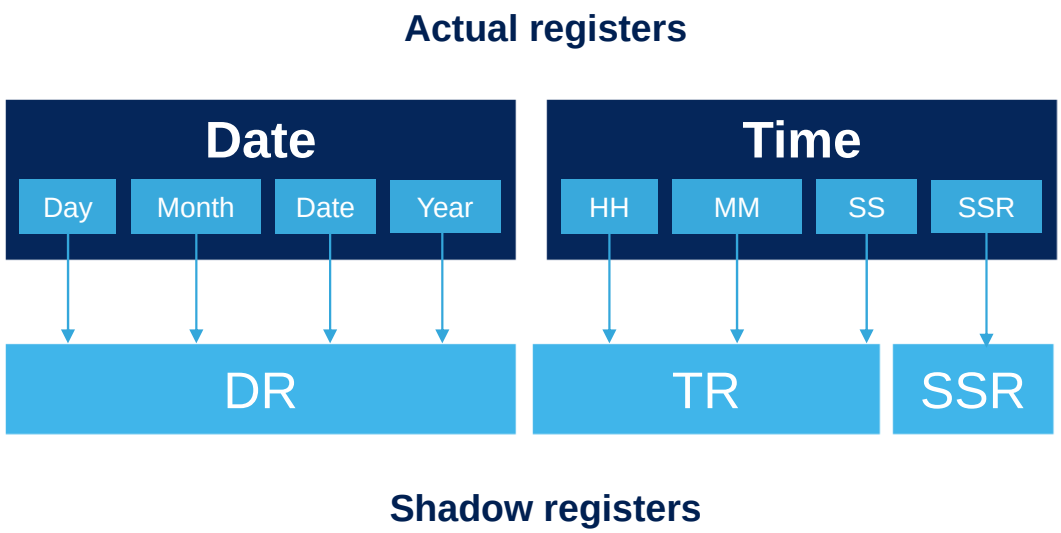
Safe RTC initialization

- The RTC registers are write-protected to avoid possible parasitic write accesses
  - Disable Backup domain write Protection(DBP) bit must be set in the Power Controller control register (PWR_CR1) to enable RTC write access
  - A Key must be written in the RTC write protection register (RTC_WPR) register
- Specific software sequence to enter RTC initialization mode
  - Used for calendar registers and prescaler initialization

RTC calendar

Active in all low-power modes, VBAT and reset

- Initialization done through shadow registers: Time and Date registers



- Reading the calendar:
  - BYPSHAD = 0: Read shadow registers
    - Delay up to 1 RTCCLK cycles to update shadow registers when exiting Stop/Standby/Shutdown modes.
    - Reading either RTC_SSR or RTC_TR locks the values in the higher-order calendar shadow registers until RTC_DR is read.
  - BYPSHAD = 1: Bypass shadow registers
    - Calendar read directly accesses the calendar counters
    - Software must read all calendar registers twice and compare the results to ensure that the data are coherent and correct.

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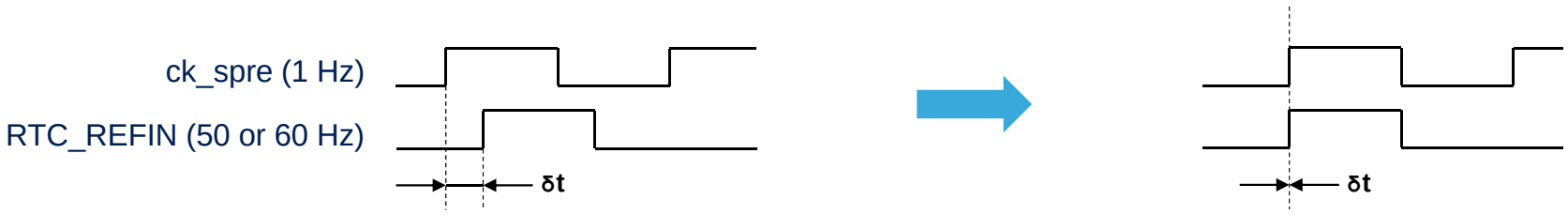
RTC calendar features

- “Daylight savings” is managed by automatic addition or subtraction of 1 hour
- Calendar synchronization up to 1 s by adding/subtracting an offset with the sub-second resolution => Allows synchronization with remote clock
- Reference clock detection: A more precise second-source clock (50 or 60 Hz mains) can be used to enhance the long-term precision of the calendar:
  - The reference clock is automatically detected and used to enhance the calendar precision
  - The LSE clock is automatically used to update the calendar whenever the reference clock becomes unavailable



RTC calendar features

- Timestamp
  - Calendar value is saved in timestamp registers on external I/O event
  - Internal timestamp detection when a switch to VBAT occurs
  - Optional timestamp in case of tamper detection

- If a new timestamp event is detected while the timestamp flag (TSF) is already set, the timestamp overflow flag (TSOVF) flag is set

Smooth digital calibration

Crystal inaccuracy compensation

- Consists in masking/adding N (configurable) 32.768 kHz clock pulses, fairly well distributed in a configurable window
  - When LPCAL=1: the calibration clock is ck_apre
- Calibration value can be changed on the fly
- A 1 Hz output is provided to measure the crystal frequency and the calibration result

Calibration window	Accuracy	Total range
8 s	± 1.907 ppm	[-487.1 ppm, +488.5 ppm]
16 s	± 0.954 ppm	[-487.1 ppm, +488.5 ppm]
32 s	± 0.477 ppm	[-487.1 ppm, +488.5 ppm]

RTC programmable alarm

2 flexible alarms based on calendar value

- The Alarm flags are set if the calendar sub-seconds, seconds, minutes, hours or date match the value programmed in the alarm registers
- 2 alarms, which exit the device from all low-power modes
- Alarm event can also be routed to the specific output pin RTC_OUT, with configurable polarity
- Calendar sub-second, seconds, minutes, hours or date fields can be independently selected (masked or not masked)
  - Masks allow configuration of periodic alarm interrupts

Periodic auto-wakeup

Flexible periodic wakeup interrupt

- The periodic wakeup flag is generated by a 16-bit programmable binary auto-reload down counter (can be extended to 17 bits)
- Able to exit the device from Stop/Standby/Shutdown modes

Wakeup timer (WUT) clock	Wakeup period	Resolution
RTCCLK divided by 2, 4, 8, 16	From 122 µs to 32 s when RTCCLK = 32.768 kHz	Down to 61 µs
ck_spre	From 1 s to 36 hours when ck_spre = 1 Hz	1s

Secure and non-secure interrupts

Interrupt event	Description
Alarm A	Set when the calendar value matches the Alarm A value
Alarm B	Set when the calendar value matches the Alarm B value
Wake-up timer	Set when the wakeup auto-reload timer reaches 0
Timestamp	Set when a timestamp event occurs

Low-power modes

Mode	Description
Run	Active
Sleep	Active • RTC interrupts cause the device to exit Sleep mode
Low-power run	Active
Low-power sleep	Active • RTC interrupts cause the device to exit Low-power sleep mode
Stop 0 / Stop 1/ Stop 2	Active when clocked by LSE or LSI • RTC interrupts cause the device to exit Stop 0/Stop 1/Stop 2 mode
Standby	Active when clocked by LSE or LSI • RTC interrupts cause the device to exit Standby mode
Shutdown	Active when clocked by LSE • RTC interrupts cause the device to exit Shutdown mode

Debug information

- DBG_RTC_STOP bit: RTC counter stopped when core is halted

Related peripherals

- Refer to these peripheral trainings linked to the RTC
  - TrustZone (TRZ)
  - Tamper and backup registers (TAMP)
  - Reset and clock control (RCC)
  - Power control (PWR)
  - Extended interrupt controller (EXTI)