



Hello, and welcome to this presentation of the STM32H5  
Extended Interrupts and Events Controller.  
We will be presenting the features of the EXTI controller.

## EXTI

EXTI line	Line source	Line type
0-15	GPIO	Configurable
16	PVD/AVD output	Direct
17	RTC non-secure	Direct
18	RTC secure	Direct
....		
40	SPI1 wakeup	Direct
41	SPI2 wakeup	Direct
....		
57	LPTIM6	Direct

- All events can wake up the system from Stop mode
  - Selectable active trigger edge for configurable events
- Direct lines from peripherals with wakeup capability
  - Upon wakeup event the system clock is enabled
  - When the system clock is present, the peripheral generates an interrupt if enabled
  - The interrupt wakes-up the device, and is directly connected to NVIC
- Individual secure and privilege configuration for each event



life.augmented

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The extended interrupts and event controller (EXTI) manages the individual CPU and system wakeup through configurable event inputs.

It provides wakeup requests to the power control and generates an interrupt request to the CPU NVIC and events to the CPU event input.

The table provides an example of the events supported by the STM32H5, that can wake up the system from Stop mode.

The STM32H5 EXTI controller supports direct peripheral events, that are generated by peripherals with wakeup capability.

Peripherals with wakeup capability request the system clock to be enabled, when system clock is present the

peripheral generates an interrupt. This interrupt wakes-up the device and is directly connected to NVIC.

Application will resume execution if the NVIC line is enabled and has enough priority to wakeup the CPU.

The EXTI is a TrustZone aware peripheral. The access to control and configuration bits of secure input events can be made secured and or privileged. When a non-secure master attempts to access a secure resource, the EXTI illegal access is reported to the Global TrustZone controller, GTZC.

# Thank you

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Thank you for attending this presentation on EXTI.  
You can also refer to the following presentations for more information if needed:

- Arm Cortex-M33 core
- Nested Vectored Interrupt Controller (NVIC).