Hello, and welcome to this presentation of the STM32MP1 Series System Configuration Controller.

Overview

- The STM32MP13 Series microprocessors feature a set of configuration registers. The main purposes of the system configuration controller are the following:
  - Select the Ethernet PHY interface type and speed (MII, RMII, RGMII)
  - Read the BOOT pin status
  - Manage the automatic I/O slew rate compensation
  - Select the analog switch supply voltage according to VDD and VDDA supply
  - Enable or disable high speed I/O drive capability at low voltages
  - Enable or disable 20mA I/O drive capability for 1MHz I^2C FM+ mode
  - Select if GP timer break input linked to PVD
  - Force an erase of SRAM3

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The STM32MP13 Series microprocessors feature a set of configuration registers which control various system-level features, including:

Select the Ethernet PHY interface type and speed (MII, RMII, RGMII)

Read the BOOT pin status

Manage the automatic I/O slew rate compensation

Select the analog switch supply voltage according to the VDD and VDDA supply

Enable or disable high speed I/O drive capability at low voltages

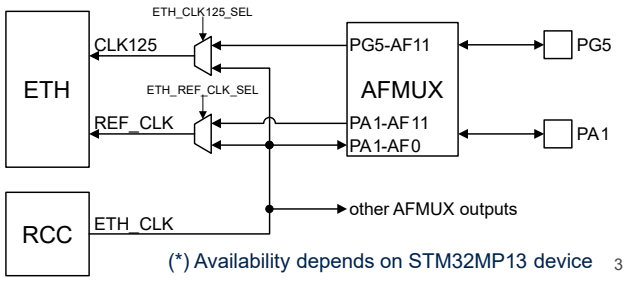
Enable or disable 20 milliamp I/O drive capability for I^2C “fast mode plus”

Select if the general-purpose timer break input is linked to PVD

Force an erase of SRAM3 memory

Ethernet PHY

- Control of PHY type
  - RGMII*, MII and RMII are supported
    - Must be selected while ETH is in reset and before enabling any ETH clock
- Control of Ethernet Reference clock
  - Depending on external Ethernet PHY, ETH_CLK1 pin can have various uses.
    - RGMII*: 125MHz clock can be supplied externally from the PHY via PG5*, or internally from the RCC
    - RMII: ETH_CLK at 50MHz can be output on PA1 as well as supplying REF_CLK
    - ALL modes: ETH_CLK can be used as 25MHz PHY reference clock (PA1, PB5 or PG8)
    - Must be selected while ETH is in reset and before enabling any ETH clock



(*) Availability depends on STM32MP13 device

The system configuration controller allows static selection of an external Ethernet physical interface. Reduced gigabit media-independent physical interface (RGMII) is supported, with the possibility of supplying the 125MHz ethernet clock from the external PHY. 10 or 100Mbit/s MII and RMII physical interfaces are also supported. The ETH_CLK output from the RCC can be used to supply the external physical interface reference clock (usually 25 MHz) thus saving a crystal.

Boot pins

- BOOT pins are used to control the source of the boot software
  - BOOT[2:0] are sampled by BOOTROM code during initialization
    - Available in a SYSCFG register which could be also read by the application if required
  - Possible BOOT settings include
    - SD-Card interface on SDMMC1 with or without external level translator
    - eMMC 4 or 8 bits on SDMMC2
    - Serial NOR-Flash on QUADSPI
    - Serial NAND-Flash on QUADSPI
    - Parallel NAND-Flash 8 or 16 bits on FMC
    - Serial (USART2/3/6 and UART4/5/7/8)
    - USB High-Speed device (OTG) thru embedded PHY
  - Default interface pin (for SDMMC, QUADSPI) and interface instance (for SDMMC) can be overridden by OTP fuse settings
  - BOOT pin choices can be overridden by OTP fuse while keeping rescue mode thru Serial/USB with a single push-button or strap (e.g. after sales services)

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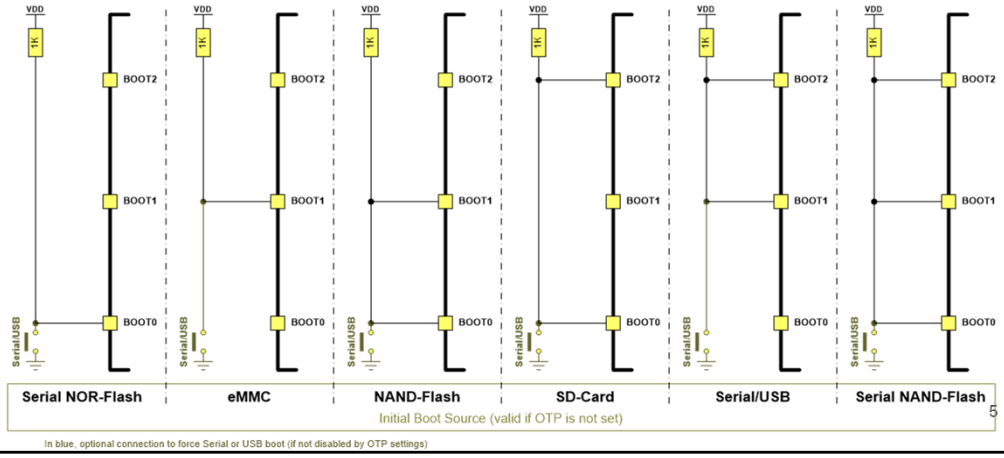
The Boot pins indicate which interface should be used to load the boot software.
The values on the BOOT pins are latched during the boot phase and read by the BOOTROM firmware. It is up to the user to set the BOOT pins to the appropriate state at power-up and before releasing the reset. This also applies to standby mode.
After the BOOTROM firmware has finished loading the boot software, the BOOT pins can be used as general purpose I/Os.

Boot pins

- Smart handling of the BOOT pins enables flexible boot scenario, e.g.:
  - Initial Boot from SD-Card which then program eMMC/NOR/NAND Flash memories
  - Rescue boot from Serial/USB port
  - Pre-Programmed Flash memory
  - Boot from USB to program Flash
  - Debug



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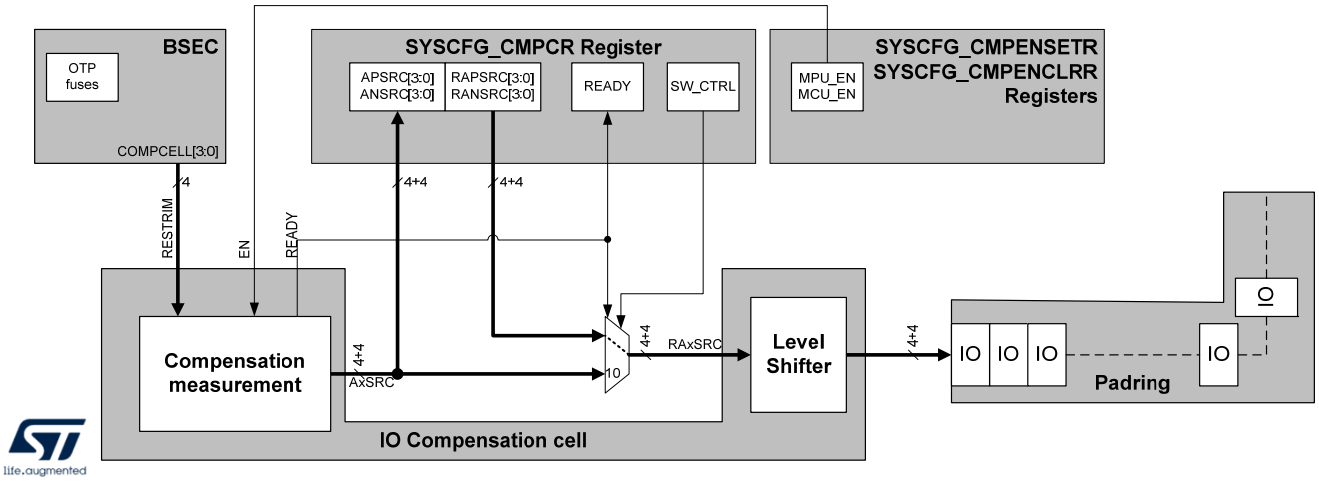
Multiple boot options can be supported, allowing flexible boot scenarios. For example, an initial boot program can be loaded from the SD-Card, which can load a main program into external flash memory. Subsequent boot will then be directly from external flash. It is also possible to switch to USB or serial port in case the start-up sequence does not work. Refer to the application note AN5031 (Getting started with STM32MP1 Series hardware development) and the Reference Manual for details on the BOOT pins.

IO compensation

- Automatic compensation of I/O voltage and temperature variation
  - Not used by default. Should be used for VDD I/O frequencies above 50MHz
  - IC process variation is compensated during production by setting OTP fuses



In order to have the best electrical characteristics whatever the conditions, the I/O compensation automatically tunes the characteristics of the I/Os when the voltage or the temperature changes. Compensation is required only for I/O frequencies above 50 MHz. There are three I/O partitions with a separate supply voltage for each one, VDD, VDD_SD1 and VDD_SD2. Each partition has dedicated compensation.

Control Timer Break

Safety

- Safety features in Control Timer Break registers
  - PVD lock to connect PVD interrupt to TIM1/8/15/16/17 Break input and to lock PVD enable and threshold
  - Puts timers in a safe state in the event of a PVD alarm

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The Control Timer Break Register connects the Programmable Voltage Detector alarm output to the general-purpose control timers' break input and locks the PVD enable and threshold. The register can only be written once after a system reset.

High Speed, Low Voltage I/Os

- High speed, low voltage (HSLV) output buffer control
  - When the I/O supply voltage is below 2.5V, a set of registers enables high speed, low voltage mode on certain interfaces:
    - SPI1-5, SDMMC1-2, ETH1-2, QUADSPI, TRACE, LTDC
  - Separate registers are provided for each interface. HSLV mode is only activated when the corresponding interface is selected in the I/O AFMUX.
  - [**Warning**] Enabling HSLV mode when the I/O supply is >2.7V could damage the device.
  - To avoid accidental setting of the HSLV enable, a special value must be written in the register to enable HSLV mode.
  - A fuse is provided in the OTP which must be programmed before HSLV mode can be enabled, for all I/Os in the VDD supply domain. SDMMC I/Os in the VDDSD1 and VDDSD2 domain are not protected by OTP fuse.

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When the I/O supply voltage is below 2.5V, a set of system configuration registers enables high speed, low voltage mode on the SPI, SDMMC, Ethernet, QUADSPI, TRACE and LTDC interfaces.
Separate registers are provided for each interface. HSLV mode is only activated when the corresponding interface is selected in the I/O AFMUX.
Warning: Using HSLV mode when the I/O supply is >2.7V could damage the device.
To avoid accidental setting of the HSLV enable, a special value must be written in the register to enable HSLV mode. In addition, a fuse is provided in the OTP which must be programmed before HSLV mode can be enabled, for any I/Os in the VDD supply domain. SDMMC I/Os in the VDDSD1 and VDDSD2 domain are not protected by OTP fuse.

SYSCFG other features

- Enable 20 mA I/O current drive for I²C Fast-mode Plus.
  - This mode is only enabled on pads where I2C is selected in the AFMUX.
- Control of analog switch supply voltage on ADC inputs
  - Improves ADC performance when VDDA is below 2.7V

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The system configuration controller manages the following additional features:

- Enable 20 mA I/O current drive for I²C Fast-mode Plus. This mode is only enabled on pads where I2C is selected in the alternate function multiplexer.
- Control analog switch supply voltage when the IO supply (VDD) and/or analog supply (VDDA) are below 2.7V. The analog switch supply is boosted to ensure optimal performance at low voltages.

STM32MP13x Lines Bootloader

- The Bootloader supports the following Serial/USB interfaces
  - USART3 (PB12/PB10)
  - USART6 (PC7/PC6)
  - UART4 (PD8/PD6)
  - UART5 (PB5/PB13)
  - UART7 (PF6/PF7)
  - UART8 (PE0/PE1)
  - OTG HS in Device mode (USB_DP2/USB_DM2)
    - Need HSE quartz or external clock (default 24 MHz)

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The on-chip bootloader allows the user to program the Flash memory or set OTP fuses through a serial communication peripheral. The supported protocols are USART and USB.

USB is recommended for a large amount of external memory.

Note

The USB Boot works with specific values of the external quartz oscillator on HSE with 24 MHz as default; 25 and 26 MHz are also possible with dedicated OTP fuse settings;

OTP setting for HSE auto-detection allows 8, 10, 12, 14, 16, 20, 24, 28, 32, 36, 40, and 48 MHz for USB Boot.

The USART/UART uses the internal HSI oscillator with automatic baud rate detection.

There is no restriction on the HSE frequency between 8 and

48MHz if the USB port is not used during the boot phase (could be used by the application with any HSE frequency).

Related peripherals

- Refer to these training modules linked to this peripheral:
  - Reset and clock control (RCC)
  - Power controller (PWR)
  - Timers (TIM)
  - Ethernet (ETH)
  - Inter-Integrated Circuit (I²C)

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In addition to this training, you can refer to the Reset and Clock Control, Power Controller, Timers, Ethernet and I²C trainings.

Thank you

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