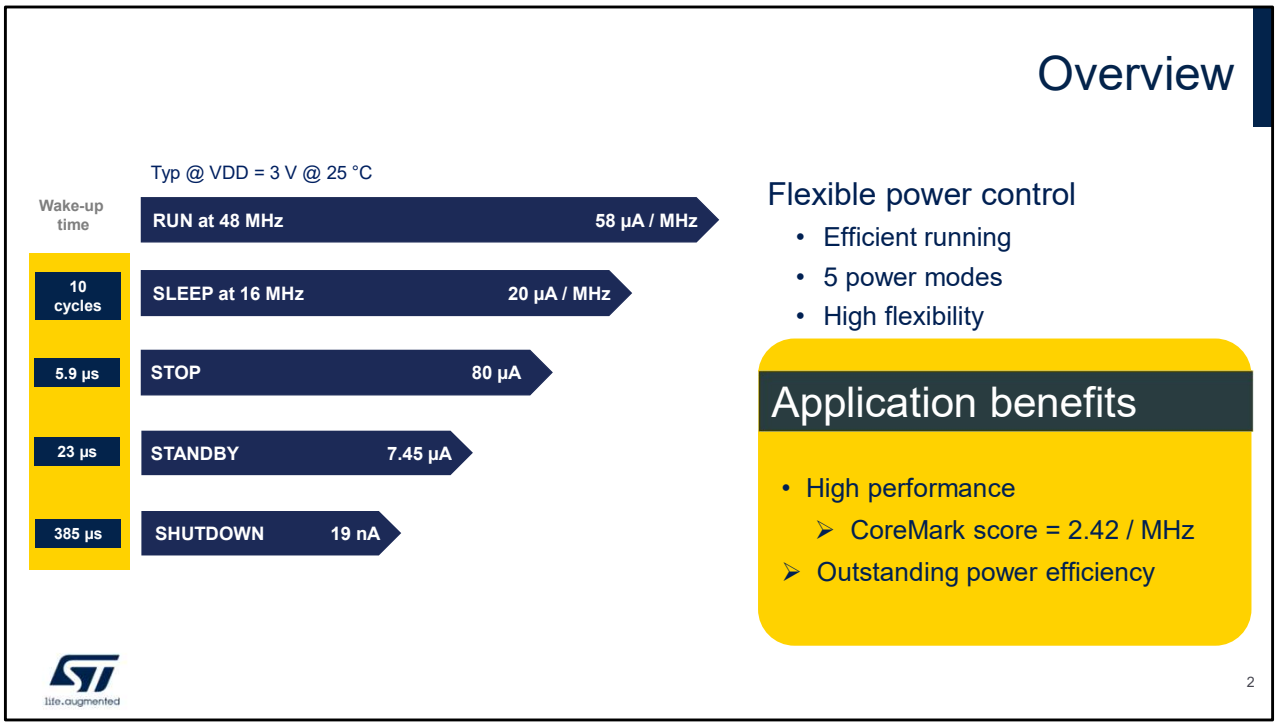

Hello, and welcome to this presentation of the STM32C0 power controller.
The STM32C0's power management functions and all low power modes are also covered in this presentation.




STM32C0 devices feature a power control unit, designed to increase flexibility in power mode management and further reduce the overall application consumption.
Run mode can support a system clock running at up to 48 MHz, with only 58 µA/MHz.
STM32C0 devices support 5 main power modes: Run, Sleep, Stop, Standby and Shutdown modes.
The high flexibility in power management provides both high performance with a CoreMark score equal to 125 at 48 MHz, together with an outstanding power efficiency.

## Key features

- Four low-power modes with fast wakeup
  - Down to 19 nA with I/O wake-up
  - Down to 8 µA with IWDG
  - Wake-up from high number of peripherals
- Down to 58 µA / MHz in Run mode
- 4x16-bit backup registers retained in Standby
- Only one supply pair $V_{DD}$/ $V_{DDA}$

### Application benefits

- High flexibility to lower power consumption depending on active peripherals, required performance and needed wakeup sources
- Increase battery life

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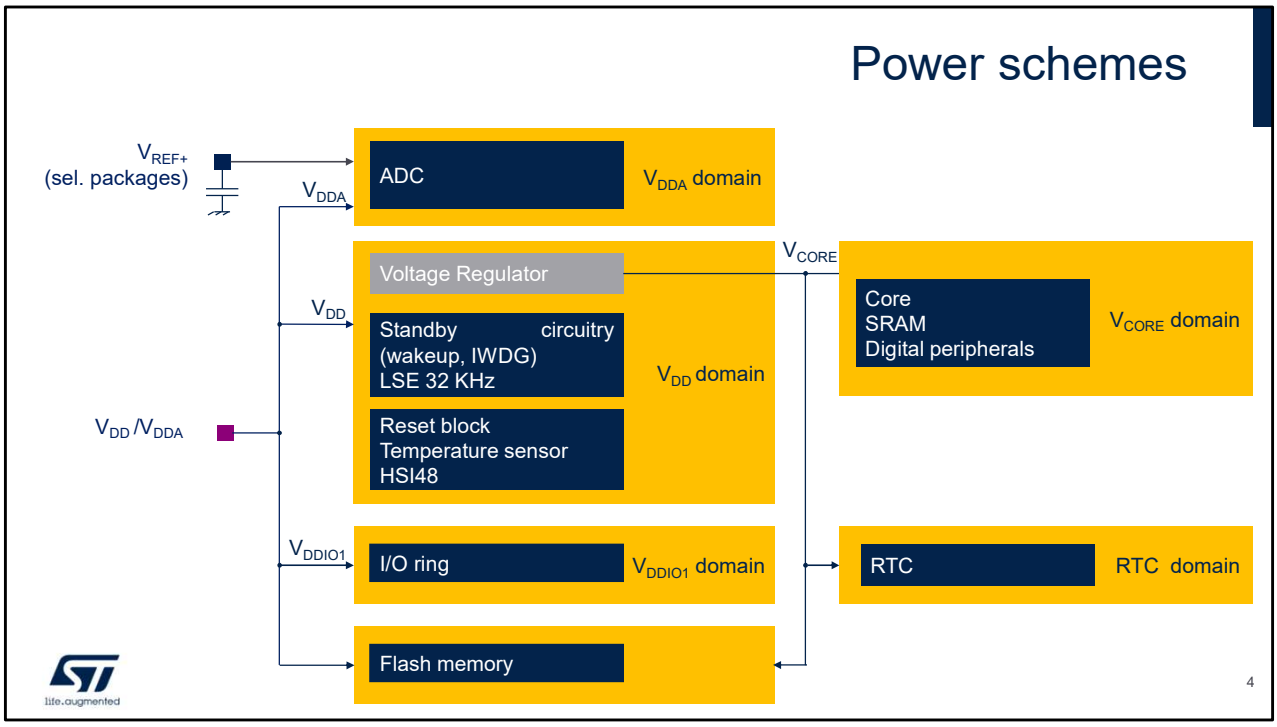
The STM32C0 has several key features related to power management:

- Several low-power modes, down to 19 nA while it is still possible to wake up the MCU with an event on an I/O.
- A large number of peripherals can wake-up from the various low-power modes.
- Dynamic consumption is down to 58 µA/MHz, executing from Flash memory.
- Thanks to the large number of power modes, STM32C0 devices offer high flexibility to minimize the power consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.




STM32C0 main power supply is VDD/VDDA pin, supplying all I/Os, the reset block, temperature sensor and all internal clock sources.
In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog.
VDD supplies voltage regulators which provide the VCORE supply.
VCORE supplies most of the digital peripherals, SRAM and Flash controller.
VDDA voltage is the same as the VDD one and supplies the analog peripheral.
The VREF+ pin provides the reference voltage to the analog-to-digital converter and can be used as an external buffer reference for the application.

Note that the flash is connected to two power rails: VDD for the memory and Vcore for the controller.

## Power schemes

**Optimized power and performance thanks to independent power supplies**

- The STM32C0 devices require a 2.0 V to 3.6 V operating supply voltage ($V_{DD}$)
  - Several different power supplies are provided to specific peripherals:
    - $V_{DD}$ from 2.0 to 3.6 V
    - $V_{DDA}$ from 2.0 to 3.6 V
      - $V_{DDA}$ always shared (bonded) with $V_{DD}$
    - $V_{REF+}$ = from 2.0V to $V_{DDA}$
  - $V_{REF+}$ : reference voltage for ADC
    - It can be provided by an external reference voltage or shared with $V_{DD}$
    - $V_{REF+}$ pin is not available on low pin count packages
      - On those packages, this pin is double-bonded with $V_{DD}$

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The main power supply VDD ensures full feature operation in all power modes from 2 up to 3.6 V.
Device functionality is guaranteed down to 2 V, the minimum voltage after which a power-down reset is generated.
The analog power supply VDDA is always connected to VDD.
VREF+ is the analog peripheral input reference voltage.
VREF+ must be between 2 V and VDDA.
It can be grounded when the analog peripherals using VREF+ are not active.
On packages without VREF+ pin, VREF+ is internally connected with VDD.

## Power supply supervisor

**Safe and ultra-low-power reset management**

- POR & PDR are always enabled in all modes except Shutdown mode
- Brown-out reset is enabled in all modes except Shutdown mode when BOR_EN option bit is set
  - Ensure reset as soon as microcontroller drops below selected threshold, regardless of the $V_{DD}$ slope
  - Four thresholds selected by option byte BORR_LEV[1:0] and BORF_LEV[1:0], independently configurable for rising and falling edge

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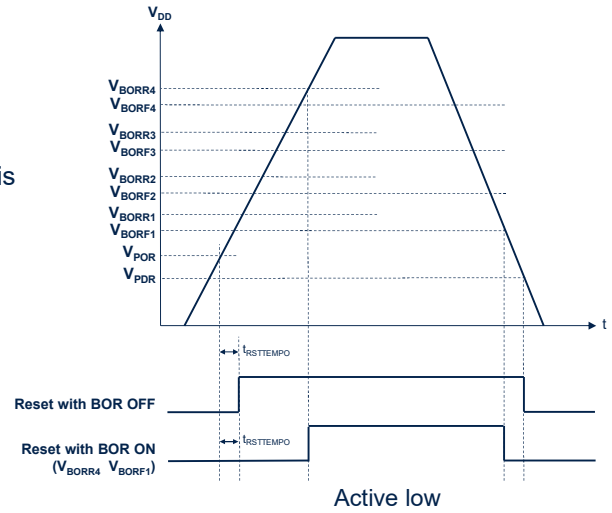
The power supply supervisor guarantees a safe and ultra-low power reset management.
STM32C0 devices embed a Power-On Reset (POR) and a Power-Down Reset (PDR) which are always enabled in all power modes except Shutdown mode.
The Brown-Out reset (or BOR) ensures reset generation as soon as the microcontroller power supply drops below the selected threshold, regardless of the VDD slope.
Four thresholds from 2.0 to 2.95 V can be selected by option byte programmed in Flash memory independently for rising and falling edge. It can also be disabled to save power consumption.

# Brown Out Reset

- The BOR maintain the device under reset until reaching the desired supply voltage
- Four BOR thresholds, separately configurable for rising and falling edge are available, offering flexibility in the hysteresis to the user

| | Rising Threshold (V) | Falling Threshold (V) |
|---|---|---|
| POR/PDR | 1.94 | 1.92 |
| BOR1 | 2.1 | 2.0 |
| BOR2 | 2.31 | 2.21 |
| BOR3 | 2.62 | 2.52 |
| BOR4 | 2.91 | 2.81 |




Active low



The Power resets (BOR and POR) resets all registers.
When exiting Standby mode, all registers powered by the Main regulator are reset.
When exiting Shutdown mode, a Power reset is generated.
When the BOR is enabled, four BOR levels can be selected through option bytes with independent configuration for rising and falling thresholds.

## Run mode

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except Flash interface clock
  - SRAM clock is always ON in Run mode

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In Run mode, the CPU is clocked and program can be executed from FLASH or SRAM Memory.
The power consumption in Run mode can be reduced through selecting a system clock with lower frequency, scaling down the system clock frequency, disabling unused peripherals and/or stopping their clocks (peripheral clock gating).
Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes.
By default, all peripheral's clocks are OFF, except the Flash interface clock.
The SRAM clocks are always ON in Run mode.
By default, the device is in Run mode after system or power reset.

## Run mode

- Current consumption in Run mode depends on several parameters:
  - Executed binary code (program itself + compiler impact)
  - Program location in memory (depending on address of executed code)
  - Device software configuration (depending on application)
  - I/O pin loading and switching rate
  - Temperature
  - Execution from Flash memory or SRAM
    - When execution from Flash memory: accelerator configuration (Cache, Prefetch)
      - Energy efficiency better with Prefetch + Cache ON
    - When execution from SRAM:
      - Energy efficiency better versus Flash

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The current consumption in Run mode depends on several parameters: first the executed binary code, which means the program itself plus the compiler impact.
Then it depends on the program location in the memory, the device software configuration, the I/O pin loading and switching rate, the temperature and the memory from which instructions are fetched: flash or SRAM.
When code is executed from Flash, the Energy efficiency is better when the Flash accelerator is enabled, because instruction cache and prefetch buffer are based on SRAM memory.

# Sleep modes

**All peripherals available and fastest wakeup time**

- Core is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing **WFI** (Wait For Interrupt) or **WFE** (Wait For Event)
- Two mechanisms to enter this mode:
  - **Sleep Now**: MCU enters Sleep mode as soon as WFI/WFE instruction are executed
  - **Sleep on Exit**: MCU enters Sleep mode as soon as it exits the lowest priority ISR
    - The stack is not popped before entering Sleep mode, it will not be pushed when the next interrupt occurs, saving running time
  - Controlled by Cortex-M0+ **SLEEPONEXIT bit in System Control Register**

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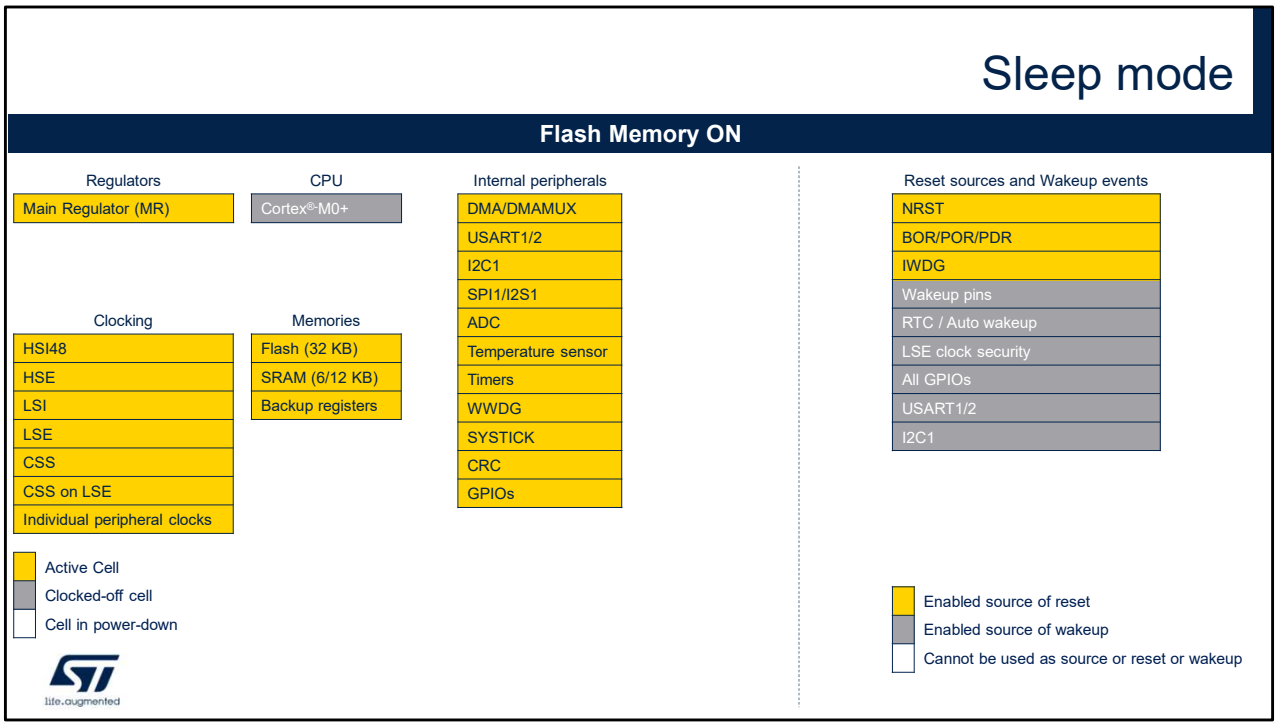
Sleep allows all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF.
This mode is entered by executing the assembler instruction Wait for Interrupt or Wait for Event.
Depending on the SLEEPONEXIT bit configuration in the CortexM0+ System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt service routine.
This last configuration allows to save time and consumption by saving the need to pop and push the stack when exiting the low power mode. However, all

computations must be done in Cortex®-M0+ handler mode, because the thread mode is no longer used.




In Sleep mode, the CPU clock is OFF.
The frequency of the system clock is up to 48 MHz.
By default, the SRAM clock is enabled.
It can be gated off during Sleep mode by software.
The Sleep mode consumption is 17 µA/MHz with the Flash memory ON.
Note that the flash memory can be powered-down in sleep mode, when the FDP_SLP bit is set to one prior to entering sleep mode.

## Stop modes

**Lowest power modes with full retention, 5.9 µs wakeup time at 12 MHz**

- SRAM and all peripheral registers retention
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup is HSI48/4
  - 2.5 µs wakeup time on RAM
  - 5.9 µs on FLASH, not powered during STOP

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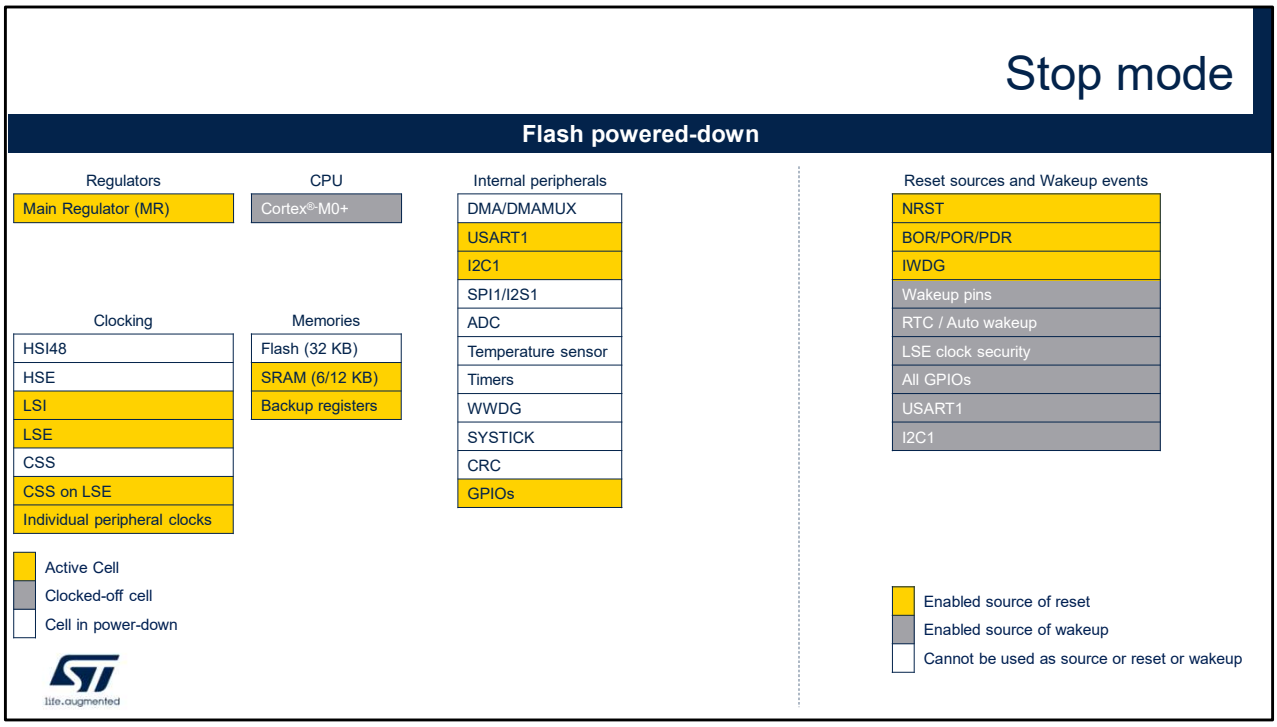
Stop mode is the lowest power modes with full retention and only a 2.5-µs wakeup time to Run mode at 12 MHz.
The contents of SRAM and all peripherals' registers are preserved in Stop modes.
All high-speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up is the internal high-speed oscillator at 12 MHz with only a 2.5-µs wakeup time from RAM or 5.9µs from FLASH, the divider configuration to SYSCLK is kept upon wake-up.




All clocks in the VCORE domain are stopped; the HSI48 and the HSE oscillators are disabled.
The RTC, clocked by the internal or external low-speed oscillator remains active.
The brown-out reset is always enabled. Most of the peripheral clocks are gated off.
Several peripherals can be functional in Stop mode: USART1/2, I2C1, independent watchdog.
The events from all I/Os can wake up from Stop mode, as well as the interrupt generated by the active peripherals.
The I2C1 and USART1 and 2 can switch the HSI48 ON during the Stop mode in order to recognize their wakeup condition and switch off the HSI48 after receiving the frame if it is not a wakeup frame.

In this case, the HSI48 clock is propagated only to the peripheral requesting it.
The Stop mode consumption typical at 3V is 80 µA when HSI is disabled, 605 µA when HSI48 is enabled.

## Standby mode

**Lowest power mode with BOR active, backup register retained and I/O control**

- No SRAM nor registers retention (voltage regulators in power down)
  - 4x 16-bit backup registers always retained
- Ultra Low Power BOR configurable: safe reset regardless of $V_{DD}$ slope
- Configurable pull-up or pull-down or none for each I/O
  - PWR_PUCRx / PWR_PDCRx registers (x = A,B,…D), applied when APC is set in PWR_CR3 register
    - Allows to control external component input state
- Five wakeup pins: the polarity of each wakeup pins is configurable
- Wakeup clock is HSI48/4 at 12 MHz

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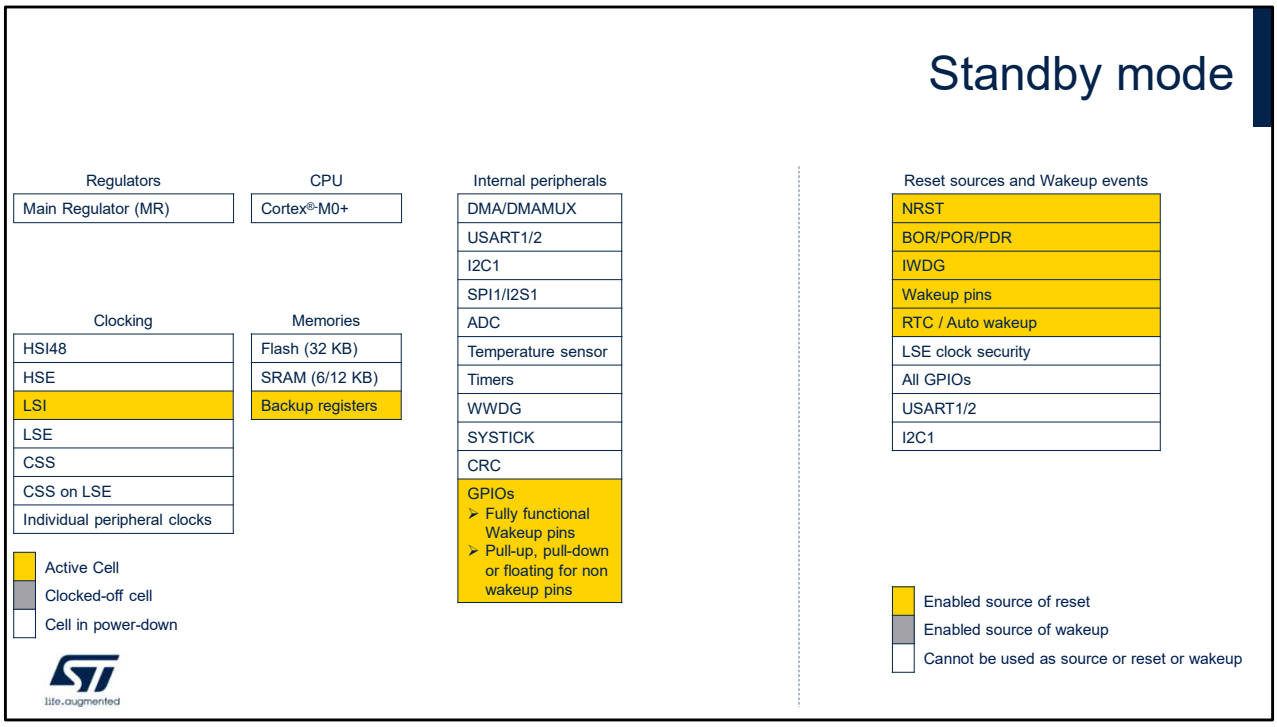
The Standby mode is the lowest power mode in which context information can be retained in four PWR Backup registers.
The voltage regulators are in Power down mode and the SRAM and the peripherals registers are lost.
The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.
Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit.
This allows to control the input state of external components even during Standby mode.
5 wakeup pins are available to wake up the device from Standby mode. The polarity of each of the 5 wakeup pins

is configurable.
The wakeup clock is HSI48 divided by 4, so a frequency of 12 MHz.

# Standby mode




In Standby mode, the voltage regulator is powered down. The RTC, clocked by the internal or external low-speed oscillator, may remain active.
The brown-out reset can be enabled. The independent watchdog can also be enabled in Standby mode.
Reset, brown-out or Power down reset, independent watchdog and any event on the 5 wakeup pins can exit the microcontroller from Standby mode.
The consumption in standby mode without the RTC is 7.45 microAmperes typical at 3 V.

## Shutdown mode

**Lowest power mode: 19 nA**

- Similar to Standby but
  - NO power monitoring: no BOR
    - The microcontroller state is not guaranteed if the power supply is lowered below 2V
  - NO LSI, no IWDG
  - BOR reset is generated when exiting Shutdown mode
    - All registers are reset.
    - Reset generated on the pad
- Wakeup sources: 5 wakeup pins
- Wakeup clock is HSI48/4 = 12 MHz

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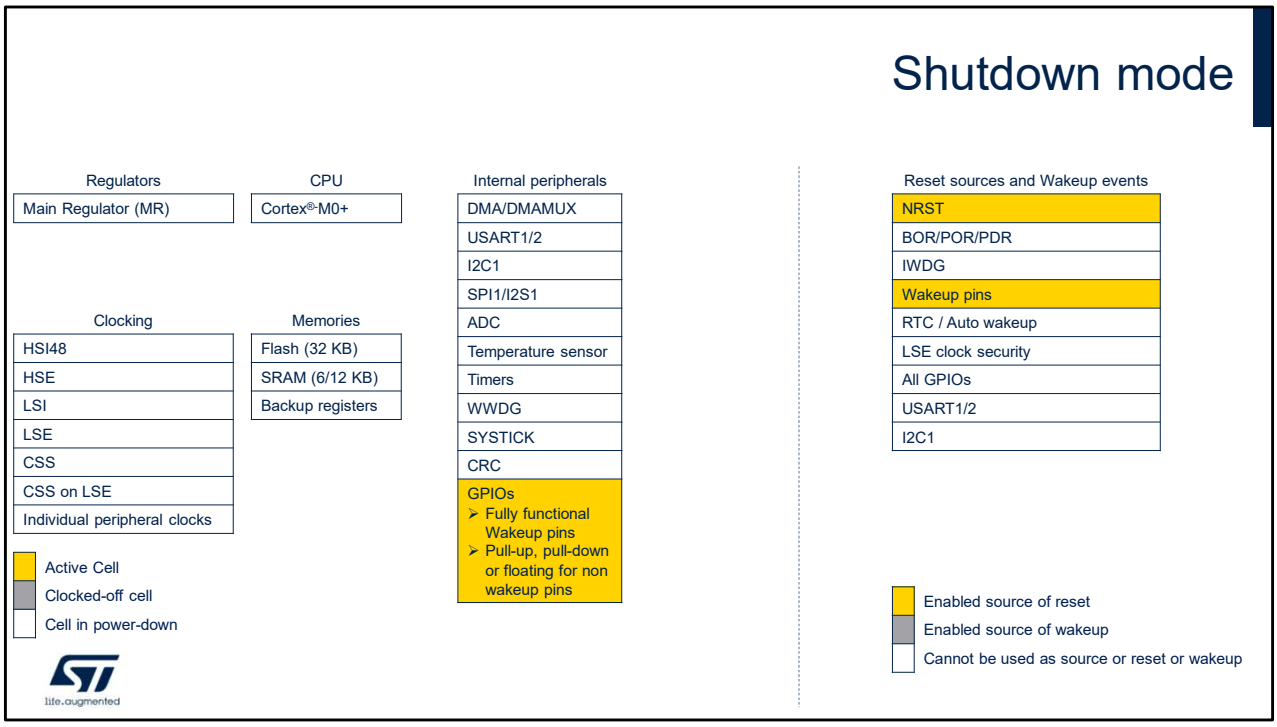
The shutdown mode is the lowest power mode, with only 19 nA at 3 V.
This mode is similar to Standby mode, but without any power monitoring: the brown-out reset is disabled.
Hence the microcontroller state is not guaranteed in case the power supply is lowered below 2V.
The LSI is not available, and consequently neither is the independent watchdog.
A brown-out reset is generated when the device exits Shutdown mode: all registers are reset, and a reset signal is generated on the pad.
The wakeup sources are the 5 wakeup pins.
When exiting Shutdown mode, the wakeup clock is HSI48/4, so 12 MHz.




In Shutdown mode, the voltage regulator is powered down. The brown-out reset is deactivated.
The wakeup events are the reset input and the 5 wakeup pins.

## Low-power modes summary

| Mode | Regulator | CPU | Flash | SRAM | Clocks | Peripherals | Wakeup time |
|---|---|---|---|---|---|---|---|
| **Run** | ON | **Yes** | **ON**(1) | **ON** | Any | All | N/A |
| **Sleep** | ON | No | **ON**(1) | **ON**(2) | Any | All<br>Any IT or event | 10 cycles |
| **Stop** | ON | No | OFF | **ON** | LSE/LSI (HSI48) | Reset pin, all I/Os<br>BOR, RTC, IWDG, USART1/2, I2C1 | 2.5 µs RAM<br>5.9 µs Flash memory |
| **Standby** | OFF | DOWN | OFF | DOWN | LSI | Reset pin, 5 WKUPx pins<br>BOR, IWDG | 23 µs |
| **Shutdown** | OFF | DOWN | OFF | DOWN | - | Reset pin, 5 WKUPx pins | 385 µs |

1. Can be put in power-down and clock can be gated off
2. SRAM can be gated off

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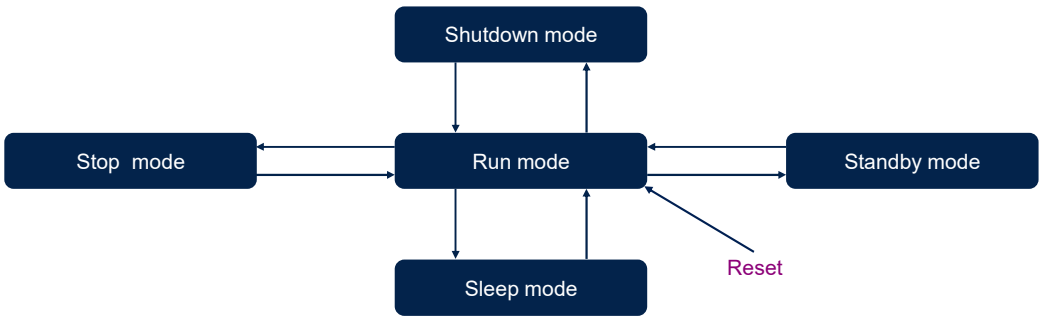
Here’s a summary of all the STM32C0 power modes.

## Low-power modes transitions

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The device can transition from Run mode to any of the low-power modes and from any low-power operating mode to Run mode.
Transiting from one low-power mode to another is not possible.

## Option bytes

- Three option bits can be configured in Flash options bytes to prohibit a given low-power mode:
  - nRST_SHDWN:
    - When cleared, a Reset is generated when entering Shutdown mode
  - nRST_STDBY:
    - When cleared, a Reset is generated when entering Standby mode
  - nRST_STOP:
    - When cleared, a Reset is generated when entering Stop modes

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3 bits are available in the Flash option bytes to prohibit a given low-power mode.
When cleared, an option bit configures reset generation when entering Shutdown mode.
Another bit configures reset generation when entering Standby mode and the last bit configures reset generation when entering Stop modes.

## Debug information

- Under Sleep mode, the DBG connection is not lost
- Two bits in DBGMCU_CR register allows to debug in Stop, Standby and Shutdown modes:
  - DBG_STANDBY:
    - When set, the digital part is not un-powered in Standby and Shutdown modes, and HCLK and FCLK remain ON, provided by internal RC
    - In addition, the MCU in under system reset during Standby/Shutdown
  - DBG_STOP:
    - When set, HCLK and FCLK remain ON in Stop modes, provided by internal oscillator
- When those bits are set, the connection with debugger is kept during the low-power mode
  - After wakeup, debug is still possible

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The microcontroller integrates special means to allow the user to debug software in low-power modes.
By default, Stop, Standby, and Shutdown low-power modes deactivate FCLK and HCLK, which prevents debug capability.
In Sleep mode however, the device keeps FCLK and HCLK always active.
To keep FCLK or HCLK clocks active and preserve debug capability in Stop, Standby, and Shutdown modes, the debugger host must set, before entering one of these low-power modes, the DBG_STOP bit (for Stop) or DBG_STANDBY bit (for Standby and Shutdown) of the DBG_CR register.
When the related bit is set, the regulator is kept on in

Standby and Shutdown modes, and the HCLK and FCLK clocks are provided by an internal RC oscillator.
This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup.
Remember to clear these bits when the microcontroller is not under debug, because the consumption is increased in low power modes.

## Related peripherals

- Refer to the following list of peripherals training presentations for more details of their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Interrupts (NVIC, EXTI)
  - Independent watchdog (IWDG)
  - Real-time clock (RTC)
  - Inter-integrated circuit (I2C) interface
  - Universal synchronous asynchronous receiver transmitter (USART)


To complement this presentation, you can refer to the following presentations:

- Reset and Clock Control
- Interrupt management
- Peripherals with wakeup from Stop capability.

## Differences vs. STM32G0

- The Power controller is simplified vs. the one implemented in the G0 family

| | STM32G0 | STM32C0 |
|---|---|---|
| Low Power modes | Stop1 and Stop0 | Stop |
| SRAM retention in standby mode | Full SRAM | 4x16 bit registers in PWR |
| PVD & BOR | Falling and Rising threshold independency | Falling and Rising threshold independency from 2.1V no PVD |
| Vbat mode | Yes | No |
| Sampling Mode for BOR & PDR (ULPEN) | Yes | No |

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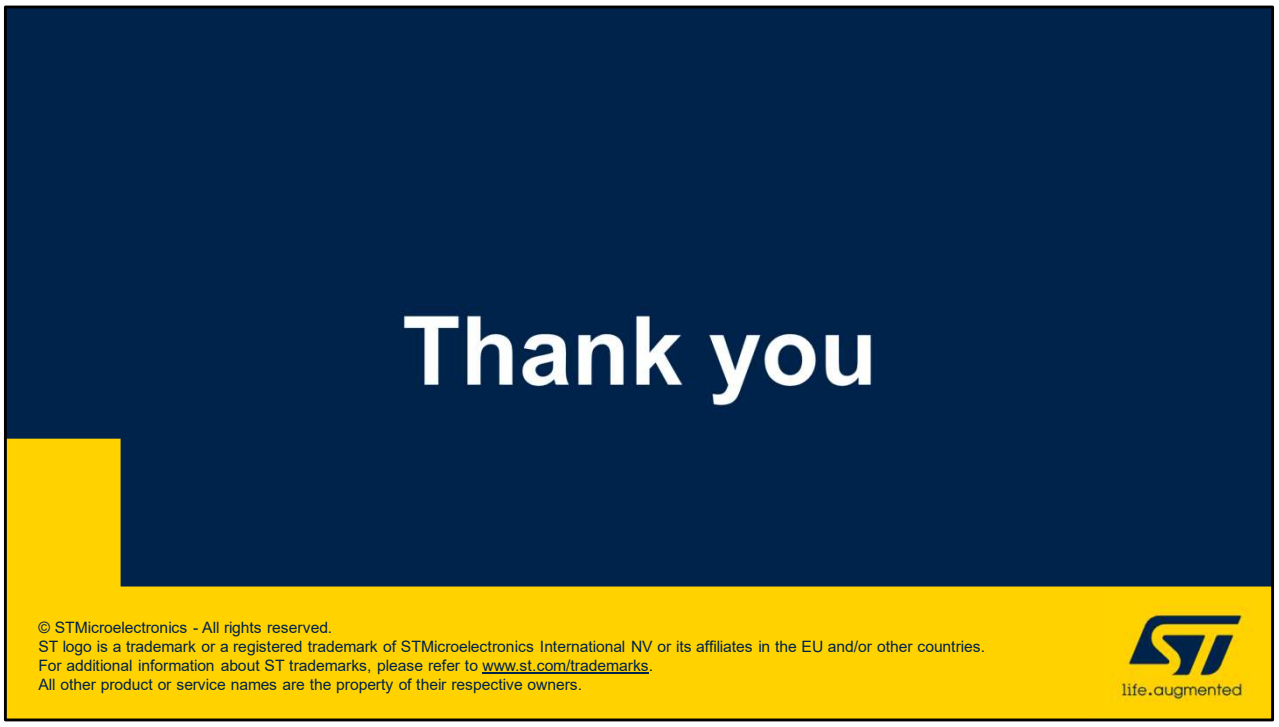
The table in this slide compares the features of STM32C0 and STM32G0 in terms of power control.
The STM32C0 supports a unique stop mode, while the STM32G0 supports two stop modes.
The STM32C0 ensures the retention of only the backup registers in standby mode, while the STM32G0 also ensures the retention of the SRAM.
VBAT mode is not supported by STM32C0.
Sampling mode for BOR and PDR is not supported by STM32C0.
In Stop 0/1 and Standby mode, POR and PDR can be periodically activated in STM32G0 to decrease power consumption.




Thank you for attending this presentation.