STM32MP1 – SERIES

Series presentation

Revision 2.1

Hello, and welcome to this introduction to the STM32MP1 series.
This short presentation describes the various lines available in the STM32MP1 series of high-performance MPUs with an Arm Cortex-A7 core.

STM32MP15x product lines

ACCELERATION / CONNECTIVITY / AUDIO / OTHER	Product line	f_CPU (MHz)	Cortex-A7 cores	f_MCU (MHz)	Cortex-M4 cores	f_GPU (MHz)	Cortex-A7 L1 cache (I/D) L2 cache	RAM (Kbytes)	HW Crypto	3D GPU	FDCAN	MIPI-DSI	T_J
ACCELERATION • Dual core* Arm® Cortex®-A7 processor • L1 and L2 caches • 3D Graphic Processing Unit* • Floating Point Unit + Arm® NEON™ • Arm® Cortex®-M4 209MHz coprocessor • MDMA + DMA • LPDDR2/LPDDR3 16/32**-bits 533MHz • DDR3/DDR3L 16/32**-bits 533MHz	STM32MP151A	650	1	-	1	-	32K+32K + 256K	640K + 64K retention + 4K backup	-	-	-	-	-40°C to 125°C
	STM32MP151C								●	-	-	-	
CONNECTIVITY • 2 x USB2.0 HS Host • USB2.0 OTG FS/HS • 3 x SDMMC/SDIO • USART, UART, SPI, I²C • 2 x (TT)FDCAN2.0* • HDMI-CEC • Gigabit Ethernet IEEE 1588*** • FMC (NAND Flash) • Camera I/F • Dual mode Quad-SPI • DSI 2Gbit/s*	STM32MP151D	800	1	-	1	-	32K+32K + 256K	640K + 64K retention + 4K backup	-	-	-	-	-20°C to 105°C
	STM32MP151F								●	-	-	-	
	STM32MP153A	650	2	209	1	-	2x (32K+32K) + 256K	640K + 64K retention + 4K backup	-	-	2	-	-40°C to 125°C
	STM32MP153C								●	-	2	-	
	STM32MP153D	800	2	209	1	-	2x (32K+32K) + 256K	640K + 64K retention + 4K backup	-	-	2	-	-20°C to 105°C
	STM32MP153F								●	-	2	-	
AUDIO • I²S + audio PLL • 4 x SAI + 8 x DFSDM + SPDIF-RX • 2 x 12-bit DAC	STM32MP157A	650	2	209	1	533	2x (32K+32K) + 256K	640K + 64K retention + 4K backup	-	●	2	●	-40°C to 125°C
	STM32MP157C								●	●	2	●	
OTHER • 16- and 32-bit timers • 2 x 16-bit ADC (7.2 MSPS)	STM32MP157D	800	2	209	1	533	2x (32K+32K) + 256K	640K + 64K retention + 4K backup	-	●	2	●	-20°C to 105°C
	STM32MP157F								●	●	2	●	

Arm® Cortex®-A7 – up to 800 MHz

Notes:
* not available in all product lines
** 16/32-bits for LFBGA448 and TFBGA361 packages, 16-bits only for LFBGA354 and TFBGA257 packages
*** 10/100M Ethernet only for LFBGA354 and TFBGA257 packages

Taking advantage of L1 and L2 caches, STM32MP15x microprocessors deliver the maximum theoretical performance of the Cortex-A7 core no matter whether the code is executed from the embedded RAM or an external memory: up to 2568 CoreMark at 800 MHz f_{CPU} for each core.
- The STM32MP151 line offers the performance of a single Cortex-A7 core (with floating point unit and NEON SIMD Engine) running up to 800 MHz, plus a Cortex-M4 with FPU which offer up to 703 Coremark at 209 MHz f_{MCU} for real time peripheral processing. The STM32MP151C integrates a crypto processor providing hardware acceleration for AES-128, -192 and -256, with support for GCM and CCM, Triple DES functions.
- The STM32MP153 line expands the family to double Cortex-A7 core, doubling the available Coremark to 5136 at 800 MHz f_{CPU} , plus additional interfaces such as two FDCAN, one having TT option. The STM32MP153C
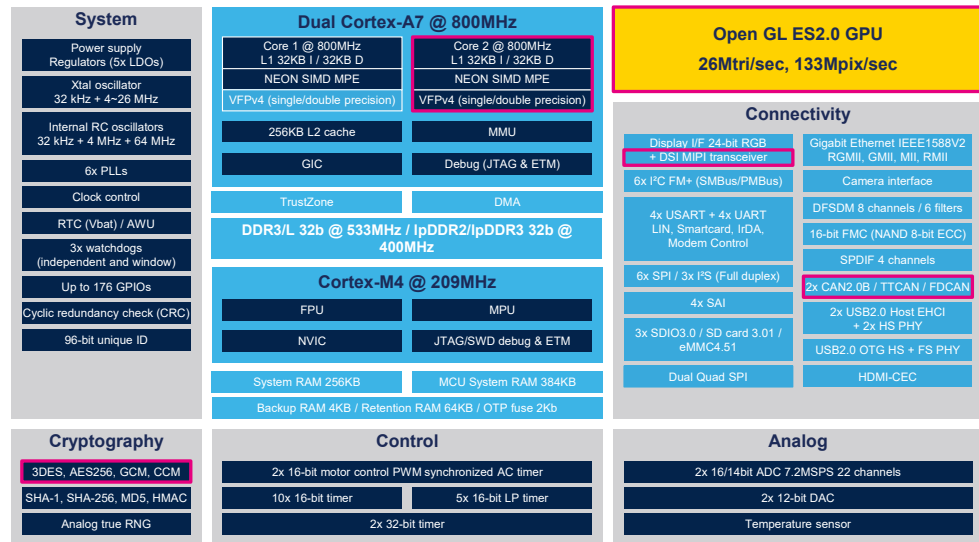
integrates a crypto processor.

- The STM32MP157 line offers in addition a 3D GPU for complex image composition (up to 26M triangles/sec or 133M pixels/sec at 533MHz f_{GPU}) and a MIPI-DSI interface (up to 1366x768 at 60fps). The STM32MP157C integrates a crypto processor.
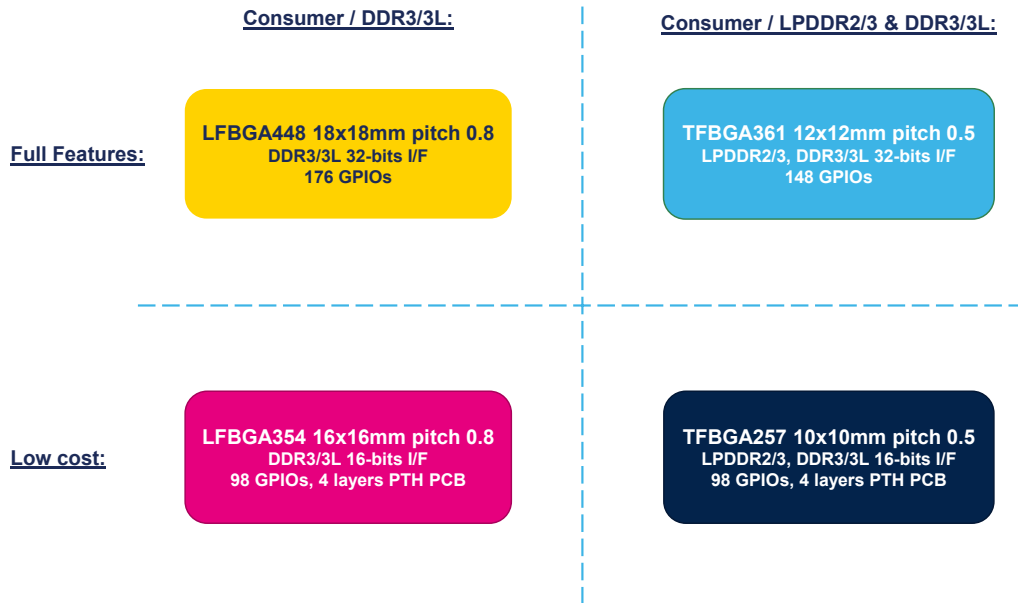
STM32MP157F block diagram

- Available packages
  - LFBGA448 18x18 pitch 0.8
  - LFBGA354 15x15 pitch 0.8
  - TFBGA361 12x12 pitch 0.5
  - TFBGA257 10x10 pitch 0.5

System
- Power supply Regulators (5x LDOs)
- Xtal oscillator 32 kHz + 4~26 MHz
- Internal RC oscillators 32 kHz + 4 MHz + 64 MHz
- 6x PLLs
- Clock control
- RTC (Vbat) / AWU
- 3x watchdogs (independent and window)
- Up to 176 GPIOs
- Cyclic redundancy check (CRC)
- 96-bit unique ID

Dual Cortex-A7 @ 800MHz
- Core 1 @ 800MHz L1 32KB I / 32KB D
- Core 2 @ 800MHz L1 32KB I / 32KB D
- NEON SIMD MPE
- NEON SIMD MPE
- VFPv4 (single/double precision)
- VFPv4 (single/double precision)
- 256KB L2 cache
- MMU
- GIC
- Debug (JTAG & ETM)
- TrustZone
- DMA
- DDR3/L 32b @ 533MHz / lpDDR2/lpDDR3 32b @ 400MHz

Cortex-M4 @ 209MHz
- FPU
- MPU
- NVIC
- JTAG/SWD debug & ETM
- System RAM 256KB
- MCU System RAM 384KB
- Backup RAM 4KB / Retention RAM 64KB / OTP fuse 2Kb

Open GL ES2.0 GPU
26Mtri/sec, 133Mpix/sec

Connectivity
- Display I/F 24-bit RGB + DSI MIPI transceiver
- Gigabit Ethernet IEEE1588V2 RGMII, GMII, MII, RMII
- 6x I²C FM+ (SMBus/PMBus)
- Camera interface
- DFSDM 8 channels / 6 filters
- 4x USART + 4x UART LIN, Smartcard, IrDA, Modem Control
- 16-bit FMC (NAND 8-bit ECC)
- SPDIF 4 channels
- 6x SPI / 3x I²S (Full duplex)
- 2x CAN2.0B / TTCAN / FDCAN
- 4x SAI
- 2x USB2.0 Host EHCI + 2x HS PHY
- 3x SDIO3.0 / SD card 3.01 / eMMC4.51
- USB2.0 OTG HS + FS PHY
- Dual Quad SPI
- HDMI-CEC

Cryptography
- 3DES, AES256, GCM, CCM
- SHA-1, SHA-256, MD5, HMAC
- Analog true RNG

Control
- 2x 16-bit motor control PWM synchronized AC timer
- 10x 16-bit timer
- 5x 16-bit LP timer
- 2x 32-bit timer

Analog
- 2x 16/14bit ADC 7.2MSPS 22 channels
- 2x 12-bit DAC
- Temperature sensor

Not Available on all product lines

This block diagram summarizes the key features and the available packages for STM32MP157F devices.
The STM32MP157F line integrates the dual Cortex-A7 core (with floating point unit and NEON SIMD Engine) running up to 800MHz, with 708 Kbytes of SRAM in total and up to 35 communication interfaces in addition to a 3D Graphic Processing Unit and an LCD-TFT controller with a parallel or DSI interface for advanced graphics processing.
Boxed red blocks are not available on all product lines.

STM32MP15x Packages

Consumer / DDR3/3L:

Consumer / LPDDR2/3 & DDR3/3L:

Full Features:

> **LFBGA448 18x18mm pitch 0.8**
> DDR3/3L 32-bits I/F
> 176 GPIOs

> **TFBGA361 12x12mm pitch 0.5**
> LPDDR2/3, DDR3/3L 32-bits I/F
> 148 GPIOs

Low cost:

> **LFBGA354 16x16mm pitch 0.8**
> DDR3/3L 16-bits I/F
> 98 GPIOs, 4 layers PTH PCB

> **TFBGA257 10x10mm pitch 0.5**
> LPDDR2/3, DDR3/3L 16-bits I/F
> 98 GPIOs, 4 layers PTH PCB

The four packages are optimized for a wide range of usage. Full feature packages provide maximum available GPIO count, and exist in pitch 0.8mm for robust and low-cost PCB as well as pitch 0.5mm for smaller PCB footprint.
Low cost packages are optimized for low cost Plated-Through Hole (PTH) PCB routing and are available in two different ball pitch for low-cost PCB or small PCB footprint.

ACCELERATION
- Arm® Cortex®-A7 processor
- L1 and L2 caches
- Floating Point Unit + Arm® NEON™
- MDMA + DMA
- LPDDR2/LPDDR3 16-bits 533MHz
- DDR3/DDR3L 16-bits 533MHz

CONNECTIVITY
- 2 x USB2.0 HS Host
- USB2.0 OTG HS
- 2 x SDMMC/SDIO
- USART, UART, SPI, I²C
- 2 x (TT)FDCAN2.0*
- Dual Gigabit Ethernet IEEE 1588*
- FMC (NAND Flash)
- Camera I/F*
- Dual mode Quad-SPI

AUDIO
- I²S + audio PLL
- 2 x SAI + 4 x DFSDM + SPDIF-RX

OTHER
- 16- and 32-bit timers
- 2 x 12-bit ADC (7.2 MSPS) *

Arm® Cortex®-A7 – up to 800 MHz

Product line	fCPU (MHz)**	Cortex®-A7 cores	Cortex®-A7 L1 cache (I/D) L2 cache	RAM (Kbytes)	HW Crypto	Display/Camera	FDCAN	Eth	ADC	T_J
STM32MP131A					-	-	-	x1	x1	−40°C to 125°C
STM32MP131C					●					
STM32MP131D					-	-	-	x1	x1	−20°C to 105°C
STM32MP131F					●					
STM32MP133A					-	-	2	x2	x2	−40°C to 125°C
STM32MP133C	650/1000	1	32K+32K + 128K	160K + 8K backup	●					
STM32MP133D					-	-	2	x2	x2	−20°C to 105°C
STM32MP133F					●					
STM32MP135A					-	●	2	x2	x2	−40°C to 125°C
STM32MP135C					●					
STM32MP135D					-	●	2	x2	x2	−40°C to 125°C
STM32MP135F					●					

Notes: * not available in all product lines
** frequency in Run mode / Overdrive mode

Taking advantage of L1 and L2 caches, STM32MP13x microprocessors deliver the maximum theoretical performance of the Cortex-A7 core no matter whether the code is executed from the embedded RAM or an external memory: up to 2952 CoreMark at 1 GigaHertz fCPU.
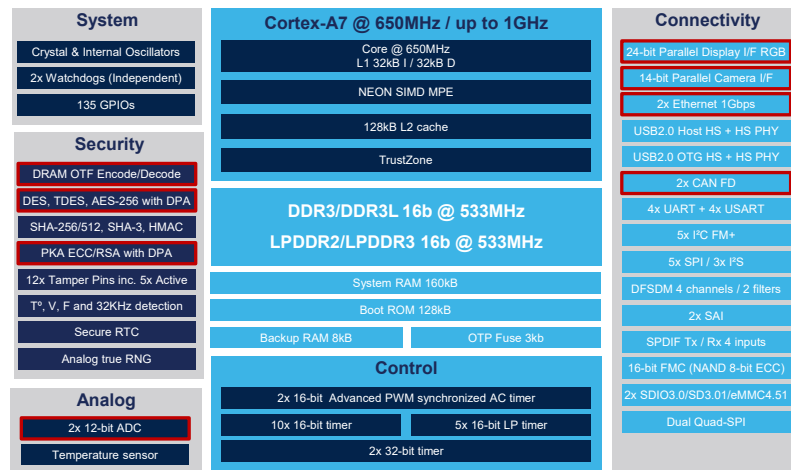STM32Mp13x offers 3 lines: STM32MP131, STM32MP133, STM32MP135
All lines have a single Cortex-A7 core up to 650MHz in normal in mode and up to 1Ghz in overdrive mode, 2x32KB L1 cache and 128KB L2 cache, 160KB SRAM and 8KB backup SRAM.
Each line offers a crypto version including secure boot with authentication, cryptography (Secure AES and CRYP), DRAM on the fly encoding/decoding, Public key accelerator. and a non crypto version.
The table shows the feature differences for each line.

STM32MP135F block diagram

- Available packages
  - LFBGA289 14x14 pitch 0.8
  - TFBGA320 11x11 pitch 0.5
  - TFBGA289 9x9 pitch 0.5

System
- Crystal & Internal Oscillators
- 2x Watchdogs (Independent)
- 135 GPIOs

Security
- DRAM OTF Encode/Decode
- DES, TDES, AES-256 with DPA
- SHA-256/512, SHA-3, HMAC
- PKA ECC/RSA with DPA
- 12x Tamper Pins inc. 5x Active
- T°, V, F and 32KHz detection
- Secure RTC
- Analog true RNG

Analog
- 2x 12-bit ADC
- Temperature sensor

Cortex-A7 @ 650MHz / up to 1GHz
- Core @ 650MHz / L1 32kB I / 32kB D
- NEON SIMD MPE
- 128kB L2 cache
- TrustZone

DDR3/DDR3L 16b @ 533MHz
LPDDR2/LPDDR3 16b @ 533MHz
- System RAM 160kB
- Boot ROM 128kB
- Backup RAM 8kB
- OTP Fuse 3kb

Control
- 2x 16-bit Advanced PWM synchronized AC timer
- 10x 16-bit timer
- 5x 16-bit LP timer
- 2x 32-bit timer

Connectivity
- 24-bit Parallel Display I/F RGB
- 14-bit Parallel Camera I/F
- 2x Ethernet 1Gbps
- USB2.0 Host HS + HS PHY
- USB2.0 OTG HS + HS PHY
- 2x CAN FD
- 4x UART + 4x USART
- 5x I²C FM+
- 5x SPI / 3x I²S
- DFSDM 4 channels / 2 filters
- 2x SAI
- SPDIF Tx / Rx 4 inputs
- 16-bit FMC (NAND 8-bit ECC)
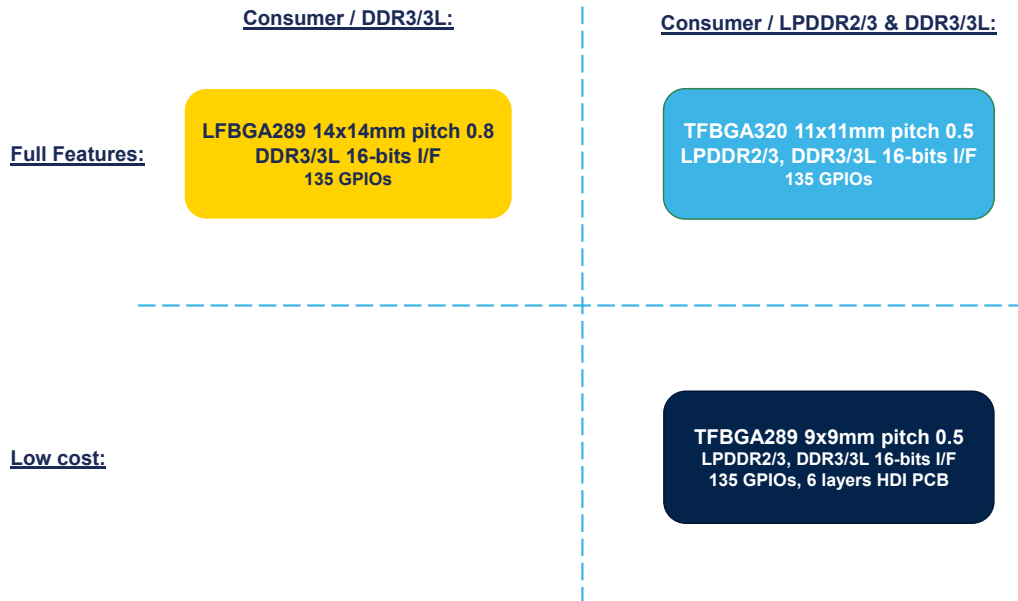- 2x SDIO3.0/SD3.01/eMMC4.51
- Dual Quad-SPI

Not Available on all product lines

This block diagram summarizes the key features and the available packages for STM32MP135F devices.
The STM32MP135F line integrates a Cortex-A7 core (with floating point unit and NEON SIMD Engine) running up to 1 GigaHertz , with 160 Kbytes of SRAM in total and up to 30 communication interfaces in addition to advanced security features.
Boxed red blocks are not available on all product lines.

Consumer / DDR3/3L:

Consumer / LPDDR2/3 & DDR3/3L:

Full Features:

LFBGA289 14x14mm pitch 0.8
DDR3/3L 16-bits I/F
135 GPIOs

TFBGA320 11x11mm pitch 0.5
LPDDR2/3, DDR3/3L 16-bits I/F
135 GPIOs

Low cost:

TFBGA289 9x9mm pitch 0.5
LPDDR2/3, DDR3/3L 16-bits I/F
135 GPIOs, 6 layers HDI PCB

The three packages are optimized for a wide range of usage.
They all offer the same number of GPIO count with different
cost, size and pitch trade-off.
Full feature packages provide maximum available GPIO count,
and exist in pitch 0.8mm for robust and low-cost PCB as well
as pitch 0.5mm for smaller PCB footprint.
Low cost packages are optimized for low cost Plated-Through
Hole (PTH) PCB routing and are available in two different ball
pitch for low-cost PCB or small PCB footprint.

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Thank you