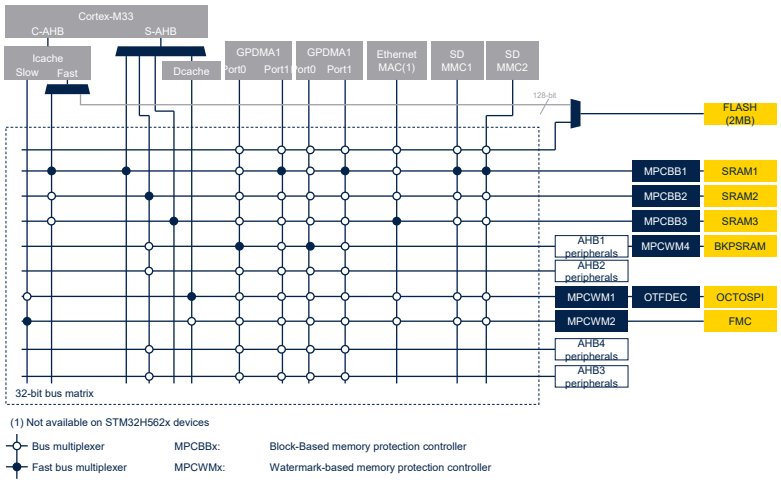
Hello, and welcome to this presentation of the bus matrixes interconnecting masters and slaves in the STM32H5.

Bus matrixes overview STM32H56x and STM32H573



- **Main Bus matrix**:
  - 32-bit multi-layer AHB bus matrix
  - 13 AHB master interfaces + 10 AHB slave interfaces
- **Instruction cache re-fill**
  - 128-bit direct path to flash memory
  - 32-bit path through the bus matrix to access external memories (FMC or OCTOSPI)

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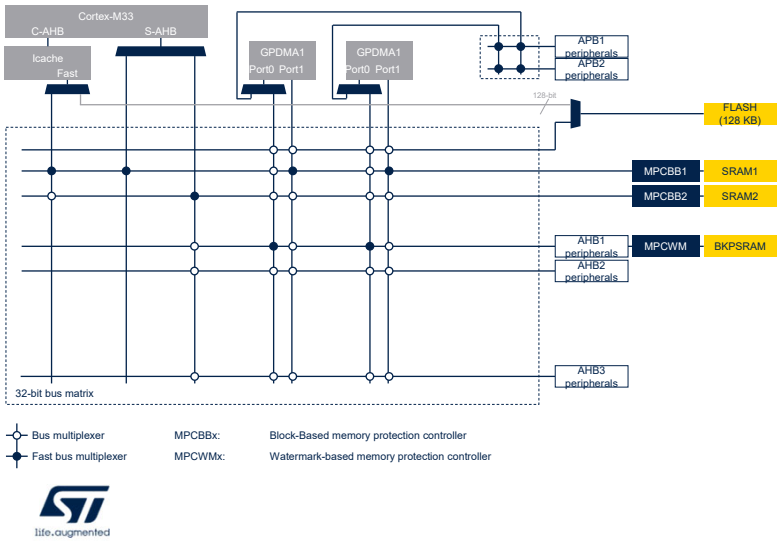
This slide describes the 32-bit bus matrix of STM32H56X and STM32H573 microcontrollers.
Masters are located at the top of the figure, while slaves are located on the right.
The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.
The STM32H5 Arm® Cortex®-M33 core is optimized for execution thanks to an instruction cache with direct access to Flash through the fast master port.
The AHB5 multilayer bus matrix, in the center of the figure, interconnects 13 masters and 10 slaves.
In order to offer a high bandwidth path to refill the instruction cache, a direct 128-bit bus connects the Fast

port of the instruction cache to the flash interface.
The bus matrix features a fast bus multiplexer used to connect each master to a given slave without latency.
For the same master, other slaves undergo a latency of at least one cycle at each new access.
You can see that a unique fast bus multiplexer is present in any particular column.
It selects the default slave for the related master, which is accessed without latency, for instance the FMC for the ICACHE slow port.
Access permissions of memories are controlled by the Block-Based memory protection controller (MPCBB) or Watermark-based Memory Protection Controller (MPCWM).
Note that the flash controller embeds dedicated protection mechanisms.

Bus matrixes overview STM32H503



- **Main Bus matrix**:
  - 32-bit multi-layer AHB bus matrix
  - 7 AHB master interfaces + 6 AHB slave interfaces
- **Instruction cache re-fill**
  - Same as for STM32H56x and STM32H573
- **Compared to STM32H56x and STM32H573:**
  - No data cache
  - No SRAM3
  - No AHB4
  - Neither Ethernet MAC nor SD/MMC controllers
  - Neither OCTOSPI nor FMC

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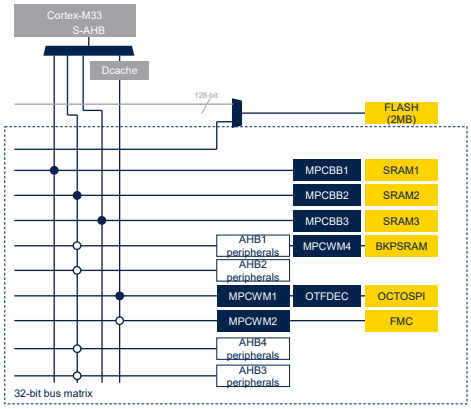
This slide describes the 32-bit bus matrix of STM32H503 microcontrollers.
The AHB5 multilayer bus matrix, in the center of the figure, interconnects 7 masters and 6 slaves.
Through multiplexers, the general-purpose DMA controllers have a direct access to APB buses, enabling them to efficiently service requests from APB peripherals.

S-AHB bus
STM32H56x and STM32H573



- **S-AHB interconnections (Internal memories):**
  - Used to access data located in peripheral/SRAMs area
  - 3 Masters connected to internal SRAMs (SRAM1, SRAM2, SRAM3, and BKPSRAM)
  - For SRAM1,2,3: Zero latency
- **DCACHE S-AHB (external memories)**
  - External memories are accessed through the data cache (FMC and OCTOSPI)
  - Used for instruction fetch and data access to the external memories mapped in the data region
  - Fetching instructions through this bus is less efficient than fetching through the C-AHB bus and ICACHE slow port

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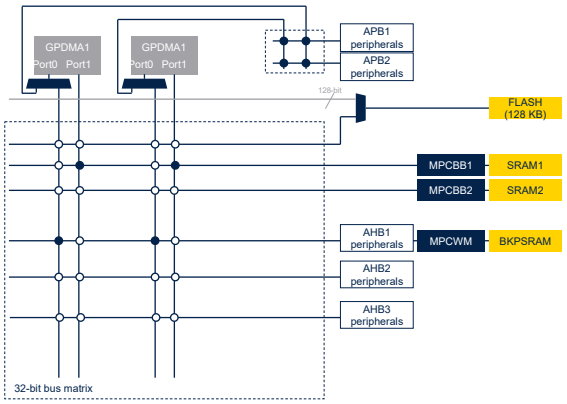
Accesses to internal SRAM memories initiated by the Cortex-M33 are performed through the S-AHB port.
The demultiplexer connected to the S-AHB port selects the slave port in the main bus matrix according to the address:

- SRAM1
- SRAM2
- SRAM3
- Backup SRAM

For SRAM1, 2, 3, latency is zero when no other master currently accesses the SRAM.
SRAM1, SRAM2 and SRAM3 are accessible on S-AHB bus with a continuous mapping.
Accesses to external memories connected to FMC or OctoSPI controllers are done through the DCACHE, even

if requests are marked as non-cacheable.
These accesses can be data requests as well as instruction requests mapped in the external data region of the mapping.
Note that fetching instructions through the S-AHB and DCACHE is less efficient than fetching through the C-AHB bus and ICACHE slow port.
This is the reason the ICACHE supports the address remapping capability.

GPDMA-bus STM32H503



- **GPDMA-bus has:**
  - 4 AHB master interfaces to BusMatrix
- **GPDMA1 and GPDMA2 can access :**
  - Internal memories: Flash, SRAM1/2, SRAM3(1) and BKPSRAM
  - External memories FMC or OCTOSPI(1)
  - AHB1 peripherals including the APB1 and APB2 peripherals through a direct path
  - AHB2 peripherals
  - AHB3 peripherals
  - AHB4 peripherals(1)
- **Default slaves:**
  - AHB1 peripherals on port 0
  - SRAM1 on port 1

(1) Not available on STM32H503x devices

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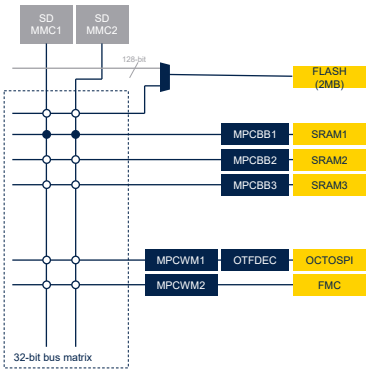
The GPDMA has a dual bidirectional master port: Port 0 and Port1, to support concurrent transfers over these ports.
Both master ports can access any memory-mapped resource in the microcontroller: internal and external memories, internal and external peripherals.
The port 0 is the default slave for AHB1 peripherals access.
The port 1 is the default slave for SRAM1 access.
Regarding the STM32H503, a direct access to APB1 and APB2 peripherals is performed through multiplexers and dedicated interconnect represented at the top of the figure.
Thus, transfer requests initiated by these peripherals can be handled quickly by using this low latency path.

SDMMC1 and SDMMC2 controllers DMA buses STM32H56x and STM32H573



- **SDMMC1 and SDMMC2 DMA master buses interface the bus matrix**
- **Used by the SDMMC1 and SDMMC2 DMA to load/store data from/to the memories :**
  - Internal memories (Flash and SRAM1/2/3)
  - External memories (FMC or OCTOSPI)
- **Default Slave:**
  - SRAM1 for both

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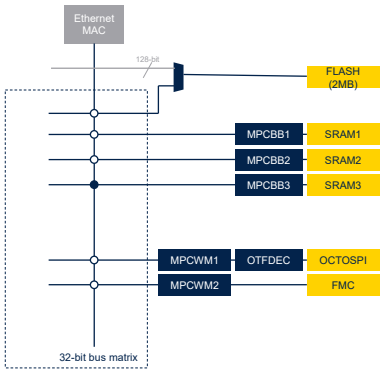
The SD and MMC controllers are master modules.
They can access any memory, internal or external, because data written to SD/MMC is read from buffers in RAM and data read from SD/MMC is stored into buffers in RAM.
The default slave is SRAM1 for both controllers.

Ethernet MAC bus
STM32H56x and STM32H573



- **One master interface to BusMatrix**
- **Can access to :**
  - Internal memories (Flash and SRAM1/2/3)
  - External memories FMC or OCTOSPI
- **Default Slave:**
  - SRAM3

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The Ethernet MAC integrates a dedicated bus master, that has a direct access to internal memories as well as external memories.
The default slave is SRAM3.

Thank you

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In addition to this presentation, you can refer to the following presentations:

- Instruction cache (ICACHE)
- Data cache (DCACHE)
- Flash memory (FLASH)
- Power management (PWR)
- Reset and clock controller (RCC).