Hello, and welcome to this presentation of the STM32C0 reset and clock controller.

Overview

- The STM32C0 reset and clock controller manages system and peripheral clocks
  - Two internal oscillators
  - Two external oscillators (crystal or resonator) with shared pins on smaller packages
  - Several peripherals have independent clocks
- The RCC manages the various system and peripheral resets

Application benefits

- High flexibility in choice of clock sources to meet consumption and accuracy requirements
- Many independent peripheral clocks allow for adjusting power consumption without impacting communication baud rates, and to keep some peripherals active in low-power modes
- Safe and flexible reset management

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2

The STM32C0 reset and clock controller manages system and peripheral clocks.
STM32C0 devices embed two internal oscillators and 2 oscillators for an external crystal or resonator.
Note that no PLL is present in the STM32C0.
Many peripherals have their own clock, independent of the system clock.
The RCC also manages the various resets present in the device.
The STM32C0 RCC provides high flexibility in the choice of clock sources, which allows the system designer to meet both power consumption and accuracy requirements.
The numerous independent peripheral clocks allow a designer to adjust the system power consumption without

impacting the communication baud rates, and also keep some peripherals active in low-power modes. Finally, the RCC provides safe and flexible reset management.

Reset key features

Safe and flexible reset management without external components

- Manages three types of reset:
  - System reset
  - Power reset
  - RTC domain reset
- Peripherals have individual reset control bits

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Safe and flexible reset management without any need for external components reduces application costs.
The RCC manages three types of resets: the system reset, the power reset and the backup domain reset.
The peripherals have individual reset control bits.

Reset sources

- System reset
  - Resets all registers except the reset flags in the RCC control/status register 2 (RCC_CSR2) and the registers in the RTC domain
  - Reset sources
    - Low level on the NRST pin (external reset)
    - WWDG event
    - IWDG event
    - A software reset (through NVIC)
    - Low-power-mode security reset
    - Option byte loader reset
    - Power On Reset reset
  - The Reset Source flag is in the RCC_CSR register

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4

The first type of reset is the System reset, which resets all the registers except reset flags present in the RCC control and status register 2. It does not reset the RTC domain either.

The System reset sources are:

- The external reset (generated by a low level on the NRST pin),
- A window watchdog event,
- An independent watchdog event,
- A software reset request,
- A low-power-mode security reset (which is generated when Stop, Standby or Shutdown mode is entered but is prohibited by the option byte configuration),
- An option byte loader reset,

- And a Brown-out or Power-on reset.

The reset source flag can be found in the RCC Control and Status register.

Reset sources

- PF2-NRST
  - The configuration of the Reset circuitry is done through the option bytes NRST_MODE[1:0] and IRHEN

Mode	Configuration		Behavior
	NRST_MODE	IRHEN	
Input/Output (Legacy)	11	0	20 µs output pulse generated on NRST pin in case of Internal Reset
		1	Output pulse maintained until NRST voltage reach Vil threshold (~0.3VDD) This function allows the detection of internal reset sources by external components when the line faces a significant capacitive load
Input only	01	x	Internal Reset are not propagated outside of the part
GPIO	10	x	Port F pad 2 (PF2) only, no reset pin

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5

Two fields in the option bytes are used to configure the NRST pin:

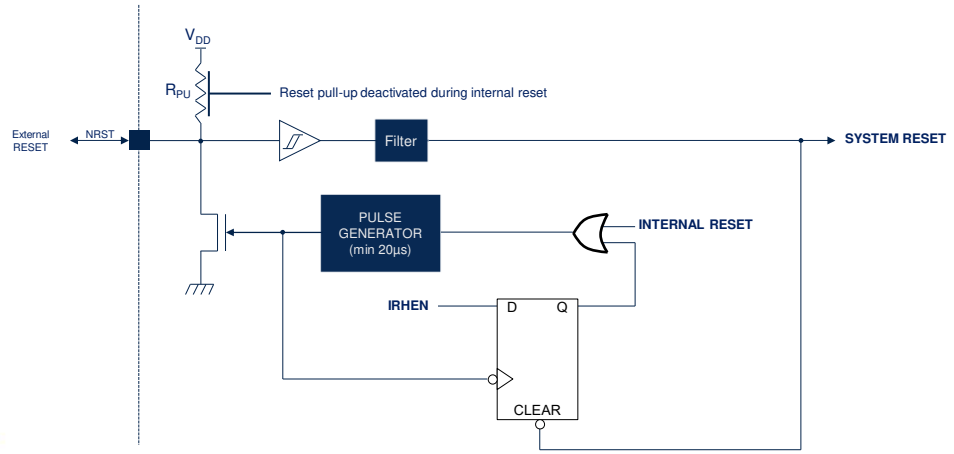
- NRST_MODE selects the operation mode of the NRST pin: input / output reset, input only reset or GPIO.
- IRHEN stands for Internal Reset Holder Enable. When this mode is enabled, the NRST pin is driven low until its voltage level goes under the voltage input low threshold.

Upon power reset or wakeup from shutdown mode, the NRST pin is configured as Reset input/output and driven low by the system until it is reconfigured to the expected mode when the option bytes are loaded.

Reset sources

No external components are needed due to internal filter and power monitoring

System reset sources can reset external components



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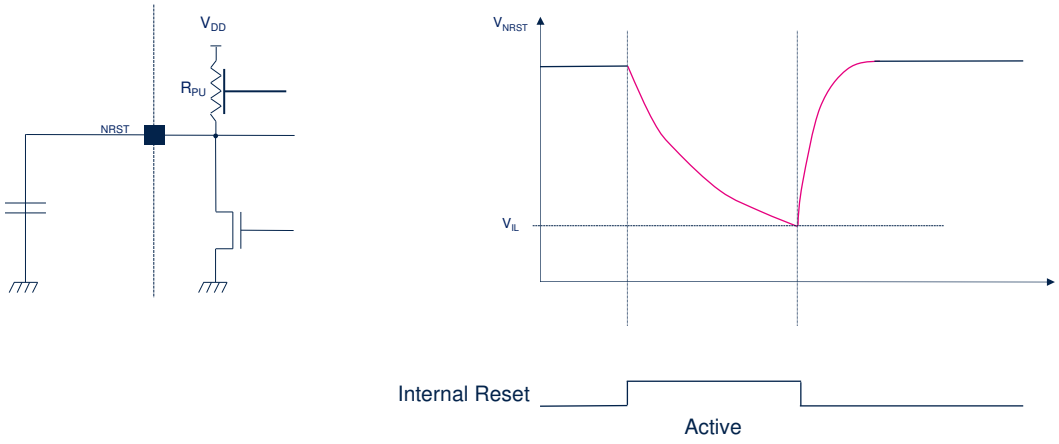
6

Here is the simplified block diagram of the system reset.
All internal reset sources provide a reset signal on the NRST pin, which can be used to reset other components of the application board.
In addition, no external reset circuitry is needed due to the internal glitch filter and the safe power monitoring feature which guarantees the reset of the application when VDD is below the selected threshold.
The internal pull-up on the NRST pin, which maintains a high level when no reset signal drives it low, is deactivated when an internal reset is driven in order to reduce power consumption under reset.
Additionally, except the debug pins and some test pins, all I/O pins are placed in analog mode during and after reset

to eliminate power consumption through the Schmitt trigger when the I/Os are floating under reset and before software initialization.

Reset sources

No external components are needed, in case of strong capacitive load on the line, Reset Holder can be used



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The purpose of the reset holder is to maintain NRST driven LOW until the voltage level of this signal goes below VIL. This is useful when the NRST line has an important capacitive load.

Reset sources

- Power reset
  - Sources
    - Brown-out reset (BOR) or Power-On reset (POR)
      - Rsets all registers
    - Exit from Standby
      - Resets all registers in VCORE domain
      - Registers outside the VCORE domain are not impacted (Back up register, WKUP, IWDG, and Standby/Shutdown mode control
      - Exit from Shutdown generates a BOR reset, resets all registers
- RTC domain reset
  - Two specific resets
    - Software reset through RTCRST control bit
    - VDD power-on

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8

The second type of reset is the power reset.
The Brown-out reset (BOR) resets all registers in VCORE power domain.
When exiting Standby mode, all registers powered by the regulator are reset.
When exiting Shutdown mode, a Brown-out reset is generated.
The third type of reset is the RTC domain reset, which affects the LSE oscillator, the RTC and the RCC control & status register 1.
Note that backup registers are outside the VCORE domain.

Clock key features

Choice of clock sources for power, accuracy, and performance

- Two internal clock sources
  - High-speed internal 48 MHz RC oscillator (HSI48)
  - Low-speed internal 32 kHz RC oscillator (LSI)
- Two external oscillators
  - High-speed external 4 to 48 MHz oscillator (HSE) with clock security system
  - Low-speed external 32.768 kHz oscillator (LSE) with clock security system
- One audio clock source I2S_CKIN pin
  - Direct clock input for I2S1 peripheral

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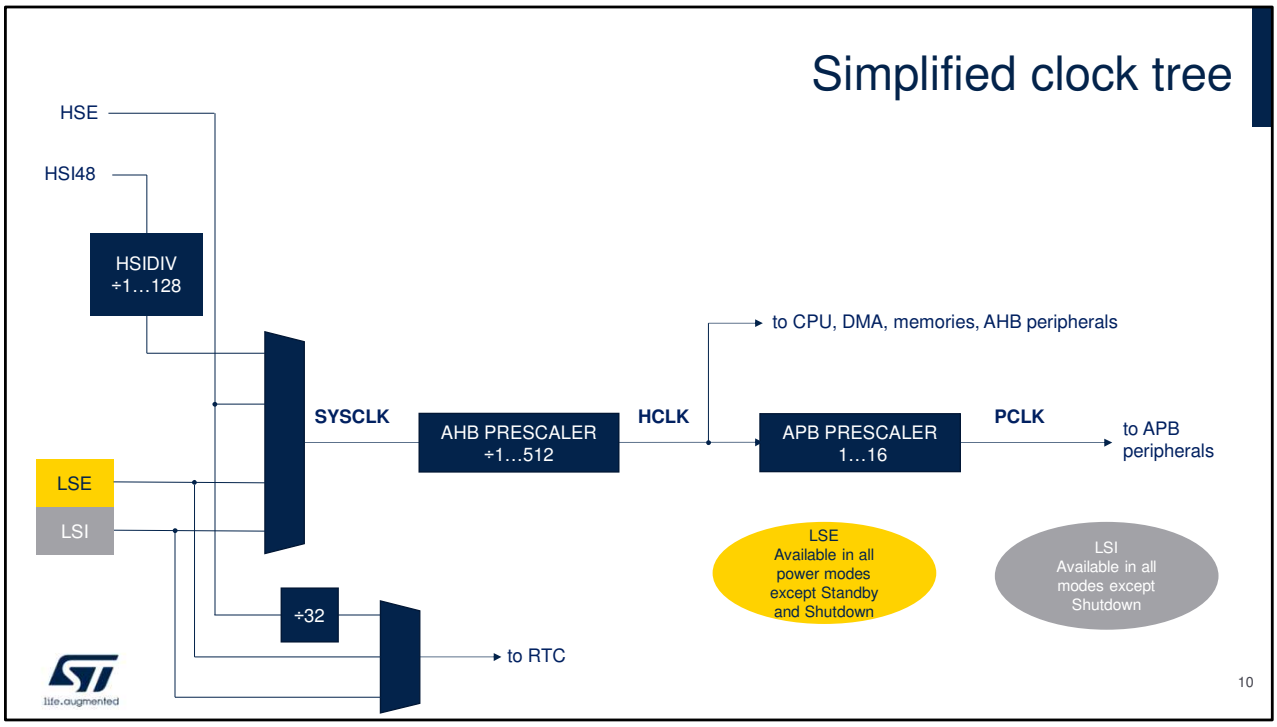
9

The RCC offers a large choice of clock sources, which can be selected depending on low-power, accuracy, and performance requirements.
STM32C0 devices embed 2 internal clock sources: a high-speed internal 48 MHz RC oscillator (HSI48) and a low-speed internal 32 kHz RC oscillator (LSI).
STM32C0 devices embed two oscillators for use with an external crystal or resonator: a high-speed external 4 to 48 MHz oscillator (HSE) with a clock security system and a low-speed external 32.768 kHz oscillator (LSE) also with a clock security system.
The I2S_CKIN pin is one of the possible clock sources of the I2S1 peripheral.
STM32C0 devices does not embed PLL but the HSI48

provides the max frequency for the device which can be then reduced by clock dividers.



The system clock can be derived from the high-speed internal 48 MHz RC oscillator (HSI48) or the high-speed external 4 to 48 MHz oscillator (HSE).
The AHB clock, called HCLK, is derived by dividing the system clock by a programmable prescaler.
The APB clock, called PCLK is generated by dividing the AHB clock by programmable prescalers.
The RTC clock is generated by the low-speed external 32.768 kHz oscillator (LSE), the low-speed internal 32 kHz RC oscillator (LSI), or the HSE divided by 32.
The LSE can remain enabled in all low-power modes except Shutdown.
The LSI can remain enabled in all modes except Shutdown and Standby.

Each oscillator can be switched on or off independently when it is not used, to optimize power consumption.

High-Speed Internal (HSI48) clock

1% accuracy and fast wakeup time

- HSI48 48 MHz, factory- and user-trimmed
- HSI48 after HSIDIV is the
  - Wakeup clock from Stop mode
  - Backup clock for Clock Security System (CSS)
- I2C1, U(S)ART1-2 can enable the HSI48 during Stop mode to detect their wakeup from Stop sequence
  - HSI48 remains off during Stop mode except for the peripheral wakeup sequence detection

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11

The high-speed internal oscillator is a 48 MHz RC oscillator which provides 1% accuracy and fast wakeup times.
The HSI48 is trimmed during production tests and can be user-trimmed.
The HSI48 can be selected as clock at wakeup from Stop mode, and as the backup clock if an HSE failure is detected by the Clock Security System.
The HSI48 can be automatically awaken up when exiting Stop mode in order to make it available for peripherals when it is not used as the system clock.
The USART1, USART2 and I2C1 peripherals can enable the HSI48 oscillator even when the MCU is in Stop mode, if HSI48 is selected as clock source for one of those

peripherals.

HSI48 characteristics

	HSI48 (48 MHz)	
Accuracy (typ.)	0 – 85°C	+/- 1 %
	-40 – 125°C	- 2.5 / + 2 %
Consumption (typ.)	260 µA	
Startup time (typ.)	1.4 µs	

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This table provides the characteristics of the HSI48 clock.
The HSI48 accuracy can be improved by implementing a trimming procedure, based on TIM14, TIM16 and TIM17 channel 1 input capture.
A clock reference such as HSE/32 or LSE is used for high accuracy capture of the current value of the counter clocked by HSI48.
The HSI clock has a typical 1.4 microsecond startup time while the HSE clock has a typical 2 millisecond startup time.

High-Speed External (HSE) clock

Safe crystal system clock

- HSE 4-48MHz
  - External source (Bypass mode) up to 48 MHz
  - External crystal/ceramic resonator (4 - 48 MHz)
- Clock Security System (CSS)
  - Automatic detection of HSE failure with switching to HSI48 (after HSIDIV)
    - Non-maskable interrupt generation
    - Break input to TIM1/TIM16/TIM17
      - Critical applications such as motor control can be put in a safe state

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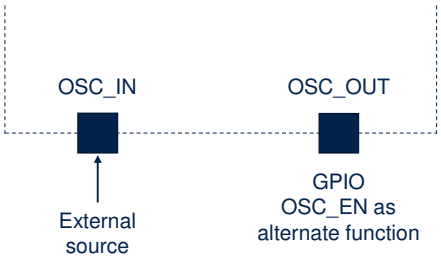
13

The high-speed external oscillator provides a safe crystal system clock.
The HSE supports a 4 to 48 MHz external crystal or ceramic resonator, and also an external source in bypass mode.
A clock security system allows an automatic detection of HSE failure.
In this case a Non-Maskable Interrupt is generated, and a break input can be sent to timers in order to put critical applications such as motor control in a safe state.
When an HSE failure is detected, the system clock is automatically switched to an internal oscillator, the HSI48, so the application software does not stop in case of crystal failure.

High-Speed External (HSE) clock

- New Alternate Function is available on the HSE system to be used with oscillators
  - When the external clock is used in bypass mode, a new pin OSC_EN is available for the application to be used as ENABLE signal for the external clock. It is used to switch off the external clock when entering Low Power modes.



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14

In External source mode, also called HSE bypass mode, an external clock source must be provided.
It can have a frequency of up to 48 MHz.
The external clock signal (square, sinus or triangle) must drive the OSC_IN pin.
The OSC_OUT pin can be used as GPIO or it can be configured as an OSC_EN alternate function, to provide a signal enabling the stop of the external clock synthesizer ,when the device enters low-power modes.

Low-Speed Internal (LSI) clock

Ultra-low power internal 32 kHz oscillator
Available in all modes except Shutdown

	LSI 32 kHz
Accuracy (typ.)	Over Temperature and VDD +/-7%
Consumption (typ.)	110 nA

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15

STM32C0 devices embed an ultra-low-power 32 kHz RC oscillator, which is available in all modes except Shutdown.
The LSI can be used to clock the RTC and the independent watchdog.
The accuracy of the LSI is plus or minus 1.5% over temperature and plus 0.1 minus 0.2% over voltage.
The LSI consumption is typically 110 nA.
If the Independent watchdog (IWDG) is started by either hardware option or software access, the LSI oscillator is forced ON and cannot be disabled.

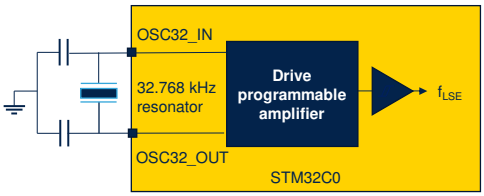
Low-Speed External (LSE) clock

32.768 kHz configurable for low-power or high-drive

Available in RUN, Sleep, Stop modes

- The LSE can be used with external crystal or ceramic resonator, or with external clock source in bypass mode
- **Clock Security System on LSE**: available in all modes except Standby and Shutdown
- Operates under reset
- The LSE can be used as the source of SYSCLK

Mode	Maximum critical crystal gm (µA/V)	Consumption (nA)
Medium-high driving	1.7	500
High driving	2.7	630



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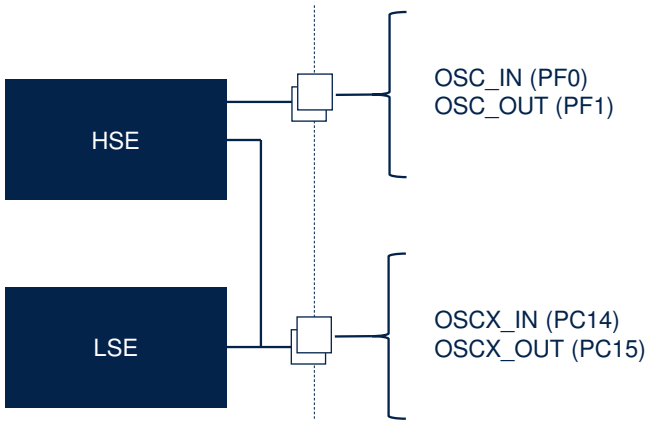
16

The 32.768 kHz low-speed external oscillator can be used with external crystal or resonator, or with an external clock source in bypass mode.
In bypass mode, an external clock source must be provided. It can have a frequency of up to 1 MHz.
The oscillator driving strength is programmable.
It can be changed at runtime using the LSEDRV bit in the RCC control/status register 1 (RCC_CSR1) to obtain the best compromise between robustness and short start-up time on one side and low-power consumption on the other side.
A clock security system monitors for failure of the LSE oscillator.
In case of failure, the application can switch the RTC clock

to the LSI and an NMI is automatically generated.
The CSS is functional in all modes except Shutdown.
It is also functional under reset.
The LSE can be used as the source clock of SYSCLK.

HSE / LSE shared pins

- HSE oscillator pins remap can be controlled through HSE_NOT_REMAPPED option bit
- The HSE oscillator can be connected to
  - Either OSC_IN, OSC_OUT dedicated pins
  - or pins shared with LSE oscillator OSCX_IN and OSCX_OUT



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17

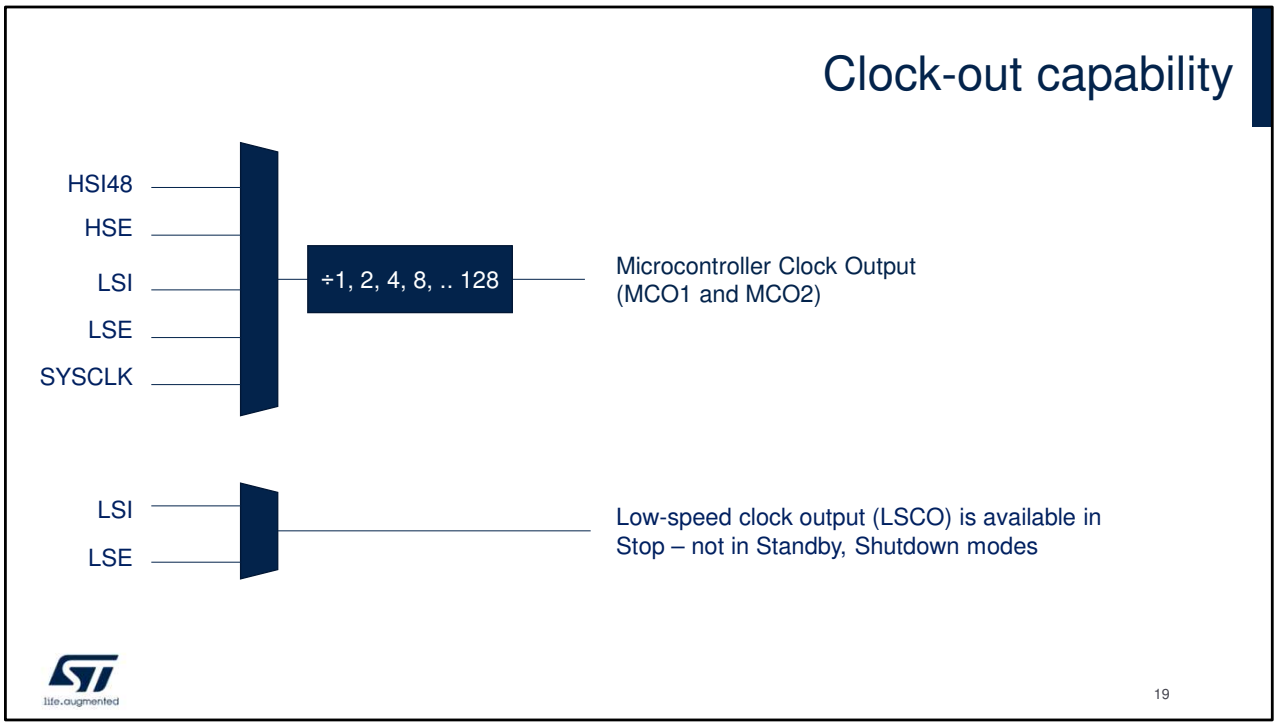
STM32C0 introduces oscillator pins sharing between high speed and low speed oscillators.
This remapping option offers high level of flexibility especially useful on low pin-count devices.
Thus PC14-OSCX_IN/PC15-OSCX_OUT are shared by both LSE and HSE and the two clock sources cannot be used simultaneously.

System clock

- Selected between LSI, LSE, HSI48 possibly prescaled, and HSE clock sources
- System clock, AHB and APB maximum frequency: 48 MHz
- Single power range

SYSCLK	HSI48	HSE
48 MHz	48 MHz	48 MHz

The system clock is selected among the LSI, LSE, HSI48 and HSE clock sources.
The maximum system clock frequency is 48 MHz.
The APB bus frequencies are up to 48 MHz.
Upon system reset, the HSISYS clock derived from HSI48 oscillator is selected as system clock.
When a clock source is used as a system clock, it is not possible to stop it.



The various clocks can be output on I/O pads.
The MCO and MCO2 pins output, independently of each other, the clock selected from: LSI, LSE, SYSCLK, HSI48, and HSE.
The multiplexers for MCO and MCO2, respectively are further divided by a programmable ratio.
The LSCO pin allows outputting of low-speed clocks: LSI or LSE.
The low-speed clock output is available in Stop mode.

Clock gating

Dynamic consumption optimization in Run and Sleep modes

- Peripheral clock enable registers
  - Peripheral clocks disabled by default (except Flash)
  - Registers read and write access not supported when clock is disabled
  - The memory interface clocks (Flash memory and SRAM interfaces) can be stopped by software during sleep mode
- Peripheral clock enable registers in Sleep and Stop modes
  - Enables or disables the peripheral clocks in Sleep and Stop modes
    - No effect if corresponding peripheral clock enable is cleared
    - Controls both bus and kernel clocks
    - Affects Sleep and Stop modes (for peripheral with independent clock active in Stop mode)

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20

The dynamic power consumption can be optimized by using peripheral clock gating.
Each peripheral clock can be gated ON or OFF in Run and Low-power run modes.
By default, the peripheral's clock is disabled, except the Flash memory clock which is enabled by default.
When a peripheral's clock is disabled, the peripheral's registers cannot be read or written.
Other registers allow for configuring the peripheral's clock during the Stop and Sleep modes.
This also affects Stop mode for peripherals with an independent clock active in Stop mode.
These control bits have no effect if the corresponding peripheral clock enable is cleared.

By default, no active peripheral clock is gated in Stop, Sleep and Low-power Sleep modes.
When a peripheral is not needed, its clock enable bit should be cleared to reduce the power consumption.

Interrupts

Interrupt event	Description
LSE clock security system	Set when a failure is detected in the LSE oscillator
HSE clock security system	Set when a failure is detected in the HSE oscillator
HSE ready	Clock ready caused by the HSE oscillator
HSI48 ready	Clock ready caused by the HSI48 oscillator
LSE ready	Clock ready caused by the LSE oscillator
LSI ready	Clock ready caused by the LSI oscillator

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This slide lists the RCC interrupts.
The LSE and HSE clock security systems, and all oscillator ready signals can generate an interrupt.
Note that the flag indicating an automatic clock switch in case of external LSE or HSE loss has to be cleared in the NMI interrupt service routine.

Main Difference vs. STM32F0 and STM32G0

	STM32F0	STM32G0	STM32C0
NRST	Input & output	GPIO, Input , Input & output	GPIO, Input , Input & output
Reset Holder	No	Yes	Yes
PLL	One output	Three ouputs	No PLL
CSS on LSE + LSCO	No	Yes	Yes
HSI divider to SYSCLK	No	Yes	Yes
Timers running at 2xSYSCLK	No	Yes	No
HSI / MAX CPU speed (MHz)	8 / 48	16 / 64	48 / 48

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22

The RCC unit implemented in the STM32C0 is like STM32G0 and offers new features in comparison to STM32F0 microcontrollers.
The NRST pin has 3 possible usages:

1. Reset input used by an external logic to signal a reset condition to the STM32C0
2. Reset input & output (legacy mode), any valid reset signal on the pin is propagated to device internal logic and all internal reset sources are externally driven through a pulse generator to this pin
3. GPIO, in this mode, the pin can be used as standard GPIO, reset is only possible from the device's internal reset sources.

The reset holder option can be used, if enabled in the

option bytes, to ensure that the pin is pulled low until its voltage meets the VIL threshold.
No PLL is embedded for cost purposes. The HSI48 oscillator allows the system to run at maximum speed of 48 MHz.
The Clock Security System (CSS) also monitors the LSE and detects failures.
If the low-speed external 32.768 kHz oscillator (LSE) is used as system clock, and a failure of LSE clock is detected, the system clock switches automatically to the low-speed internal 32 kHz RC oscillator (LSI).
Regarding the STM32C0, the timer clock TIMPCLK runs at PCLK frequency if the APB prescaler division factor is set to 1, or at twice the PCLK frequency otherwise. So the max frequency of timers is SYSCLK frequency.

Related peripherals

- Refer to these presentations linked to this peripheral
  - STM32C0 power control (PWR)
  - STM32C0 interrupts (NVIC-EXTI)

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23

In addition to this training, you may find the Power Control and Interrupt Controller trainings useful.

References

- For more details, please refer to following sources
  - AN2867 Oscillator design guide for STM8S, STM8A and STM32 microcontrollers

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24

For more details, please refer to application note AN2867, an oscillator design guide for STM8S, STM8A and STM32 microcontrollers.

Thank you

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Thank you for attending this presentation!