Hello, and welcome to this presentation, which describes the autonomous operation of the GPDMA during low power modes.

Autonomous GPDMA

- DMA finely manages its own clock gating; requesting its clock from the RCC only when needed in any power mode
- In Sleep mode, the DMA can be programmed to either:
  - Wake up the Cortex-M33 CPU on completion of a specific transfer via an enabled interrupt
  - Continue autonomously and perform another LLI_{n+1} transfer

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To save power while the GPDMA executes programmed linked-list transfers, the DMA controller hardware automatically manages its own clock gating and generates a clock request output signal to the RCC, whenever the device is in Run or Sleep mode.
When used in Sleep mode, as shown in the next slide, a CPU wakeup can be requested on completion of a specific channel transfer.
Alternatively, the DMA can autonomously perform a next LLI transfer.

Autonomous GPDMA

Low-power mode	GPDMA
Sleep	No effect ➢ DMA interrupts cause the device to exit Sleep mode
Stop	The content of the DMA registers are kept when entering Stop mode
Standby	The DMA is powered down and must be reinitialized after exiting Standby mode

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This table summarizes the effect of low-power modes on the GPDMA.
Sleep mode has no effect on the DMA which remains functional. An interrupt generated by the DMA controller can cause the exit from sleep mode.
In stop mode, the GPDMA is not functional, however the content of the GPDMA registers is kept.
In standby, the GPDMA is powered down. It must be reinitialized when exiting from Standby.

Thank you

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In addition to this presentation, you can refer to the other presentations on the GPDMA:

- DMA overview
- DMA transfers hardware and software views
- DMA linked list
- DMA Circular buffering & double buffering
- DMA 2D addressing
- DMA Register file
- DMA Error reporting
- DMA Input-output LLI control.

You can also refer to the presentation on power management.