Hello, and welcome to this presentation of the STM32C0 power backup register

Overview

- The STM32C0 PWR backup registers are intended to keep key information about the application state during the Standby are reset followed by the resume from Standby
- As there is no secondary power supply – battery option - the PWR backup register keeps information as long as the main VDD voltage is present

Application benefits

- Keeps information in all low-power modes and after resume except Shutdown
- Can be used to restore the context of the application after wake-up from Standby mode

The STM32C0 PWR backup registers are intended to keep some key information about the application state during the low power modes and resume from it except Shutdown.
As there is no secondary power supply, such as a battery, the PWR backup registers keep information as long as the main VDD voltage is present.

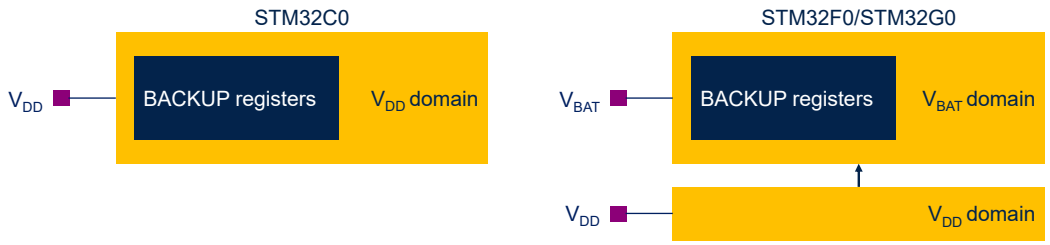
Backup register key features

- The backup registers are organized in 4 x 16-bit registers BKPxR[15:0] stored in the APB memory space
- The backup registers are not reset when exiting Standby mode as well as when the PWRRST bit of the RCC_APBRSTR register is set
- Requires three (writing) or two (reading) extra APB clock cycles, compared to standard APB access

The backup registers are organized in 4 x 16-bit registers stored in the APB memory space.
They can store state information that is preserved when switching to standby power state.
The backup registers are not reset when exiting Standby mode as well as when the PWRRST control bit of the RCC_APBRSTR register is set.
This PWRRST control bit is used to reset the PWR domain.
In term of wait states, access to backup registers require three extra APB clock cycles on write and two on read, compared to standard APB access.

Main Difference C0 vs. F0 and G0

- Main difference vs. STM32F0x and STM32G0x is the backup register power supply
- The backup registers on STM32C0x is powered from the V_{DD} domain as there is no V_{BAT} domain implemented



life.augmented

4

The backup registers on STM32C0x is powered from the VDD domain as there is no Vbat domain implemented.
In STM32F0 and STM32G0 series, the contents of backup registers may be preserved when the VDD power supply is switched off.

Related peripherals

- Refer to the following training module linked to this peripheral
  - STM32C0 Power control (PWR)

life.augmented

In addition to this presentation, you may find the Power Control training module useful.

Thank you

life.augmented

Thank you for attending this presentation!