Hello, and welcome to this presentation of the interface of STM32U5 Digital Filters for Sigma-Delta modulators, covering both the Multi-Function Digital Filter or MDF and the Audio Digital Filter or ADF.

Agenda

1 Overview

2 ADF/MDF versus DFSDM

3 ADF/MDF presentation

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This presentation is split into three parts:

- First an overview
- Then a comparison between ADF/MDF modules present in the STM32U5 and the DFSDM module present in the STM32L5. DFSDM stands for Digital filter for Sigma-Delta modulators interface.
- And finally, a detailed description of the ADF and MDF modules.

1

Overview

MDF stands for **M**ulti-function **D**igital **F**ilter

ADF stands for **A**udio **D**igital **F**ilter

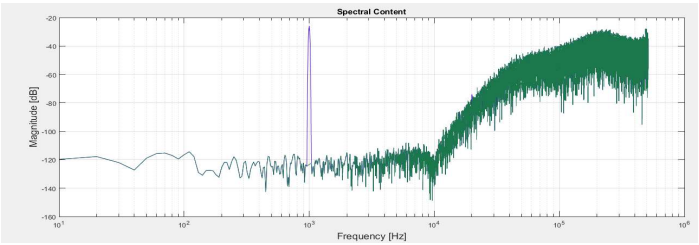
ADF is a subset of MDF, with a Sound Activity Detector

ADF/MDF is dedicated to the connection of external sensors using Sigma-Delta A/D converters

ADF/MDF target the following applications:

- Motor Control
- Audio Capture and Detection
- Metering

SDM4 quantization noise example



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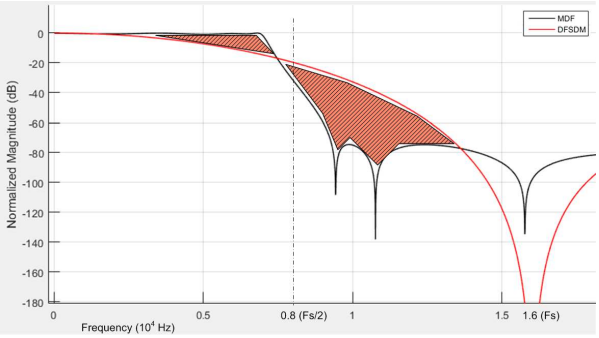
3

The Multi-function Digital Filter (MDF) and Audio Digital Filter (ADF) are high-performance modules dedicated to the connection of external sigma-delta (ΣΔ) modulators for sample acquisition.
They also support configurable filter functions.
ADF is a subset of MDF, except for the sound activity detector, which is supported only by ADF.
ADF and MDF target the following applications:
Audio capture and detection
Metering.
In addition, MDF can be used for motor control.
The figure on the right shows an example of the spectrum aspect of a sine wave converted by a fourth order single-bit sigma-delta ADC. The main goals of MDF and ADF are to keep the lower frequency part (here the signal to up to 10 kHz), to remove the quantization noise and to reduce the

sampling rate.

2

ADF/MDF Versus DFSDM



ADF/MDF replaces the DFSDM block

Main ADF/MDF improvements versus DFSDM:

- Supports autonomous mode
- Kernel clock just needs to be twice the bitstream rate
- Improved image rejection in the Fs/2 to Fs band
- Improved in-band droop
- Addition of a high-pass filter
- Gain/attenuation steps of ~ 3dB
- Saturation blocks
- Voice and Sound activity detector

Benefits:

- Lower power consumption
- Better speech capture quality
- More sophisticated trigger detection

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4

The STM32L5 includes a module called DFSDM, which stands for Digital filter for Sigma-Delta modulators interface. Let's list the improvements made by ADF/MDF compared to DFSDM.

Firstly, ADF and MDF support Low-power background autonomous mode (or LPBAM), which allows these peripherals to be functional and autonomous in stop modes, without any software running.

Another clocking benefit is that: the kernel clock of ADF/MDF only needs to be twice the bitstream rate, while the DFSDM requires a ratio of four.

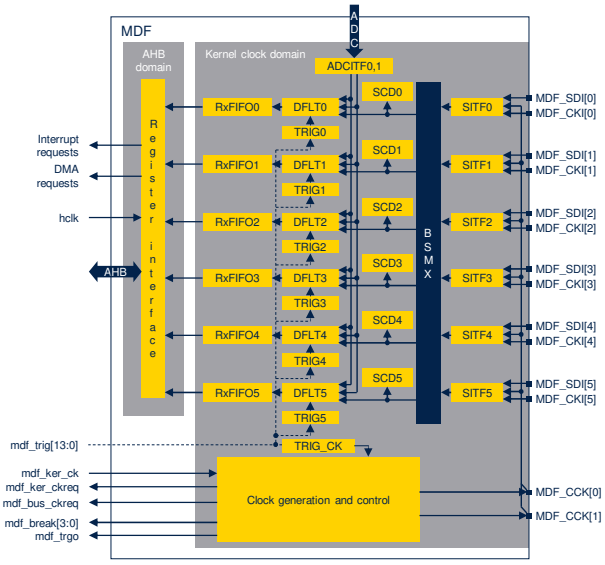
In the frequency range from half of the sampling frequency to sampling frequency, ADF/MDF improves image rejection. Refer to the figure on the left.

The Cascaded-integrator-comb (CIC) filter implemented in ADF/MDF also improves in-band droop.

A high-pass filter is added to remove low frequency noise from the input signal.
The gain or attenuation can be adjusted with an accuracy of 3 decibels.
ADF/MDF also features saturation blocks which prevent wrap-around of the binary code when the code exceeds its maximum or minimum value.
Finally, ADF supports a voice and sound activity detector.
All these innovations contribute to reducing the power consumption and improving the quality of the speech capture.
A flexible trigger interface can be used to control the start of the conversion. This timing control can trigger simultaneous conversions or insert a programmable delay between conversions.

3

MDF Overview



MDF has:

- 6 flexible serial interfaces (SITF) with 2 common clocks for connecting external sensors
- A full matrix (BSMX) allowing the connection of any serial interface to any digital filter
- 6 flexible digital filters (DFLTx) configurable for motor control, metering or audio capture
- Flexible TRIGGER interface to control filter acquisition
- Many other functions: Short-circuit detector (SCD), Saturation, Gain control, Snapshot, ADCITF....
- Dual clock domain, in order to increase flexibility and reduce the power consumption

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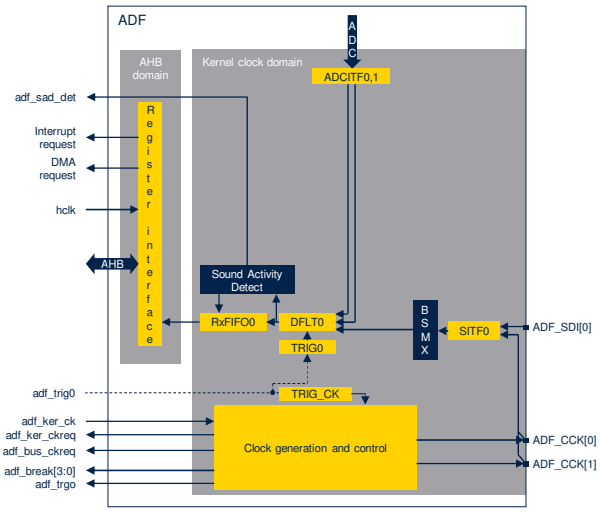
5

MDF incorporates several features, making it very suitable for interfacing sigma-delta modulators for audio capture, motor control and metering applications.
MDF incorporates:

- 6 flexible serial interfaces (SITF), and 2 common clocks (inputs/outputs) for connecting of external sensors
- A full digital matrix (BSMX) allowing any serial interface to be connected to any digital filter
- 6 flexible digital filters (DFLT) configurable for motor control, metering or audio capture
- 2 parallel interfaces for the internal ADCs, only one is used in the STM32U5 to interconnect ADC1 to MDF
- Flexible TRIGGER interface to control filter acquisition
- Many other functions: Short-Circuit Detector (SCD), Out of limit detector, Clock absence detector, Saturation, Gain control, Snapshot

MDF has two clock domains, to increase flexibility and reduce power consumption.

ADF Overview



ADF has:

- 1 flexible serial interface (SITF) with 2 common clocks for connecting external sensors
- An audio digital filter (DFLT)
- Flexible TRIGGER interface to control filter acquisition
- Sound activity detection (SAD)
- Dual clock domain to increase flexibility and reduce the power consumption

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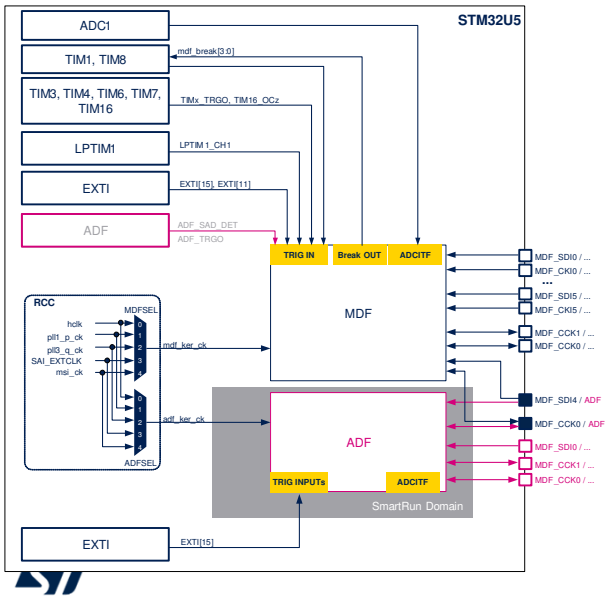
6

ADF is a sub-set of MDF, making it very suitable mainly for audio applications.
ADF incorporates:

- 1 flexible serial interface, and 2 common clocks (input/output) for connecting of external microphones.
- A BSMX for selecting the desired bitstream.
- A configurable audio digital filter for audio capture.
- 2 parallel interfaces for internal ADCs, not used in the STM32U5
- Flexible TRIGGER interface to control filter acquisition
- A sound activity detector, for sound or voice detection

ADF has two clock domains to increase flexibility and reduce power consumption.

MDF and ADF Integration



- MDF is in the main domain
- ADF is in the SmartRun domain
- MDF and ADF share the same I/Os in order to share the same microphone if needed
- There are several trigger possibilities for MDF
- ADF can trigger MDF when a sound is detected or when an acquisition is started

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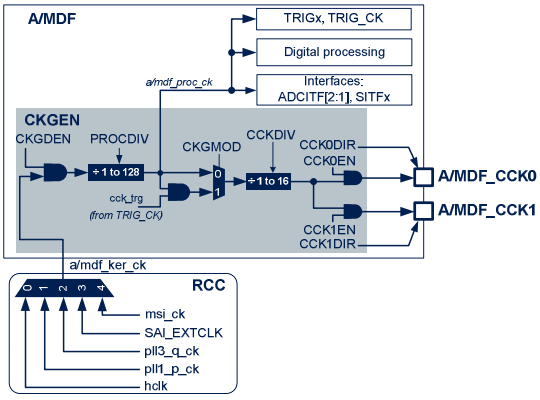
This slide shows the integration of MDF and ADF in STM32U5.
MDF is in the main domain, while ADF is located in the SmartRun domain for low-power applications. Thus the ADF can run autonomously in stop 2 and an interesting use case is a wakeup request from ADF in the case of voice detection.
Some pins are shared between MDF and ADF in order to share the same microphone if needed.
MDF can be triggered by several peripherals, such as timers, EXTI.
ADF can trigger MDF when a sound is detected or when an acquisition is started.
Trigger details are explained later in this presentation.

Clock Generator (CKGEN)



- The RCC provides a rich choice of clock sources for the A/MDF kernel clock
- Most of the processing is done with the kernel clock divided by PROCDIV (a/mdf_proc_ck)
- A/MDF_CCK[1:0] pins can be either output or input, depending on CCK[1:0]DIR
- A/MDF_CCK[1:0] are derived from a/mdf_proc_ck divided by CCKDIV

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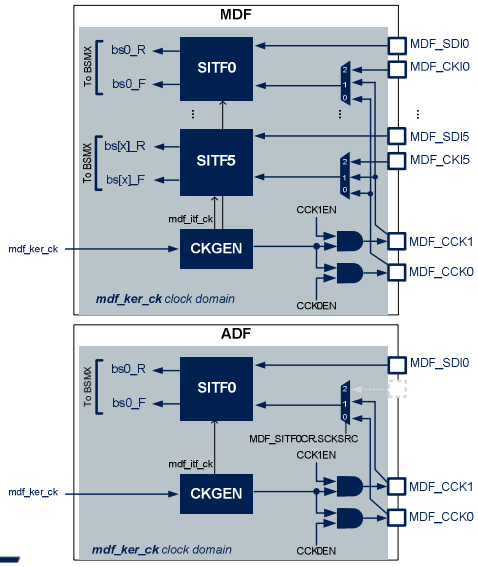
8

RCC provides a rich choice of clock sources for the MDF and ADF kernel clocks.
Note that the SAI_EXTCLK and pll1_p_ck sources are common to the SAIs kernel clocks.
The clock frequency for MSIK can be chosen from 16 frequencies.
For their internal processing, MDF and ADF use a processing clock which is obtained by dividing the kernel clock by the PROCDIV prescaler.
This processing clock is used for the serial interfaces, the ADC interfaces, the trigger functions, the digital filters, the short circuit detectors, and the out of limit detectors.
The MDF_CCK and ADF_CCK pins can be either output or input, depending of CCKDIR.
When the MDF_CCK clocks are generated by ADF or MDF, they are derived from the kernel clock divided by CCKDIV.

Serial Interface (SITF)



- ADF/MDF supports several serial modes:
  - SPI in SDR or DDR mode
  - Manchester mode
- For optimal flexibility, each SITF can use:
  - Its dedicated serial clock from MDF_CKIx pads
  - A common clock either generated by ADF/MDF or received from the MDF_CCK0 or 1 pads
- The maximum speed supported is 25 MHz
- ADF/MDF only needs a kernel clock twice the spedd of the serial link for audio applications (MASTER_LF mode)

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9

MDF supports two main serial modes:

-SPI in SDR or DDR mode

-Manchester mode

For greater flexibility, each serial interface of MDF can use:

-Its own serial clock input from a dedicated pad.

-A common clock either generated by MDF or received from MDF_CCK0 or 1 pads.

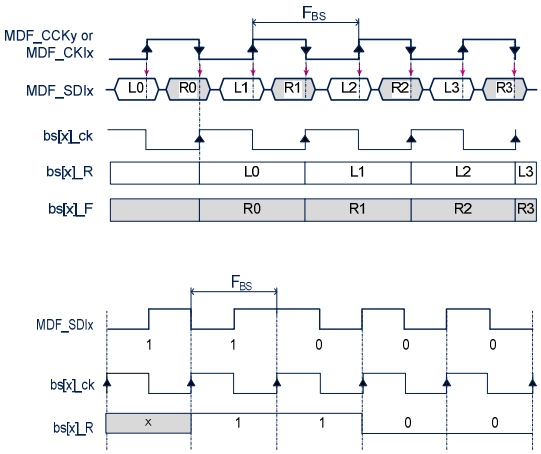
ADF does not support the serial interface clock input.

The maximum speed supported is 25 MHz.

MDF only needs a kernel clock twice the speed of the serial

link rate for audio applications.

Serial Interface (SITF)



- In SPI mode, each serial interface provides:
  - The data sampled with the rising edge of bitstream clock (bs[x]_R)
  - The data sampled with the falling edge of the bitstream clock (bs[x]_F)
- Manchester mode:
  - Does not require an external bitstream clock signal
  - Data is available on bs[x]_R
- It is possible to detect a clock absence in SPI or Manchester modes

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10

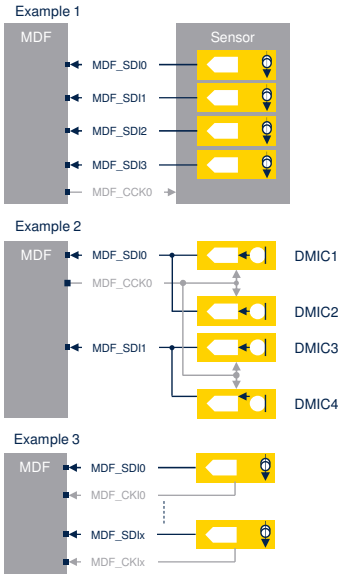
In SPI mode, the serial interfaces sample the incoming data on the falling and rising edges of the serial clock.
Each serial interface provides two data streams to the digital bitstream matrix:

- One representing the data sampled with the rising edge of the serial clock (bs[x]_R),
- One representing the data sampled with the falling edge of the serial clock (bs[x]_F),

In Manchester mode, the clock is recovered from the data stream. Valid data is available on the bs[x]_R output.

A clock absence detection allows the application to detect if there an absence of clock transition for a defined period of time.

Connection examples (SITF)



- Example 1
  - Several sensors with a common bitstream clock
  - The bitstream clock can be provided by the sensor or by MDF
- Example 2
  - Simple connection of 4 digital microphones
  - All microphones share the same clock
  - Each microphone pair shares the same data line
- Example 3
  - Independent sensors with independent clocks

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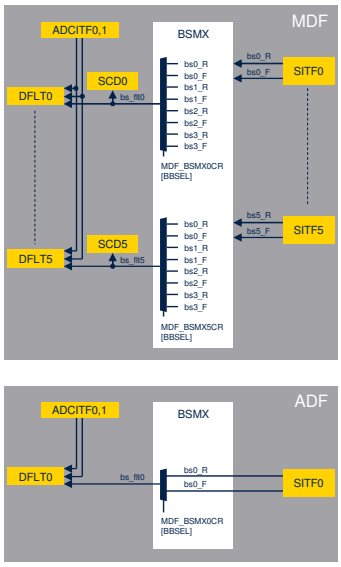
11

Example 1 shows the case where several sensors share the same bitstream clock.
MDF can either provide a common bitstream clock as in this figure, or receive the common bitstream clock from the external sensor.
The second example shows the connection of several digital microphones. Only three IO pads are required to connect 4 microphones.
Each microphone pair shares a single data line.
It is also possible to provide one microphone with a dedicated clock signal in order to keep that microphone active, while the others are in STANDBY.
Example 3 shows the case where independent sensors are connected to MDF. Each data line has its own dedicated clock.

Bitstream Matrix (BSMX)



- BSMX receives the bitstreams from all serial interfaces (SITFx)
- BSMX provides the selected input to the digital filters (DFLTx)
- For each filter path any bitstream input can be selected

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BSMX receives the bitstreams from all serial interfaces, and provides the selected input to the digital filters.
For each filter any bitstream input can be selected.
Each serial interface provides two streams: one with the data sampled on the falling edge and one with the data sampled on the rising edge.

MDF Only !

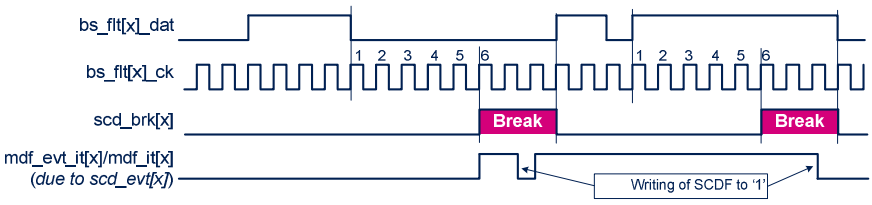
Short Circuit Detector (SCD)

Detects short or open conditions with a very fast response time

- The SCD detects if the incoming bitstream remains fixed to the minimum or maximum value for a certain amount of time with a very fast response time
- It can be used to detect short or open circuit errors (e.g. overcurrent or overvoltage)
- Interrupt and break events can be generated

Break events can be used to perform an emergency stop of the power stages

- An SCD block is available for each selected bitstream



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13

The SCD detects if the incoming bitstream remains fixed to the minimum or maximum value for a certain amount of time with a very fast response time.
The application can program the time during which the bitstream remains at the same value. If the bitstream remains fixed for an amount of time longer than the programmed value, then an interrupt and break events can be generated.
Break events can be used to perform an emergency stop of the power stages, by asserting the break signal.
SCD is used to detect short or open circuit errors (e.g. overcurrent or overvoltage).
An SCD block is available for each selected bitstream.
The figure shows an example where interrupts and break events are generated if the incoming bitstream remains fixed to the same value for more than 5 bitstream clock cycles.

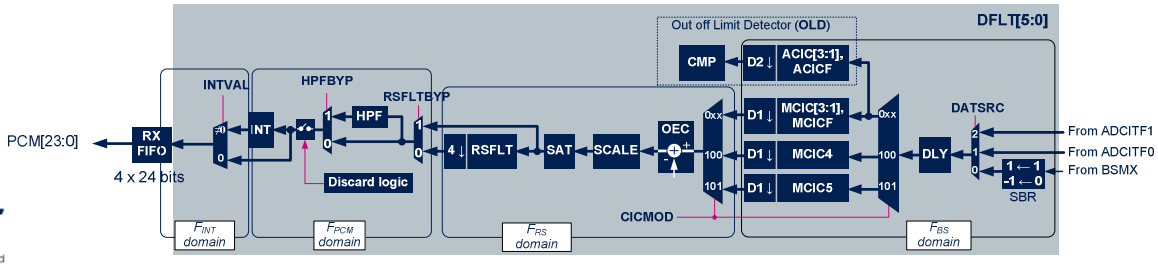
MDF Only !

Digital Filters (MDF DFLT)

Very flexible digital filter chain

MDF embeds 6 digital filters and includes the following parts:

- A delay block (DLY)
- Sinc and FastSinc filters (MCICs, MCICF)
- Offset error correction (OEC)
- Out off limit detector (OLD)
- Scale block (SCALE)
- Reshape filter (RSFLT)
- High-pass filter (HPF)
- Integrator block (INT)



14

The MCF digital filter embeds several blocks, offering great flexibility in filter configuration.
The most important parts are:

- The data source selector
- The delay block
- The main Cascaded-integrator-comb or CIC filter, often called MCIC
- The auxiliary CIC filter, often called the ACIC. This filter is included into a function called out off limit detector (OLD)
- An offset error correction
- A gain adjust, called SCALE
- A Reshape filter, called RSFLT
- A High-Pass filter, called HPF
- A discard function,
- An integrator, called INT.

The digital filter can be configured in multiple stage, so not all parts of the filter will work at the same frequency.
We call the Fbs frequency domain, the clock domain working on the bitstream clock.
The Frs domain, is the domain working at the frequency of the reshape filter, Fpcm is the sampling rate at the output of the reshape filter.
Finally, the Fint frequency domain is the final sampling rate of the samples stored in the RX-FIFO.
The final stage is storing the data processed by the filter in the RxFIFO.
Note also that the filter works with the processing clock.

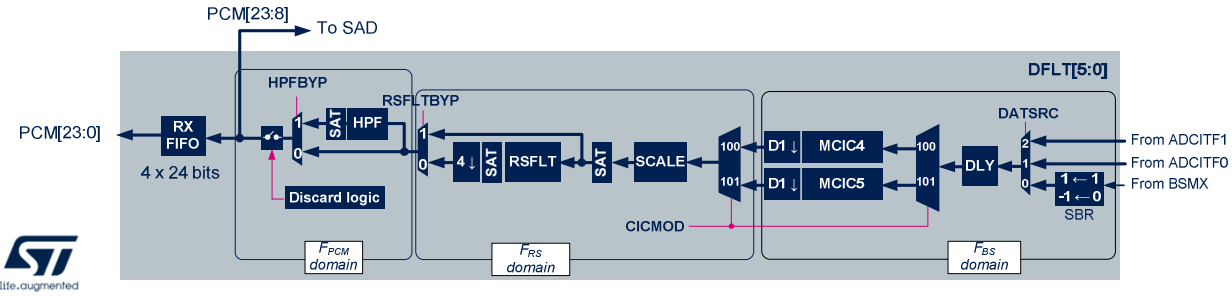
ADF Only !

Digital Filters (ADF DFLT)

Very flexible digital filter chain

ADF digital filter embed several blocks and includes the following parts:

- A delay block (DLY)
- Sinc4 and Sinc5 filters (MCICs)
- Scale block (SCALE)
- Reshape filter (RSFLT)
- High-pass filter (HPF)



15

ADF digital filter embed several blocks, giving a great flexibility on the filter configuration.
The most important parts are:

- The data source selector
- The delay block
- The main CIC filter, often named MCIC
- The auxiliary CIC filter, often named the ACIC. This filter is included into a function called out off limit detector (OLD)
- An offer error correction
- An gain adjust, called SCALE
- A Reshape filter, called RSFLT
- A High-Pass filter, called HPF
- A discard function,
- An integrator, called INT,

The digital filter can be configured in multi-stage, and thus all

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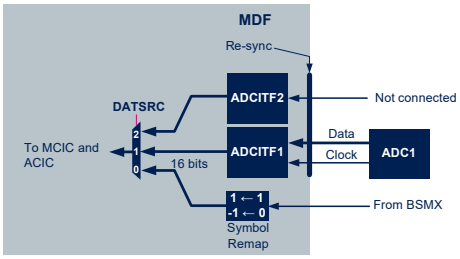
The Frs domain, is the domain working at the frequency of the reshape filter, the Fpcm is the sampling rate at the output of the reshape filter.
Finally, the Fint frequency domain is the final sampling rate of the samples stored into the RX-FIFO.
The final stage is storing the data processed by the filter into the RxFIFO.
Note as well that the filter is working with the processing clock.

Digital Filters (Data Source)

- The data sources can be:
  - The stream provided by BSMX
  - The samples provided by the ADC1
- The serial data coming from the BSMX are remapped into a series of ‘+1’, ‘-1’ symbols
- For MDF only, ADC1 provides parallel data with the sampling clock



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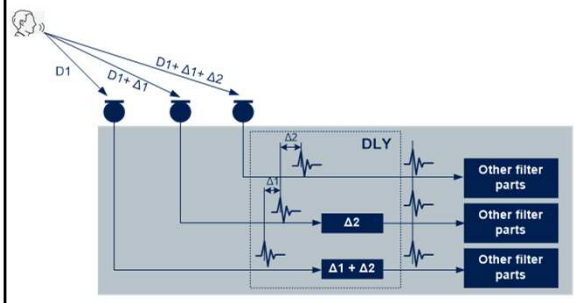
The samples processed by the digital filter can be provided either by BSMX, or by ADC1.
The BSMX provides a serial bitstream, and a symbol remapper is used to translate this bitstream into a series of plus ones and minus ones.
The samples from ADC1 are resynchronized by the ADC interface number one ADCITF1.
ADC1 provides the samples and the sampling clock.
ADF has no connection to the ADCs.

Digital Filters – Bitstream delay (DLY)

High resolution delay for beamforming



- The DLY block allows the delay between each bitstream to be finely tuned
- This feature is needed for audio beamforming with digital microphone arrays
  - *It allows to place the microphones close to each others, without any loss of performance or impact on processing*
- Main features:
  - Resolution: 1 bitstream clock period
  - Delay range: typically1 PCM period but can be greater (limit is given by the RX-FIFO depth)
  - Can be changed dynamically
  - Also works for the ADC interface

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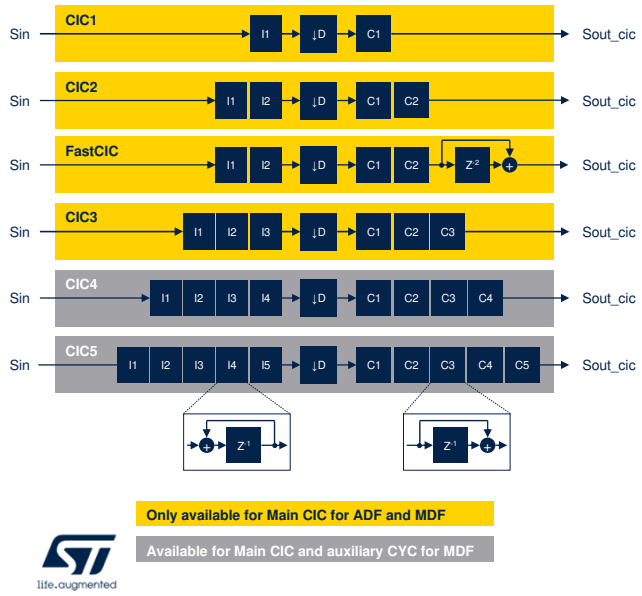
17

The delay block can be used to delay one or more data paths relative to others.
Delays are performed by skipping a certain number of samples before decimation.
Delay granularity depends on the bitstream clock rate or on the sample clock rate provided by the ADC.
This feature is useful for beamforming applications with digital microphones.
For example, in a typical speech capture at 16 kHz, with a decimation of 64, the resolution of the DLY block is about 976 nanoseconds, and sound travels about 0.33 mm in 976 nanoseconds. Increasing the decimation rate improves the resolution proportionally.
The delay range depends on the depth of the RX-FIFO, but generally it is not necessary to delay more than one PCM sample period using this block.

Other means should be used if longer delays are needed: either by software, or by using the discard block.

Digital Filters – CIC

Flexible CIC architecture



- CIC supports 3 configurations:
  - Main and Auxiliary filters:
    (Configuration dedicated to motor control)
    - The main filter can be CIC1 or 2 or 3 or FastCIC
    - The auxiliary filter can be CIC1 or 2 or 3 or FastCIC and is used by the Out off Limit Detector (OLD)
  - Main filter using a CIC4: (Configuration generally used for audio or metering)
    - The Out off Limit Detector cannot be used
  - Main filter using a CIC5: (Configuration generally used for audio or metering)
    - The Out off Limit Detector cannot be used
- ADF only supports CIC4 and CIC5

18

The abbreviation CIC stands for Cascaded Integrator-Comb filters.
MDF contains a single flexible CIC filter that can either be split into two filters (auxiliary and main filter), or used as a single main filter.
CIC supports 3 configurations:

- Main and Auxiliary filters. This configuration is dedicated to motor control.
  In this configuration, the main filter can be CIC1 or CIC2 or CIC3 or FastCIC.
  And the auxiliary filter can also be CIC1, 2 ,3 or FastCIC and is used for the Out off Limit Detector (OLD).
- The CIC filter can also be configured as single main filter in CIC4 or CIC5.
  Those two configurations are generally used for audio or metering applications.

In this case the Out off Limit Detector cannot be used Note that the ADF only supports CIC4 and CIC5 configurations.

Digital Filters – CIC

Large decimation range

The main and auxiliary CIC filters support output data size (DS_{CIC}) to up to **26 bits**

The output data size is a function of the input signal amplitude (DS_{IN}), the decimation ratio (D) and the CIC order (N)

$$DS_{CIC} = \left(\frac{N \cdot \ln(D)}{\ln(2)}\right) + DS_{IN}$$

$$G_{CIC} = D^N$$

Decimation ratio range for main CIC (1)

- Up to 512 for CIC1 and CIC2
- Up to 322 for CIC3
- Up to 76 for CIC4
- Up to 32 for CIC5

Decimation ratio range for auxiliary CIC (1)

- Decimation ratio up to 32

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(1) When the input data is taken from the serial interfaces (SITF)

19

The CIC data size is fixed to 26 bits.
The gain of a CIC filter depends on the decimation ratio (D) and on the order (N).
The same applies to the data size.
The decimation ratio and the order must be adjusted in order to avoid having a signal amplitude larger than 26 bits at the output of the CIC filter.
In order to satisfy this requirement, this slide indicates the maximum decimation according to the order of the filter. CIC n is a filter of order n.

CIC Transfer Function

CIC properties:

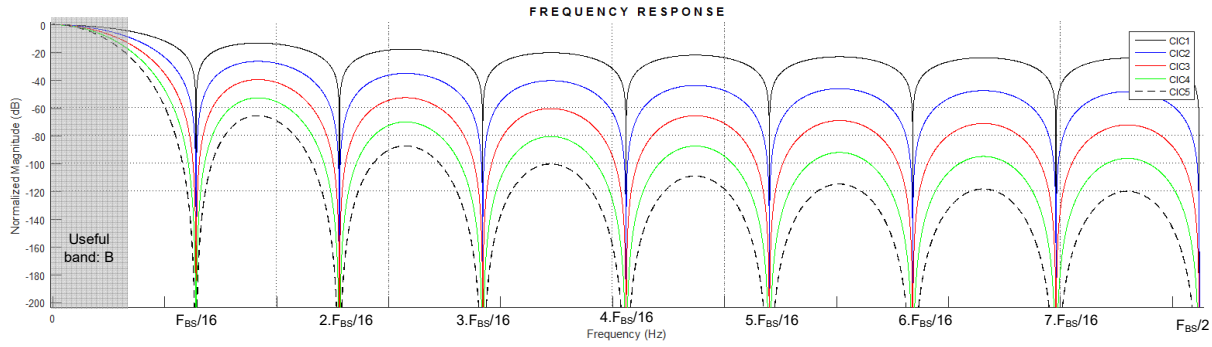
- Higher orders have stronger attenuation in the useful band (B)
- Zeroes are located at k.F_{BS} / dec

Figure hereafter given for dec =16

CIC transfer function: $H(z) = \left(\frac{1 - z^{-D}}{1 - z^{-1}}\right)^{N}$

Fast CIC transfer function (MDF only):

$$H(z) = \left(\frac{1 - z^{-D}}{1 - z^{-1}}\right)^{2} \cdot \left(1 + z^{-(2 \cdot D)}\right)$$

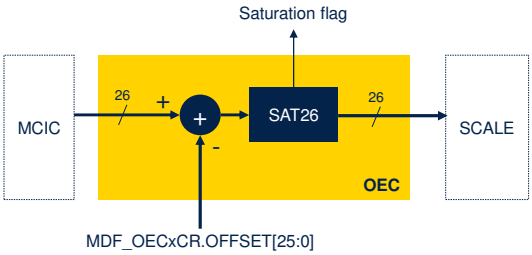


20

The CIC has a very simple filter structure, based on adders. Higher orders attenuate high frequency components more, but also introduce a droop in the useful band.
The amount of zeroes depends on the decimation ratio, and the zeroes are a multiple of Fbs/decimation.
The figure represents the frequency response of CIC filters assuming a decimation ratio of 16.

MDF Only !

Digital Filter – Offset Error Correction



- A constant value can be substracted from the signal provided by MCIC.
  - The value OFFSET[25:0] is subtracted from the incoming signal
- Possibility to dynamically change the OFFSET value
- A saturation block prevents wrap-around

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The offset error correction block can be used to cancel a DC component value from the signal provided by MCIC.

The value OFFSET[25:0] is subtracted from the incoming signal.

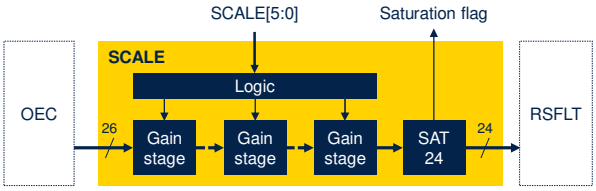
The application can change this OFFSET value dynamically if needed.

In addition, the saturation block prevents wrap-around issues.

A saturation flag is set in case of saturation to inform the application.

Digital Filter – SCALE

Wide gain range, with saturation block



- The SCALE block is needed to adapt the width to the filter configuration, and to the targeted application
- It must be adjusted to:
  - Limit the data width at the input of RSFLT to 22 bits, when RSFLT is enabled
  - Limit the data width to 24 bits in the other cases
- The gain steps are 3 dB (+/- 0.5 dB)
- The gain range is +72 dB (+12 bits) to -48 dB (-8 bits)
- The gain value can be changed on-the-fly
- After the gain stages, a saturation is done to 24 bits

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22

The SCALE block is needed in order to adapt the width to the filter configuration, and to the targeted application.
When the reshape filter is used, the signal at the output of SCALE block must not exceed 22 bits.
If the reshape filter is bypassed, then the signal at the output of the SCALE block can be up to 24 bits.
The gain steps are 3 dB plus or minus 0.5 dB.
The gain range is between +72 dB and -48 dB.
The gain value can be changed on-the-fly.
A saturation is done at the output of the SCALE block to limit the signal width to 24 bits.

Digital Filter – SCALE

- In order to optimize the signal quality, the gain must be properly adjusted
- The signal stored in the RX-FIFO must be as close as possible to 24 bits
- The signal provided to RSFLT must not exceed 22 bits

Maximum gain value versus configuration and decimation ratio:

Decimation ratios	SITF → CICx → RSFLT → (HPF)				SITF → CICx → (HPF)			
	CIC5	CIC4	CIC3	CIC2	CIC5	CIC4	CIC3	CIC2
8	33.6 dB	51.7 dB	69.7 dB	72.2 dB	45.7 dB	63.7 dB	72.2 dB	72.2 dB
12	18.1 dB	39.6 dB	60.2 dB		30.1 dB	51.7 dB		
16	3.5 dB	27.6 dB	51.7 dB		15.6 dB	39.6 dB	63.7 dB	
24	-12 dB	15.6 dB	42.1 dB	69.7 dB	0 dB	27.6 dB	54.2 dB	
32	-26.6 dB	3.5 dB	33.6 dB	63.7 dB	-14.5 dB	15.6 dB	45.7 dB	
48	-	-8.5 dB	24.1 dB	57.5 dB	-	3.5 dB	31.6 dB	69.7 dB
64	-	-20.6 dB	15.6 dB	51.7 dB	-	-8.5 dB	27.6 dB	63.7 dB
128	-	-	-2.5 dB	39.6 dB	-	-	9.5 dB	51.7 dB
256	-	-	-20.6 dB	27.6 dB	-	-	-8.5 dB	39.6 dB

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23

Ideally, for a full-scale input signal, the signal provided to the reshape filter should be as close as possible to 22 bits in size.

If the reshape filter is not used, then the signal size should be as close as possible to 24 bits.

Too little gain can degrade the signal to noise ratio. Too much gain can cause saturation.

The table shown in this slide, gives the optimum gain value for several filter configurations.

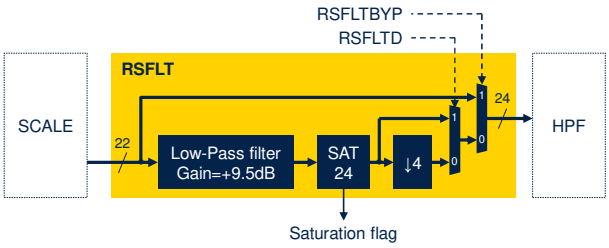
The left-hand side of the table is applicable when the reshape filter is active, the right-hand side is applicable when

the reshape filter is bypassed.

Also note that some specific applications may require a different gain setting.

Digital Filters – RSFLT

Improved in-band ripple, and image rejection



- RSFLT is a low-pass filter designed to improve image rejection, and in-band ripple
- RSFLT needs 24 cycles of mdf_proc_ck to output a sample
- RSFLT can be bypassed
- RSFLT performs a decimation by 4 after filtering
  - The decimation by 4 can be bypassed if necessary
- Saturation to 24 bits

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24

The reshape filter is a low-pass filter designed to improve image rejection, and in-band ripple.

The reshape filter performs a decimation by 4 after filtering,

The reshape filter can be completely bypassed, or it is possible to bypass the decimation by only 4.

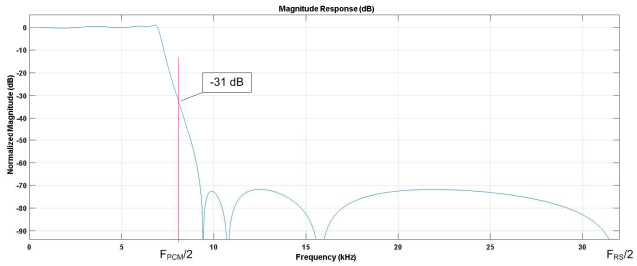
This feature can be helpful if additional processing must be performed by the software.

The reshape filter needs 24 cycles of mdf_proc_ck to output a sample.

A saturation to 24 bits is performed after the low-pass filter.

Digital Filters – RSFLT

Improved in-band ripple, and image rejection



- The cut-off frequency is fixed to 0.444 x FPCM
  - For FPCM = 16 kHz, the cut-off frequency is 7100 Hz
  - For FPCM = 48 kHz, the cut-off frequency is 21000 Hz
- The in-band ripple is +/- 0.4 dB
- The stop-band attenuation is 30 dB at FPCM / 2
- The filter gain is about +9.5 dB

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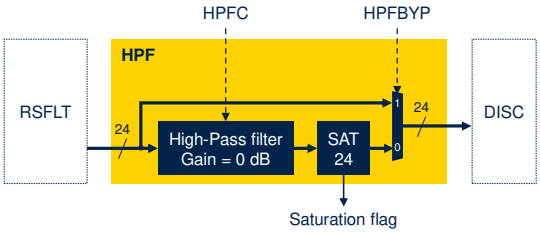
25

The following figure show the transfer function of the reshape filter alone, without the decimation by 4.
The cut-off frequency is fixed to 0.444 times Fpcm
The in-band ripple is plus or minus 0.4 dB.
The stop-band attenuation is 30 dB at Fpcm divided by 2.
The out-off band noise is attenuated by a bit more than 70 dB.
The filter gain is about +9.5 dB.

Digital Filters – HPF

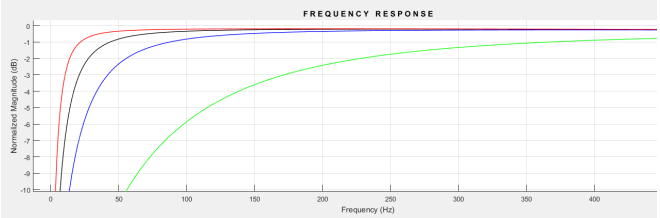
Adjustable high-pass filter



- HPF is a 1st order high-pass filter designed to cancel low-frequency components
  - Four selectable cut-off frequencies (see table):

Cut-off frequency selection	Cut-off frequency at F_{PCM} = 16 kHz	Cut-off frequency at F_{PCM} = 48 kHz
0.000625 x Fs	10 Hz	30 Hz
0.00125 x Fs	20 Hz	60 Hz
0.0025 x Fs	40 Hz	120 Hz
0.0095 x Fs	152 Hz	456 Hz

Red = 0.000625 x Fs, Black = 0.00125 x Fs, Blue = 0.0025 x Fs, Green = 0.0095 x Fs



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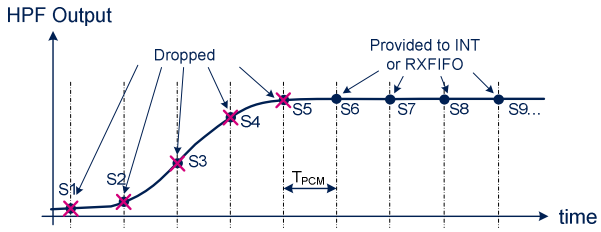
26

HPF is a 1st order high-pass filter designed to cancel low-frequency components which can be bypassed.
HPF has 4 selectable cut-off frequencies. The gain of the HPF is 0 dB.
The table shows some examples for audio capture at 16 and 48 kHz.
The HPF output is saturated to 24 bits.
The response frequency for the four cut-off frequencies is plotted in the chart.

Digital Filters – DISC

Possibility to remove the first received samples

- The discard block is used to cancel the first samples provided by the digital filter in order to mask the filter transients due to the impulse response or the settling time of the sensor
- The discard function can also be used to delay the acquisition (at the decimated rate)
- Up to 256 samples can be discarded



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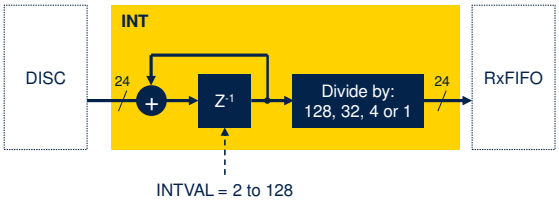
27

MDF offers the possibility to program the number of samples to be discarded after each restart.
The discard block allows the first samples provided by the digital filter to be discarded in order to mask the filter transients due to the impulse response or settling time of the sensor.
The discard function can also be used to delay the acquisition (at the decimated rate).
Up to 256 samples can be discarded.
In the example shown in the figure, the discard function is used to drop the first five samples provided by the digital filter (S1 to S5).
The first sample transferred to RXFIFO (or the INT block if enabled) is S6.

MDF Only!

Digital Filters – INT



- The integrator performs an additional decimation
- The integrator simply sums the data provided by the discard block
- The integration value can be any value between 2 and 128
- The integration output can be rescaled by 4, 32 or 128
- The integrator can be bypassed
- The integrator gain is given by:

$$G_{INT} = \frac{INTVAL + 1}{DIV}$$

  - Where DIV is the rescale factor:1, 4, 32 or 128

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28

The integrator performs an additional decimation.

The integrator simply sums the data provided by the discard block.

The integration value can be any value between 2 and 128.

The integration output can be rescaled by 4, 32 or 128.

The integrator gain depends on the integration value (INTVAL) and the rescale factor.
To bypass the integrator, initialize the INTVAL value to zero.

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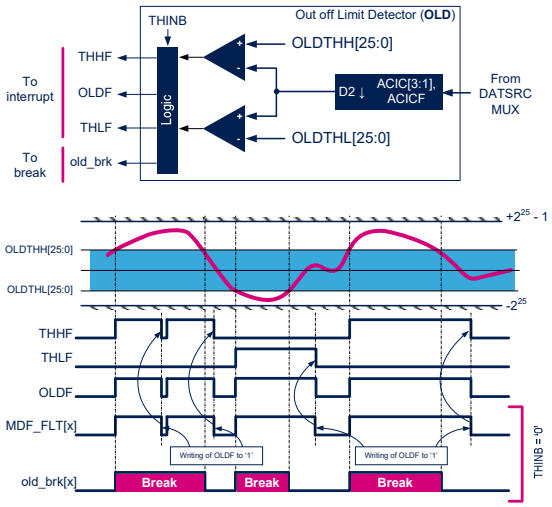
Digital Filters – OLD



- The Out off Limit Detector (OLD) contains:
  - Two digital comparators (Low and High thresholds)
  - An auxiliary CIC filter (ACIC) configurable in CIC1, CIC2, CIC3 or FastCIC
- OLD generates events if the signal is inside or outside the boundary defined by the thresholds
- The generated event can drive an interrupt or break signals
- ACIC characteristics:
  - CIC size is 26 bits
  - Decimation ratio up to 32

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29

The Out off limit detector triggers an event when a signal reaches or crosses given maximum and minimum threshold values.
The Out off Limit Detector (OLD) contains two digital comparators (Low and High thresholds).
These comparators are connected to the output of the auxiliary CIC, called ACIC.
This auxiliary CIC filter can be configured in CIC1, CIC2, CIC3 or FastCIC, with a decimation ratio up to 32.
The ACIC size is 26 bits, the data source of ACIC is the same as MCIC, and can be either a sensor connected to the serial interface, or ADC1.
The Out off Limit Detector generates events if the signal is inside or outside the boundary defined by the thresholds.
The generated event can drive an interrupt or break signals.

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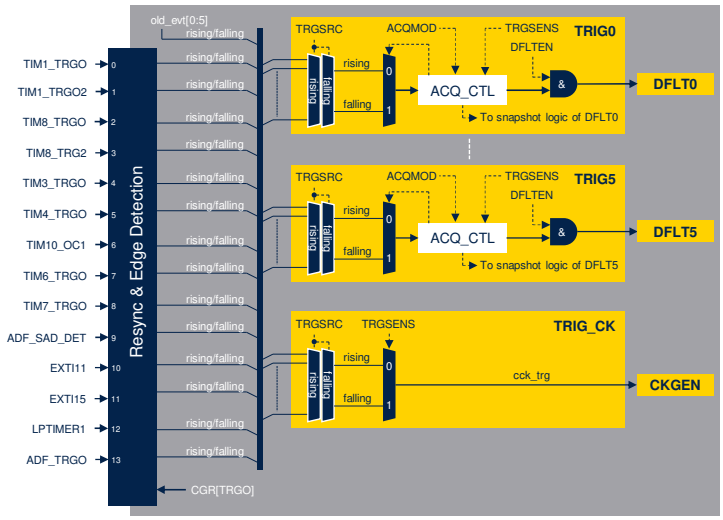
Triggers

Flexible trigger possibilities



- The trigger logic can be used to:
  - Start/Stop filter acquisition
  - Start the clock generator
- Several acquisition modes are available:
  - Asynchronous or synchronous trigger modes
  - Single-shot or Continuous acquisition modes
- Several trigger possibilities:
  - Edges (rising or falling)
  - Window
- Up to 16 trigger sources:
  - Timers, EXTI, ADF...
  - Out-off limit detector
  - Global trigger bit

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30

This slide describes the triggers present in MDF.
Each digital filter, and the clock generator have their own trigger block.
The trigger blocks are used to start and stop the acquisition of main digital filters, or to start the generation of the MDF_CCK[1:0] clocks.
Possible trigger sources are:

- 14 signals from other circuit blocks: various timers, LPTIMER1, ADF, EXTI. These trigger sources are common to all trigger blocks.
- 1 common internal signal: TRGO
- 1 dedicated internal signal: Each OLD block can trigger the main filter.

Several acquisition modes are available for the digital filters:

- Asynchronous or synchronous triggered modes
- Single-shot or Continuous acquisition modes.

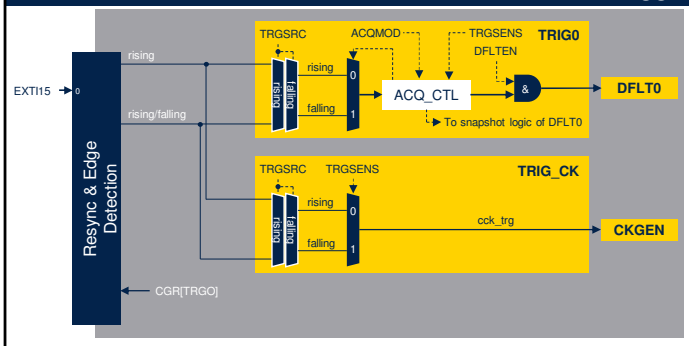
Several trigger possibilities:

- Edges (rising or falling)
- Window.

ADF Only!

Triggers

Flexible trigger possibilities



- The trigger logic can be used to:
  - Start/Stop the filter acquisition
  - Start the clock generator
- Several acquisition modes are available:
  - Asynchronous or synchronous trigger modes
  - Single-shot or Continuous acquisition modes
- Several trigger possibilities:
  - Edges (rising or falling)
  - Window
- 2 trigger sources:
  - EXTI[15]
  - Internal trigger bit

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31

This slide describes the triggers present in ADF.
The digital filter, and the clock generator have their own trigger block.
The trigger blocks are used to start and stop the acquisition of the digital filter, or to start the generation of the ADF_CCK[1:0] clocks.
The possible trigger sources are:

- EXTI[15] signal
- The internal signal: TRGO

Several acquisition modes are available for the digital filter:

- Asynchronous or synchronous triggered modes
- Single-shot or Continuous acquisition modes

Several trigger possibilities:

- Edges (rising or falling)
- Window.

DFLT States

DFLTxACTIVE	DFLTxRUN	DFLTx State
0	X	OFF
1	0	WAIT
1	1	RUN

- Each digital filter can be enabled by the DFLTxEN bit
- Two flags allows the application to check the filter state: DFLTACTIVE and DFLTRUN
- The DFLT state can be:
  - OFF: The filter is disabled
  - WAIT: The filter is enabled, and waiting for a trigger event
  - RUN: The filter is processing samples

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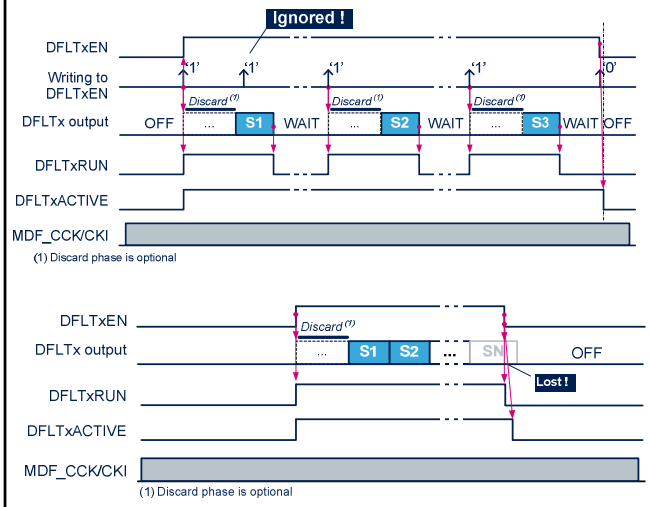
Each digital filter can be enabled by the DFLTxEN bit

The MDF_DFLTxCR register for filter x contains two flags that allow the application to check the current state of the filter: DFLTACTIVE and DFLTRUN.

The DFLT state can be:

- OFF: The filter is disabled
- WAIT: The filter is enabled, and waiting for a trigger event
- RUN: The filter is processing samples.

Triggers examples



- Asynchronous single-shot acquisition mode:
  - The acquisition of each filter is triggered when its enable bit is written to '1'
  - Only one sample is stored in the RX-FIFO when the filter is triggered
- Asynchronous continuous acquisition mode:
  - The acquisition of each filter is triggered by its enable bit
  - Consecutive samples are acquired as long as the enable bit is equal to '1'

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33

In asynchronous single-shot acquisition mode, the acquisition of each filter is triggered when its enable bit is written to '1'.

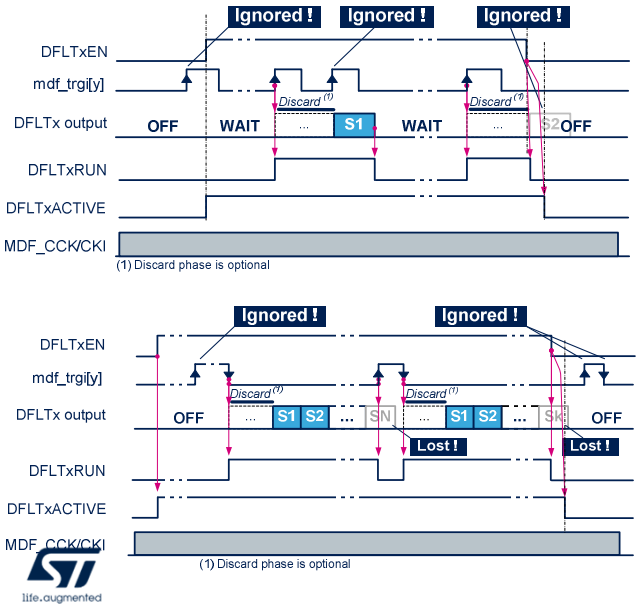
Whenever the digital filter is in WAIT state, and the DFLTxEN bit is written to '1', a sample is processed and stored in the RX-FIFO.

If the application sets DFLTxEN to '1' while a conversion is on-going, the write operation is ignored, as indicated in the upper timing diagram.

Consecutive samples are acquired as long as the enable bit is equal to one.

When DFLTxEN is deasserted, the current sample is lost, as indicated in the lower timing diagram.

Trigger examples



- Synchronous single-shot acquisition mode:
  - The acquisition of each filter is triggered by the selected trigger signal, with the selected sensitivity
  - Only one sample is stored into the RX-FIFO when the filter is triggered
- Window continuous acquisition mode:
  - The acquisition of each filter is triggered by the falling edge of the selected trigger, and stopped by the rising edge (or vice-versa)

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34

In synchronous single-shot acquisition mode, the acquisition of each filter is triggered by the selected trigger signal, with the selected sensitivity.

Whenever the digital filter is in WAIT state, and the trigger condition occurs, a sample is processed and stored in the RX-FIFO.

The DFLTxRUN flag informs the application whether the digital filter is ready to accept a new trigger event.

Trigger signals are ignored until the filter is in WAIT state, as indicated in the upper timing diagram.

In window continuous acquisition mode, the acquisition of each filter is triggered by the falling edge of the selected

trigger, and stopped by the rising edge (or vice-versa).
In the lower timing diagram, the falling edge of mdf_trgi[y] signal is used to trigger the acquisition and the rising edge to stop it.
When DFLTxEN is deasserted, the triggers are ignored.

MDF Only!

Trigger examples

- Starting several filters simultaneously:
  - Possibility to start the acquisition of several filters simultaneously by:
    - Selecting a common trigger source and sensitivity for several filters
    - Using TRGO bit
  - *Starting several filters simultaneously is very helpful for audio beam forming applications*

- Synchronous SnapShot Mode:
  - Possibility to capture the state of the CIC and INT filters using the trigger inputs
  - *This feature can be used to interpolate several intermediate values between two decimated samples*

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35

Several filters can be acquired simultaneously by selecting a common trigger source and sensitivity for several filters.

A simple option is to select TRGO as trigger source, and then set the TRGO bit to ‘1’.

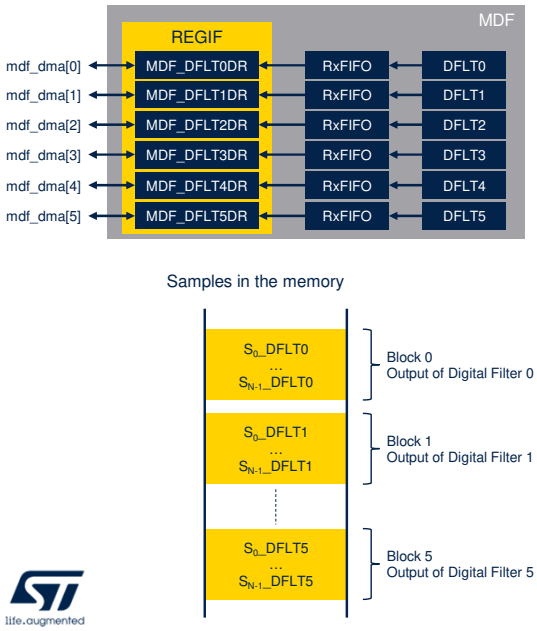
Any other common trigger signal can also be used.

Note that starting several filters simultaneously is needed for audio beam forming applications.

With Synchronous SnapShot Mode it is possible to capture the last valid sample, and the state of the CIC and INT filters using the trigger inputs.

This feature can be used to interpolate several intermediate values between two decimated samples.

Memory transfer



- Each FIFO has a depth of 4 words of 24 bits
- Independent transfer Mode:
  - Each RXFIFO stream can be independent
- Two thresholds are available:
  - FIFO not empty
  - FIFO Half full
- Each RXFIFO has its own DMA request or interrupt service
- This mode can be used for any kind of application.

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36

Each FIFO has a depth of 4 words of 24 bits.

MDF supports two modes of data transfer: independent and interleaved transfer modes.

In Independent transfer mode, RXFIFO streams are completely independent of each other.

The transfer of samples into memory can be triggered by two events:

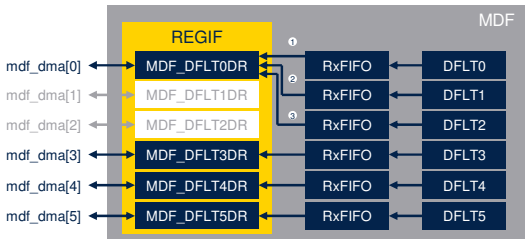
- When the FIFO is not empty, or
- When the FIFO is half full.

Each RXFIFO has its own DMA request or interrupt service.

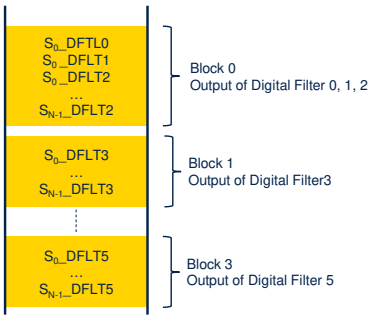
When the DMA is used, the application will find a block of data per FIFO in the memory, as shown in the figure.

This mode can be used for any kind of application.

Memory transfer



Samples inside the memory



- Interleaved transfer Mode:
  - Interleaved transfer mode allows a single DMA channel to be used ti get the samples of several filters
- Interleaved streams must be sampled at the same sample frequency
- The data is transferred to memory when all the RXFIFOs set in interleaved mode are not empty
- Only the interrupt or DMA request of RXFIFO[0] is used
- This mode can typically be used for audio applications
- It is possible to mix the interleaved and independent transfer modes

37

Interleaved transfer mode allows a single DMA channel to be used to get the samples of several filters.

Interleaved streams must be sampled at the same sample frequency.

In interleaved transfer mode, data is transferred to memory when all the RXFIFOs set in interleaved mode, are not empty.

Only the interrupt or DMA request of RXFIFO[0] is used.

This mode is typically used for audio applications.

As shown in the figure, digital filters 0 to 2 can be

programmed to work in interleaved transfer mode, while digital filters 3, 4 and 5 work in independent mode.

When the DMA is used, the data inside the memory block corresponding to the interleaved streams is also interleaved. See Block 0 in the figure.

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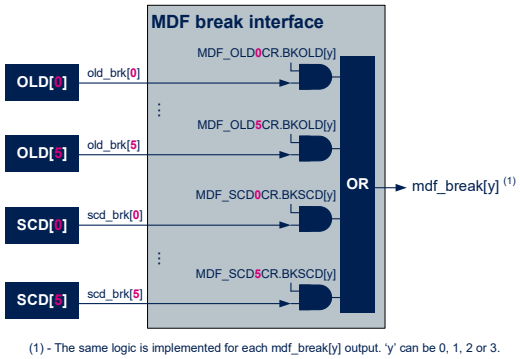
Break signal



(1) - The same logic is implemented for each mdf_break[y] output. 'y' can be 0, 1, 2 or 3.

- 4 break signals are available
- Only OLD and SCD can generate break events
- It is possible to mix within one break signal the break events coming from all OLD and SCD blocks

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38

Four break signals are available.

Timer break inputs put the timer's output signals in a safe user selectable configuration in the event of an abnormal condition.

Only Out-off Limit Detectors (or OLD) and Short Circuit Detectors (or SCD) can generate break events.

It is possible to mix within one break signal the break events coming from all OLD and SCD blocks. This is achieved by the OR gate in the figure.

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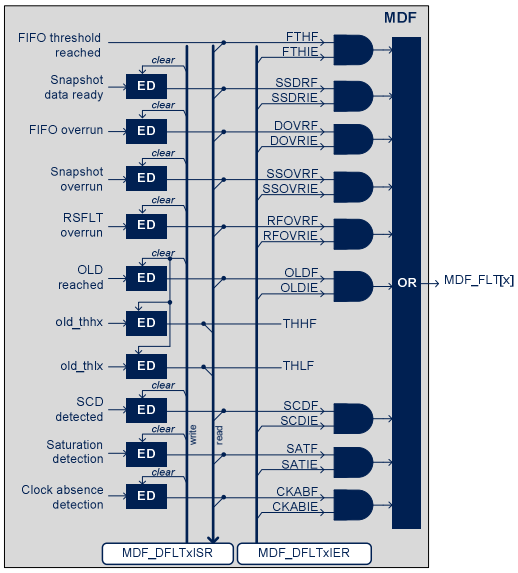
Interrupts



- Each digital filter path has its own interrupt vector
- Several events can generate an interrupt:
  - Alerts
    - RXFIFO, SnapShot or RSFLT overrun
    - Data Saturation
    - Out off Limit Detection
    - Short Circuit Detection
    - Clock absence detection
  - Data flow
    - RXFIFO level reached
    - SnapShot data ready

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39

This figure details the MDF interrupt management.

Each digital filter path has its own interrupt vector.

Alert events and data flow events can generate an interrupt.

The alert events are:

- RXFIFO, SnapShot or RSFLT overrun

- Data Saturation

- Out off Limit Detection

- Short Circuit Detection

- Clock absence detection

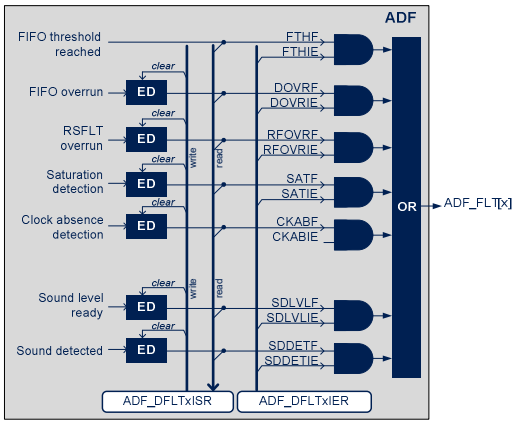
The data flow events are:

- RXFIFO level reached

- SnapShot data ready

ADF Only!

Interrupts



- Several events can generate an interrupt:
  - Alerts
    - RXFIFO or RSFLT overrun
    - Data Saturation
    - Clock absence detection
    - Sound level detected
    - Sound level value ready
  - Data flow
    - RXFIFO level reached

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40

This figure details the ADF interrupt management.

Alerts events and data flow events can generate an interrupt.

Alert events are:

- RXFIFO or RSFLT overrun

- Data Saturation

- Clock absence detection

- Sound level detected

- Sound level value ready

Data flow events is:

- RXFIFO level reached

MDF Low-Power Mode

Mode	Description
Run	Active
Low-power run	Active
Sleep	Active
Low-power sleep	Active
Stop 0/Stop 1	Active, if the kernel clock selected is an RC oscillator
Stop 2/Stop 3	Inactive
Standby	Inactive
Shutdown	Inactive

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41

MDF can be active in all modes, except in Stop 2, Stop 3, Standby and Shutdown modes.
In the stop modes, the content of MDF registers content are kept.
In Stop 0 and Stop 1 modes, MDF supports Low-power background autonomous mode or LPBAM.
In standby mode, MDF is powered down and must be reinitialized after exiting Standby mode.

ADF Low-Power Mode

Mode	Description
Run	Active
Low-power run	Active
Sleep	Active
Low-power sleep	Active
Stop 0/Stop 1/Stop 2	Active, if the kernel clock selected is an RC oscillator
Stop 3	Inactive
Standby	Inactive
Shutdown	Inactive

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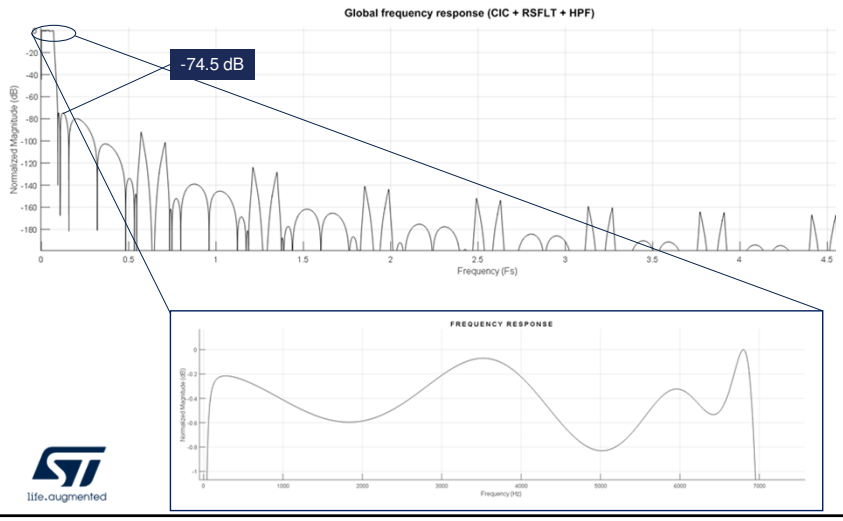
ADF can be active in all modes, except in Stop 3, Standby and Shutdown modes.
In stop mode, the ADF registers content is kept.
In the Stop 0, Stop 1 and Stop 2 modes, ADF supports the Low-power background autonomous mode or LPBAM.
In standby mode, ADF is powered down and must be reinitialized after exiting Standby mode.

Overall Frequency Response



The overall frequency response depends on several settings:

- CIC order
- CIC decimation
- Whether RSFLT is activated or not
- Whether HPF is activated or not
- Cut-off frequency of HPF
- Whether INT is activated or not
- ...

This plot is obtained with

- CIC5, with a decimation ratio of 16
- RSFLT activated with a decimation by 4
- HPF activated, HPFC = 1
- INT disabled
- Bitstream frequency 1.024 MHz
- PCM frequency 16 kHz

43

This upper figure shows the overall frequency response for a 16 kHz audio signal with a digital microphone working at 1.024 MHz.
The filter configuration is as follows:

- CIC order 5, with a decimation ratio of 16
- RSFLT enabled, with a decimation ratio of 4
- HPF enabled with a cut-off frequency of 40 Hz.

The lower figure shows the in-band ripple for a 16 kHz audio signal with a digital microphone working at 1.024 MHz.
The filter configuration is the following:

- CIC order 5, with a decimation ratio of 16
- RSFLT enabled, with a decimation ratio of 4
- HPF enable with a cut-off frequency of 20 Hz.

The resulting in-band ripple is ± 0.41 dB for CIC5. The -3 dB cut-off frequency is 7061 Hz.

Some numbers

- The table below gives the values of Signal-to-Noise ratio (SNR) and the dynamic range (DR) with and without an A-weighted window
  - These results are obtained with a 5th order Sigma Delta Modulator microphone model, delivering a signal with a DR of 126 dB @ 0 dBFS
  - The results are given using a CIC5, RSFLT, HPF, for several decimation ratios

MDF mode	Bitstream frequency	Decimation ratio	PCM frequency	SNR	DR	
Full feature or audio	0.768	12 x 4	16000	100	106	113
Full feature or audio	1.024	16 x 4	16000	115	120	123
Full feature or audio	1.536	24 x 4	16000	121	125	127
Full feature or audio	2.048	32 x 4	16000	123	125	126
Full feature or audio	3.072	16 x 4	48000	115	121	128
Full feature or audio	4.224	22 x 4	48000	120	124	130
UNIT	MHz		Hz	dB	dB	dBA

*Note that the DR of current digital microphones is between **90 to 105 dB**. The DR is measured by applying an input signal of -12 dBFS, and adding 12 dB to the measured SNR*

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44

The table on this slide provides measurements of the digital filters implemented in MDF and ADF.
These results are obtained with a 5th order Sigma Delta Modulator microphone model, delivering a signal having a DR of 126 dB at 0 dB full scale.
The configuration of the filter is as follows:
- CIC order 5
- Reshape filter
- High-pass filter.

Values of signal-to-noise ratio and dynamic range are provided for various decimation ratios.

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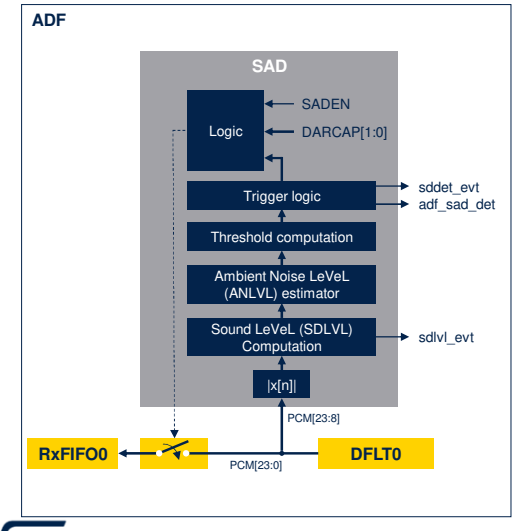
Sound Activity Detection (SAD)

Can be used to detect a sound or voice activity



- SAD is included in ADF
- SAD 'observes' the signal provided by digital filter 0 (DFLT0)
- When enabled, SAD continuously computes the sound and ambient noise levels
- SAD can work in several detection modes:
  - In sound detector mode, SAD can detect:
    - When the sound level reaches a defined level or,
    - When the ambient noise reaches a defined level,
  - In voice detection mode, SAD can detect when the sound level is larger than a threshold referenced to the ambient noise level

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45

SAD stands for Sound Activity Detection.

The SAD function is offered by ADF.

SAD can be used to observe the signal provided by the digital filter 0, it is intended to be used for audio applications.

When enabled SAD continuously computes the sound and ambient noise levels.

SAD can work in two different modes:

In sound detector mode, SAD can detect when the sound level or the ambient noise reaches a defined threshold.

In voice activity detector mode, SAD can detect when the sound level is larger than a threshold referenced to the ambient noise level.

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Sound Activity Detection (SAD)

SAD can be in 3 different states:

- The 'LEARN' state
  - To perform a first estimation of the ambient noise level
- The ‘MONITOR’ state
  - SAD is waiting for a trigger event
  - SAD continuously computes the sound level and updates the ambient noise value
- The ‘DETECT’ state
  - SAD detected an event
  - SAD continuously computes the sound level and updates the ambient noise value

SAD offers 3 modes of data capture:

- Samples are always transferred in memory
- Samples are never transferred in memory
- Samples are stored in memory when SAD is in DETECT state

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46

When enabled, SAD goes into the 'LEARN' state. During this state SAD performs a first estimation of the ambient noise level, using successive values of the sound level.

When a first estimation of the ambient noise is made, SAD transitions to the MONITOR state. In this state SAD waits for a trigger event, and continuously computes the sound level and updates the ambient noise value.

When SAD triggers, the state changes to DETECT. In this state SAD continuously checks that the DETECT condition is still true. Even in the DETECT state, SAD continuously computes the sound level and updates the ambient noise value.

To improve flexibility, SAD offers 3 options for controlling the transfer of the observed signal data to memory:

- Samples are always transferred in memory
- Samples are never transferred in memory
- Samples are stored in memory when SAD is in the DETECT state.

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Sound Activity Detection (SAD)

- The Sound level (SDLVL) is estimated by averaging the absolute values of the received samples
- The Ambient noise level (ANLVL) is estimated in two different ways:
  - By averaging SDLVL when SAD is in the LEARN state
  - By updating smoothly the ambient noise when SAD is not in the LEARN state
    - ANLVL is updated using the current SDLVL value when this sound level is considered as ambient noise

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47

Once enabled, SAD continuously computes the sound level value.

The sound level represents the average of the absolute value of an number of PCM samples given by FRSIZE[2:0].

The ambient noise level (ANLVL) is computed when the SAD working mode is binary 00 or 10.

The Ambient noise level (ANLVL) is estimated in two different ways:

-By averaging SDLVL when SAD is in the LEARN state

-By updating smoothly the ambient noise when SAD is not in

the LEARN state.

ANLVL is updated using the current SDLVL value when this sound level is considered as ambient noise.

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Voice Activity detection mode

Very high level of flexibility

Several parameters can be adjusted via registers to meet the needs of the application:

- **FRSIZE**: Defines the number of samples (frame) used to compute SDLVL.
  Can be: 8, 16, 32, 64, 128, 256 or 512 samples
- **LFRNB**: Defines the number of frames used for the learning phase.
  Can be: 2, 4 , 8, 16 or 32 frames
- **ANSLP**: Defines the slope of the noise estimator
  Typical value is +4.2 dB/s and -17.1 dB/s
- **HYSTEN**: Enable the hysteresis function
- **ANMIN**: In Voice Activity mode, defines the minimum ambient noise (sensitivity). For Sound Activity mode, defines the reference threshold.
- **SNTHR**: Defines the trigger level.
  Can be: 3.5, 6, 9.5, 12, 15.6, 18, 21.6, 24.1, 27.6 or 30.1 dB with respect to the reference threshold.
- **HGOVR**: Defines the minimum time that SAD remains in DETECT mode, between 2 trigger conditions.
  Can be 4, 8, 16, 32, 64, 128, 256 or 512 frames

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48

SAD is very flexible, and several parameters can be adjusted to meet the needs of the application:

- The frame size, called FRSIZE. It defines the number of samples used to compute SDLVL.
- The number of learning frames, called LFRNB, defines the number of frames used to compute the initial ambient noise level.
- The ambient noise level slope, called ANSLP, defines the slope of the ambient noise estimator during the MONITOR and DETECT states.

- The trigger level adjust, called SNTHR, defines the trigger level. This trigger level is used differently depending on the detection mode selected.
- The hangover, called HGOVR, defines the minimum time the SAD remains in DETECT mode, between 2 trigger conditions.
- The sensitivity or level, called ANMIN. In Voice Activity detection mode, it defines the minimum ambient noise (sensitivity). In Sound Activity detection mode, it is used to adjust the threshold.
- It is also possible to have hysteresis on the threshold value with the HYSTEN parameter.

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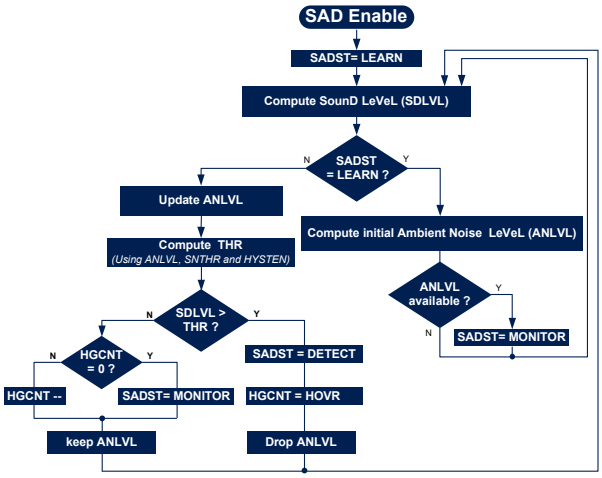
Voice Activity detection mode



- Main principle:
  - During the LEARN phase SAD computes a first estimate of the ambient noise
- SAD triggers if:
- Note that ANLVL cannot be lower than the ANMIN

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49

In voice activity detection mode, when enabled, SAD computes a first estimate of the ambient noise level.

The ambient noise level is estimated using the sound level values (SDLVL).

The duration of this LEARN phase is given by the parameter LFNBR.

When an estimate of the ambient noise level is available, SAD goes to the MONITOR state.

In MONITOR and DETECT mode, every time a new sound level value is available, SAD updates the ambient noise level and computes the threshold level to be compared to this new

sound level value.

If the sound level is larger than the threshold then SAD goes to the DETECT state.

When the SAD goes to the DETECT state, an interrupt can be generated, and the signal adf_sad_det goes to ‘1’.

SAD goes back to the MONITOR state, if the successive sound level values are lower than the threshold. HGOVR is used to adjust the number of successive values.

When SAD goes back the MONITOR state, an interrupt can also be generated.

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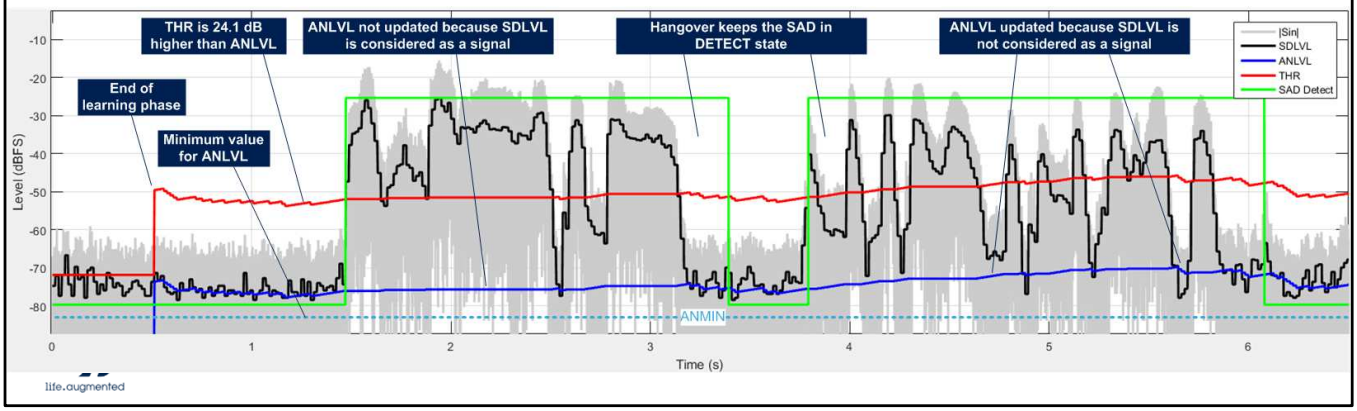
Voice Activity detection mode

Example of SAD used in Voice Activity Detection mode:

- At the end of the LEARN state, THR and ANLVL are updated, and SAT monitors the input signal
- ANLVL is continuously updated (i.e. THR as well)
- When SDLVL is higher than THR, SAD triggers
- The hangover function allows SAD to stay in the DETECT state for a given amount of time



Here is an example of SAD used in Voice Activity Detection mode:

At the end of the LEARN state THR and ANLVL are updated, and SAD monitors the input signal.

In black, we can see the successive sound level values.

ANLVL, in dark blue, is continuously updated, and the threshold level, the red signal, follows the ambient noise level exactly, with a gain given by SNTHR, in this example set to 24.1 dB.

When the sound level is higher than THR, SAD triggers. The green signal shows the SAD detection: when the signal is high it means that SAD triggers.

We can also observe that the ambient noise level is not updated when the sound level is higher than the threshold

level. But the ambient noise level is updated when the sound level is lower than the threshold.

The hangover function allows SAD to stay in the DETECT state for a given number of frames.

Note as well that the light blue signal, ANMIN defines the minimum allowed value for ANMIN, so it is a kind of sensitivity adjust, insuring that THR will not be lower than a given value.

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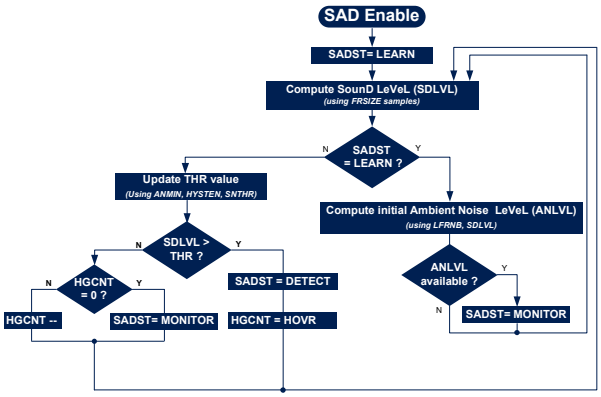
Sound Activity detection mode 1



- ANMIN defines the reference threshold, and SNTHR is used to define the trigger level (THR)
- SAD triggers if:
- THR is compared to the current SDLVL

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51

In Sound Activity Detection mode 1, SAD triggers when an absolute value of the sound level is reached.

In this mode, the ANMIN field defines the reference threshold, and SNTHR is used to define the trigger level (THR).

The formula shows the trigger condition.

In this mode the ambient noise level is not used, but SAD still goes to the LEARN phase when enabled.

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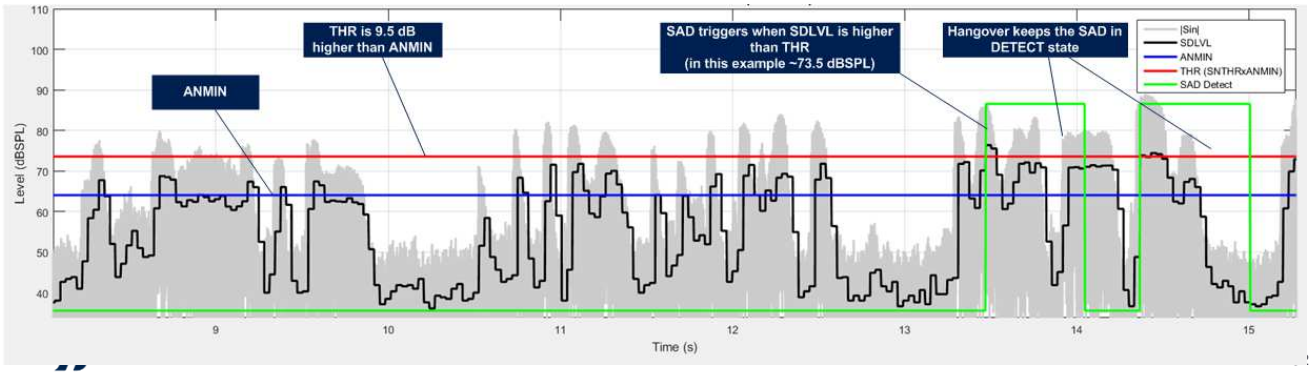
Sound Activity detection mode 1

Example of SAD used in Sound Activity Detection mode 1:

- SCALE is adjusted so that 600 LSB represents a signal of 73.5 dBSPL.
- ANMIN is set to 200 and SNTHR to 9.5 dB, which means that THR = 200 x 10^(9.5/20) = 600 LSB
- When SDLVL is higher than THR, SAD triggers,
- The hangover function allows SAD to stay in the DETECT state for a given amount of time



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Here is an example of SAD used in Sound Activity Detection mode 1.

In black, we can see the successive sound level values computed by SAD.

The threshold level THR, is computed from the value of ANMIN, multiplied by the gain factor selected with SNTHR.

When the sound level is higher than THR, SAD triggers. The green signal shows the SAD detection: when the signal is high it means that SAD triggers.

The hangover function allows SAD to stay in the DETECT state for a given number of frames.

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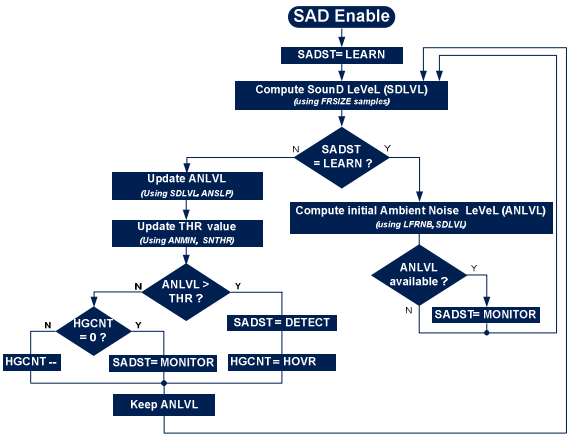
Sound Activity detection mode 2



- Sound Activity Detection mode 2
- SAD triggers if:

- THR is compared to the current ANLVL

- *Note that if SNTHR(dB) = 12 dB then THR = ANMIN*

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In Sound Activity Detection mode 2, SAD triggers on an absolute value of the ambient noise level.

In this mode, the ANMIN field defines the reference threshold.

This reference threshold level is compared to the ambient noise, multiplied by the gain selected by SNTHR.

The formula shows the trigger condition.

Note that if SNTHR(dB) = 12 dB then THR = ANMIN, because 10 power of (SNTHR divided by 20) is approximately equal to four.

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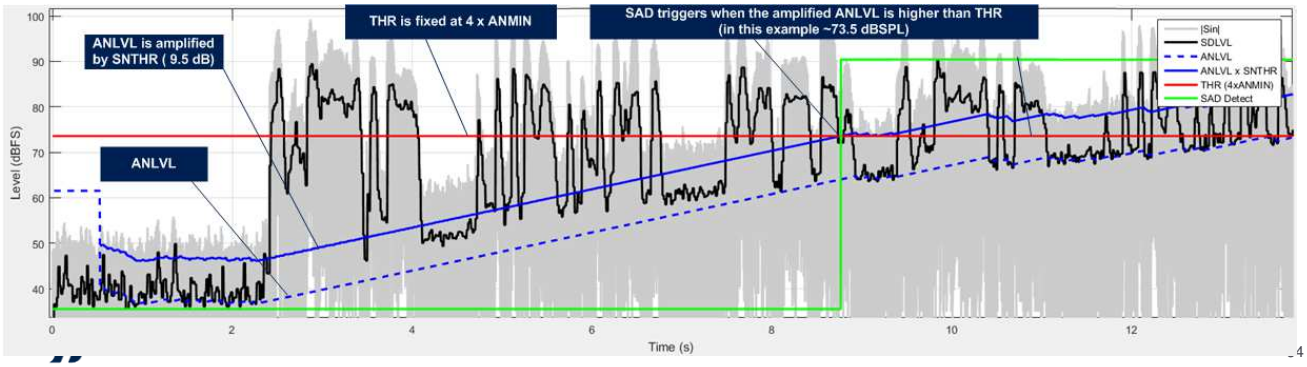
Sound Activity detection mode 2

Example of SAD used in Sound Activity Detection mode 2:

- SCALE is adjusted so that 600 LSB represents a signal of 73.5 dBSPL
- ANMIN is set to 150, which means that THR = 150 x 4 = 600 LSB
- The estimated ambient noise level is amplified by SNTHR
- When the amplified SNTHR is higher than THR, SAD triggers



Here is an example of SAD used in Sound Activity Detection mode 2:

In black, we can see the successive sound level values computed by SAD.

The threshold level THR, is computed from the value of ANMIN, multiplied by 4.

The estimated ambient noise is multiplied by the gain factor selected with SNTHR, before being compared to the threshold.

When this amplified ambient noise level is higher than the threshold, THR, SAD triggers.

The green signal shows the SAD detection: when the signal is high it means that SAD has triggered.

Thank you

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The peripherals listed below influence the behavior of MDF and ADF.
Please refer to the corresponding presentations for more information:
-RCC (MDF/ADF clock control, MDF/ADF enable/reset)
-Interrupts (MDF/ADF interrupt mapping)
-DMA (MDF/ADF output data transfer)
-GPIO (MDF/ADF input/output pins, triggers)
-Timers (MDF/ADF trigger, break signal)
-Peripherals interconnect matrix (MDF/ADF interconnection).