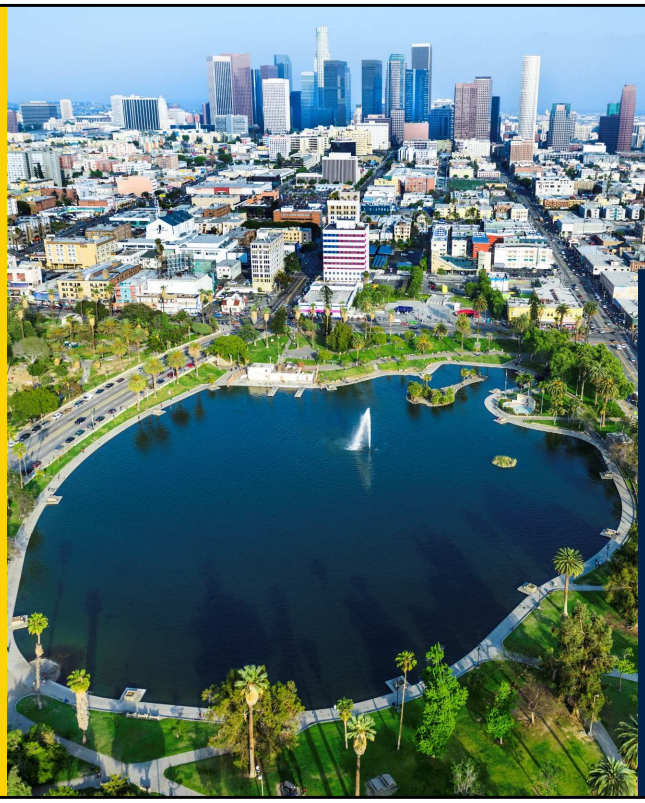
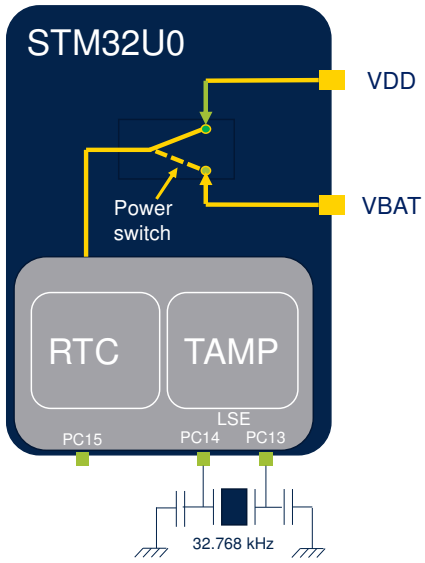


STM32U0 – RTC
Real-time clock

Hello, and welcome to this presentation of the STM32 Real-Time Clock. It covers the main features of this peripheral, which is used to provide a very accurate time base.

Overview



- The RTC provides an ultra-low-power hardware calendar with alarms, in all low-power modes
- It belongs to the Battery Backup Domain, so it is kept functional when the main supply is off and VBAT is present
- The TAMP peripheral features the backup registers and tamper detection

Application benefits

- Ultra-low power: 300 nA at 1.8 V
- Hardware BCD calendar to reduce software load

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The RTC peripheral features an ultra-low power calendar with alarms, which run in all low-power modes.
Additionally, when it is clocked by the low-speed external oscillator (LSE) at 32.768 kHz, the RTC is functional even when the main supply is off and when the VBAT domain is supplied by a backup battery.
The RTC consumes only 300 nA at 1.8 V, including the LSE power consumption.
The hardware calendar is provided in binary-coded decimal (BCD) format to reduce software load, particularly when the date and time must be displayed.
Backup registers and tamper detection belong to the TAMP peripheral.

Key features

- Sub-seconds, seconds, minutes, hours, week, day, date, month, year in BCD format
- Binary mode with 32-bit free-running counter
  - Mixed mode (Binary/BCD) support
- “On the fly” programmable daylight savings compensation
- Two programmable alarms with wakeup interrupt function
- A periodic event with programmable resolution, triggering wakeup interrupt
- A reference clock source (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit to achieve 0.95 ppm accuracy
- Timestamp feature which can be used to save the calendar content with sub-second precision (one event)

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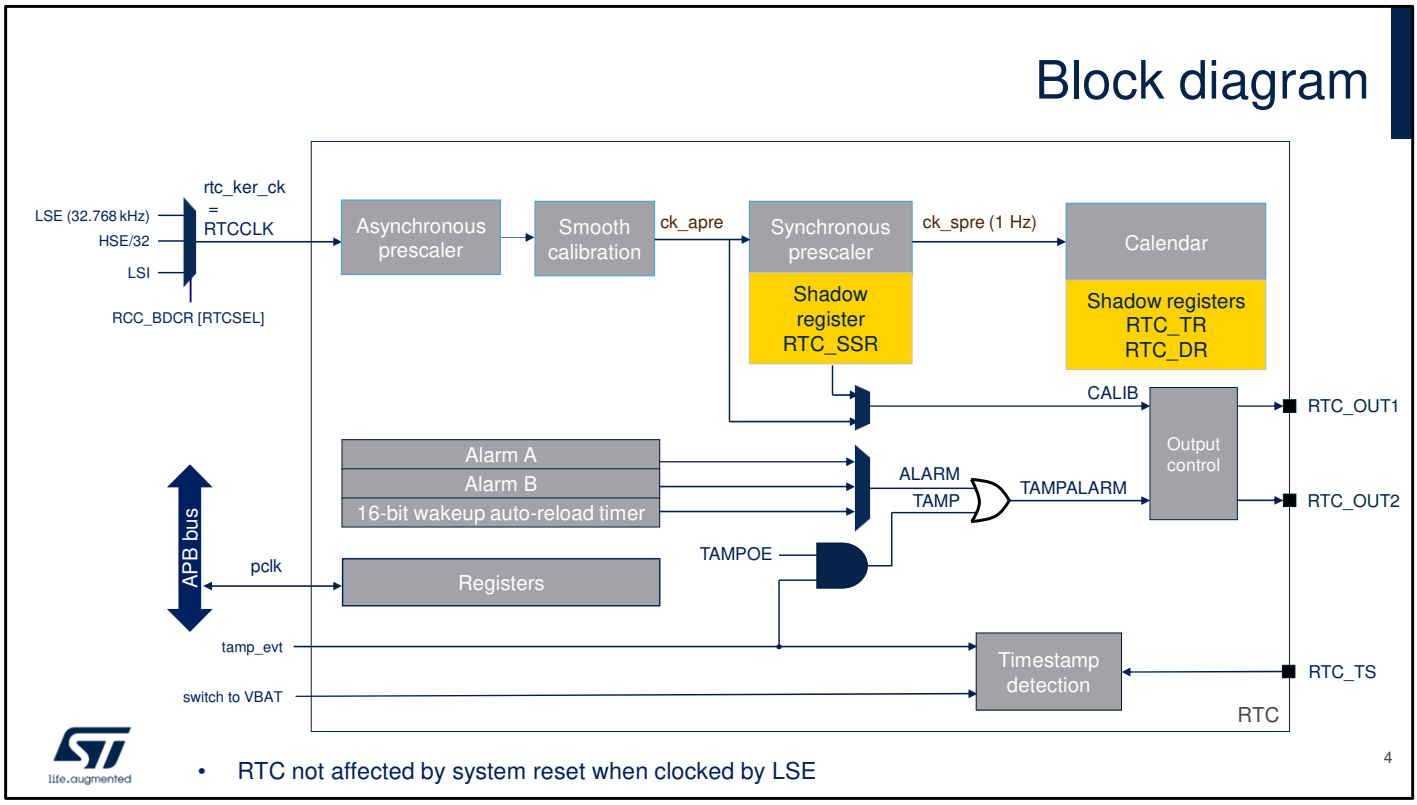
This slide lists the main features of the Real Time Clock module.
Seconds, minutes, hours, week, day, date, month, and year, are provided in binary-coded decimal format.
Sub-seconds field is provided in binary format.
It is also possible to select full binary mode, in this case the RTC is a 32-bit free-running counter.
If the mixed mode is selected, both 32-bit counter and calendar in BCD format can be used.
The other features are:

- Adding or removing one hour on the fly to the calendar, to manage daylight savings
- Two programmable alarms, which can wake up the microprocessor from all low-power modes
- An embedded auto-reload timer, which can be used to generate a periodic flag or interrupt with wakeup

capability, the resolution of this timer is programmable. The calendar can be calibrated thanks to a reference clock source which is the mains at 50 or 60 Hz.
A digital calibration circuit allows compensation of the crystal accuracy, with 0.95 ppm resolution.
A timestamp function is used to save calendar contents in timestamp registers, depending on an external event.



Here is the RTC block diagram.
The RTC has two clock sources: the RTC clock (RTCCLK) is used for the RTC timer counter, and the APB clock is used for RTC register read and write accesses.
The RTC clock can use either the high-speed external oscillator (HSE), divided by 32, the low-speed external oscillator (LSE), or the low-speed internal oscillator (LSI).
To be functional in Stop or Standby mode, the RTC clock must use the LSE or LSI. To be functional in Shutdown or VBAT mode, the RTC clock must use the LSE.
The RTC clock is first divided by a 7-bit programmable asynchronous prescaler, which provides the ck_apre clock.
Most of the RTC is clocked at the ck_apre frequency,
So, in order to reduce power consumption, it is recommended to set a high asynchronous division value.
The default value is 128.

Then, a 15-bit programmable synchronous prescaler provides the ck_spre clock.
The ck_spre clock must be 1 Hz in order to update the time and date BCD registers in 1-second increments.
The sub-second register resolution is defined by the ck_apre frequency. By default, it is 256 Hz when the RTC clock frequency is 32768 Hz.
The SSR register resolution is increased by reducing the asynchronous prescaler value.
The asynchronous prescaler can also be bypassed; in this case the sub-second register resolution is defined by the RTC clock frequency.
The RTC has 2 outputs that can provide the alarm flags, the wakeup timer flag, a calibration output from the prescalers, and also a tamper detection event.
In this figure, the shadow registers belong to the APB clock domain. This is explained later in this presentation.

RTC register write protection

Secure RTC initialization

- The RTC registers are write-protected to avoid possible parasitic write accesses
  - Disable Backup Domain (DBP) bit must be set in the Power Controller control register (PWR_CR) to enable RTC write access
  - A Key must be written in RTC write protection register (RTC_WPR) register
- Specific software sequence to enter RTC initialization mode
  - Used for calendar registers and prescaler initialization

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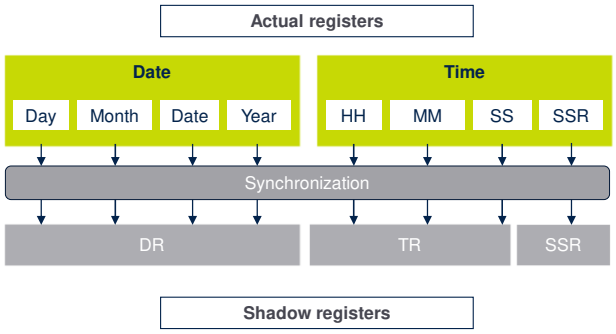
The RTC is initialized using a safe method.
The RTC registers are write-protected to avoid any possible parasitic write accesses.
First, the Disable Backup Domain Protection (DBP) bit must be set in the Power Controller control register in order to enable RTC write accesses.
Then, a specific sequence must be written in the RTC write protection register.
Initialization mode must be entered to change the clock prescaler values or the calendar value.

RTC calendar

Active in all low-power modes, VBAT and reset

- Initialization done through shadow registers: Time and Date registers



- Reading the calendar:
  - BYPSHAD = 0: Read shadow registers
    - Delay up to 1 RTCCLK cycles to update shadow registers when exiting Stop/Standby/Shutdown modes
    - Reading either RTC_SSR or RTC_TR locks the values in the higher-order calendar shadow registers until RTC_DR is read
  - BYPSHAD = 1: Bypass shadow registers
    - Calendar read directly accesses the calendar counters
    - Software must read all calendar registers twice and compare the results to ensure that the data are coherent and correct

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The RTC calendar keeps running in all low-power modes, in VBAT mode, and during reset.
Initialization of the Time and Date registers is performed via their shadow registers, which are in the APB clock domain.
The Sub-second register cannot be initialized.
The calendar Sub-second, Time, and Date registers content can be read in two different modes.
- When the Bypass Shadow Registers control bit is cleared, the shadow registers are read. The advantage of this mode is that it guarantees that all three registers are consistent. Reading either RTC_SSR or RTC_TR locks the values in the higher-order calendar shadow registers until RTC_DR is read.
The disadvantage of this mode is that when exiting Stop, Standby or Shutdown mode, the software must wait for a

synchronization delay to ensure that the shadow registers are updated with the last calendar register values. This synchronization delay can be up to one RTC clock period.
-When the Bypass Shadow Registers control bit is set, the actual calendar registers are read directly. The advantage of this mode is that there is no need to wait for the synchronization delay. The disadvantage is that the read values can be false or not consistent due to synchronization issues, so they must be read twice and compared with previous read values to ensure they are correct and coherent.

RTC format: BCD, binary or mixed

Flexible format for software load optimization

- In BCD mode, the SSR (Sub-second) register is 15-bit depth
  - Time and date registers are used
- In binary mode, the SSR is extended to 32-bit length and is free running
  - The time and date calendar BCD registers are not functional
- In mixed mode, the SSR is extended to 32-bit length and is free running
  - The time and date calendar BCD registers are also available
  - The bits BCDU[2:0] are used to define when the calendar is incremented by 1 second, using the SSR least significant bits
- Alarms and timestamp registers exist in all formats

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The RTC can be configured in three different formats: BCD, binary and mixed mode.
In BCD format, the date and time registers can be read as explained in the previous slide and can be initialized.
If a calendar in BCD format is not needed, the application can configure the RTC in binary format. In this case the SSR register is extended to 32-bit and is free running, it cannot be initialized. This counter clock is the RTC clock divided by the asynchronous prescaler, like in BCD format. Alarms and timestamps are also configured in 32-bit binary mode.
It is also possible to configure the RTC in mixed mode, so that 32-bit SSR free running register, time and date registers are also available. In this case the second field of the calendar is incremented each time the least significant bits of SSR reaches 0, where the number of SSR LSB is

configured in BCD update field. Alarms and timestamps are also configured in mixed mode.

RTC calendar features

- Daylight savings is managed by automatic addition or subtraction of 1 hour
- Calendar synchronization up to 1 second by adding/subtracting an offset with the sub-second resolution
  - Allows synchronization with remote clock
- Reference clock detection
  - A more precise second-source clock (50 or 60 Hz mains) can be used to enhance the long-term precision of the calendar:
  - The reference clock is automatically detected and used to enhance the calendar precision
  - The LSE clock is automatically used to update the calendar whenever the reference clock becomes unavailable

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This slide presents the main calendar features.
Daylight savings can be managed by software, with automatic 1 hour addition or subtraction.
It is possible to synchronize the RTC clock to a remote clock by adding or subtracting an offset to the sub-second register on the fly, with ck_apre clock resolution. This feature is commonly used in RF applications.
A reference clock, mains at 50 or 60 Hz, can be used to enhance long-term calendar precision. The reference clock is automatically detected.
When the 1 Hz clock becomes misaligned due to the imprecision of the LSE clock, the RTC shifts the 1 Hz clock a bit so that future 1 Hz clock edges are aligned. Thanks to this mechanism, the calendar becomes as precise as the reference clock.
When the reference clock is not available, the LSE clock is automatically used to update the calendar.

RTC calendar features

- Timestamp
  - Calendar value is saved in timestamp registers on external I/O event
  - Internal timestamp detection when a switch to VBAT occurs
  - Optional timestamp in case of tamper detection
- If a new timestamp event is detected while the timestamp flag (TSF) is already set, the timestamp overflow flag (TSOVF) flag is set

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A timestamp function is available: the sub-second, time, and date values are saved in timestamp registers when an event occurs on the timestamp I/O.
A timestamp event can also occur when a switch to V_{BAT} is performed , or when a tamper event is detected.
If a timestamp event occurs while the timestamp flag is set, the timestamp overflow flag is set.
In this case, timestamp registers maintain the timestamp of the previous event.

Smooth digital calibration

Crystal inaccuracy compensation

- Calibration is always running
  - LPCAL = 0 : Calibration window is 2^{20} RTCCLK = high consumption mode
  - LPCAL = 1 : Calibration window is 2^{20} ck_apre = low consumption mode = recommended
- Consists in masking/adding N (configurable) 32 kHz clock pulses, fairly well distributed in a configurable window
- Calibration value can be changed on the fly
- A 1 Hz output is provided to measure the crystal frequency and the calibration result

Calibration window	Accuracy	Total range
2^{18} cycles: 8s with LSE and LPCAL=0	± 1.91 ppm	[-487.1 ppm, +488.5 ppm]
2^{19} cycles: 16s with LSE and LPCAL=0	± 0.95 ppm	[-487.1 ppm, +488.5 ppm]
2^{20} cycles: 32s with LSE and LPCAL=0	± 0.48 ppm	[-487.1 ppm, +488.5 ppm]

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The digital calibration is used to compensate crystal inaccuracy and accuracy variations with temperature and aging.
The low power calibration is always running even when no correction is applied.
When the asynchronous prescaler is a power of two, it is possible to reduce drastically the RTC consumption by setting the LPCAL configuration bit to select the calibration low-power mode.
In this case the RTC calibration clock is ck_apre instead of ck_rtc, and the calibration window is 2**20 ck_apre instead of is 2**20 RTCCLK.
However the resulting accuracy remains unchanged, so the LPCAL configuration mode should be chosen.
The digital calibration consists in masking or adding a programmable number of RTC clock cycles, fairly well

distributed in a configurable window.
The calibration value can be changed on the fly, depending on detected temperature changes for instance.
A 1 Hz calibration output signal is provided to externally measure the crystal frequency before and after applying the calibration value.
The accuracy shown here is the resolution of the digital calibration.
When LPCAL=0, the calibration window size is configurable, between 8, 16, and 32 seconds. This LPCAL setting is useful to test the calibration result on the RTC output pin.
For a 32 seconds calibration window, the accuracy is plus or minus 0.48 ppm. The total correction range is from -487 to 488 ppm.
The accuracy resolution scales with the calibration window size.
Final accuracy in the application will depend on the crystal parameter precision, temperature detection precision, how often the software calibration procedure is launched, etc.
In order to reach the precision of the calibration window, the measurement window must be a multiple of the calibration window.

RTC programmable alarm

Two flexible alarms based on calendar value

- The Alarm flags are set if the calendar sub-seconds, seconds, minutes, hours or date match the value programmed in the alarm registers
- 2 alarms, which exit the device from all low-power modes
- Alarm event can also be routed to the specific output pin RTC_OUT, with configurable polarity
- Calendar sub-second, seconds, minutes, hours or date fields can be independently selected (masked or not masked)
  - Masks allow configuration of periodic alarm interrupts

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The RTC embeds two flexible alarms, based on comparison with the calendar value.
The alarm flags are set if the calendar sub-seconds, seconds, minutes, hours or date match the value programmed in the alarm registers.
The alarms events can wake up the device from all low-power modes.
The alarms event can also be routed to the specific output pin RTC_OUT, with configurable polarity.
The calendar alarm sub-second, seconds, minutes, hours or date fields can be independently masked or not masked for the comparison.
When the masks are used, periodic alarms are generated.

Periodic auto-wakeup

Flexible periodic wakeup interrupt

- The periodic wakeup flag is generated by a 16-bit programmable binary auto-reload down counter (can be extended to 17 bits)
- Able to exit the device from Stop/Standby/Shutdown modes

Wakeup timer (WUT) clock	Wakeup period	Resolution
RTCCLK divided by 2, 4, 8, 16	From 122 µs to 32 s when RTCCLK = 32.768 kHz	Down to 61 µs
ck_spre	From 1 s to 36 hours when ck_spre = 1 Hz	1s

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In addition to the calendar and alarms, another 16-bit auto-reload counter can generate periodic events with wakeup from low-power modes capability. This counter cannot be read.
Depending on the software configuration, the wakeup timer clock can be the RTC clock divided by 2, 4, 8 or 16, or the output of the synchronous prescaler.
With the divided RTC clock, the wakeup period can be from 122 microseconds to 32 seconds when the RTC clock frequency is 32.768 kHz.
The resolution is down to 61 microseconds in this case.
With the ck_spre clock, the wakeup period can be from 1 second to 36 hours when the ck_spre clock is at 1 Hz.

Interrupts

Interrupt event	Description
Alarm A	Set when the calendar value matches the Alarm A value
Alarm B	Set when the calendar value matches the Alarm B value
Wake-up timer	Set when the wakeup auto-reload timer reaches 0
Timestamp	Set when a timestamp event occurs

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Several RTC events can generate an interrupt.
All interrupts can wake up the microprocessor up from all low-power modes.
The Alarm A interrupt is set when the calendar value matches the Alarm A value.
Similarly, the Alarm B interrupt is set when the calendar value matches the Alarm B value.
The wakeup timer interrupt is set when the wakeup auto reload timer reaches zero.
The timestamp interrupt is set when a timestamp event occurs.

Low-power modes

Mode	Description
Run	Active
Sleep	Active • RTC interrupts cause the device to exit Sleep mode
Low-power run	Active
Low-power sleep	Active • RTC interrupts cause the device to exit Low-power sleep mode
Stop 0 / Stop 1 / Stop 2	Active when clocked by LSE or LSI • RTC interrupts cause the device to exit Stop 0/Stop 1 mode
Standby	Active when clocked by LSE or LSI • RTC interrupts cause the device to exit Standby mode
Shutdown	Active when clocked by LSE • RTC interrupts cause the device to exit Shutdown mode

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The RTC peripheral is active in all low-power modes and the RTC interrupts cause the device to exit the low-power mode.
In Stop 0, Stop 1, Stop 2 and Standby modes, only the LSE or LSI clocks can be used to clock the RTC.
Only the LSE is functional in Shutdown mode, because this oscillator belongs to the V_{BAT} domain.

Debug information

- DBG_RTC_STOP bit: RTC counter stopped when core is halted

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A bit is available in the MCU Debug interface, that enables to stop the RTC counter when the core is halted for debugging.

Related peripherals

- Refer to these peripheral trainings linked to the RTC
  - Tamper and backup registers (TAMP)
  - Reset and clock control (RCC)
  - Power control (PWR)
  - Extended interrupt controller (EXTI)

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This is a list of peripherals related to the real-time clock. Please refer to these peripheral presentations for more information if needed.

- Tamper and backup registers
- Reset and clock control
- Power control
- Extended interrupt controller.

Thank you

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Thanks for attending this presentation.