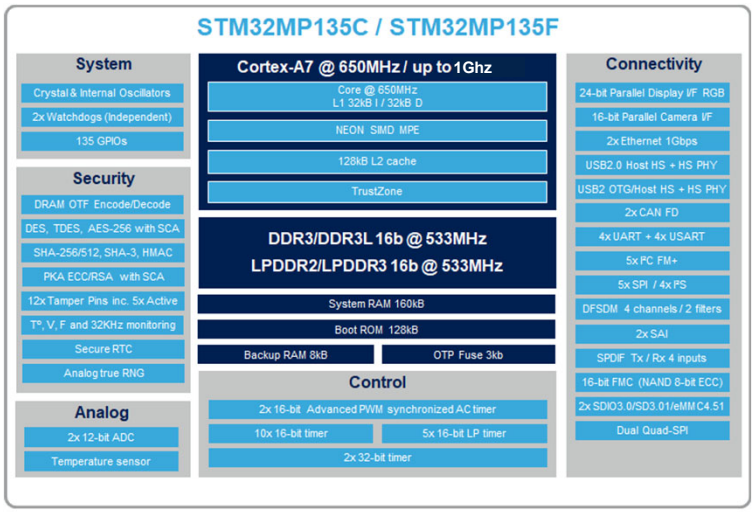
Hello, and welcome to this presentation of the STM32MP13 introducing the system architecture.

STM32MP13x Block Diagram



Cortex-A7 @ 650MHz only from -40°C<Tj<125°C
Cortex-A7 @ 1GHz only from -40°C<Tj<105°C

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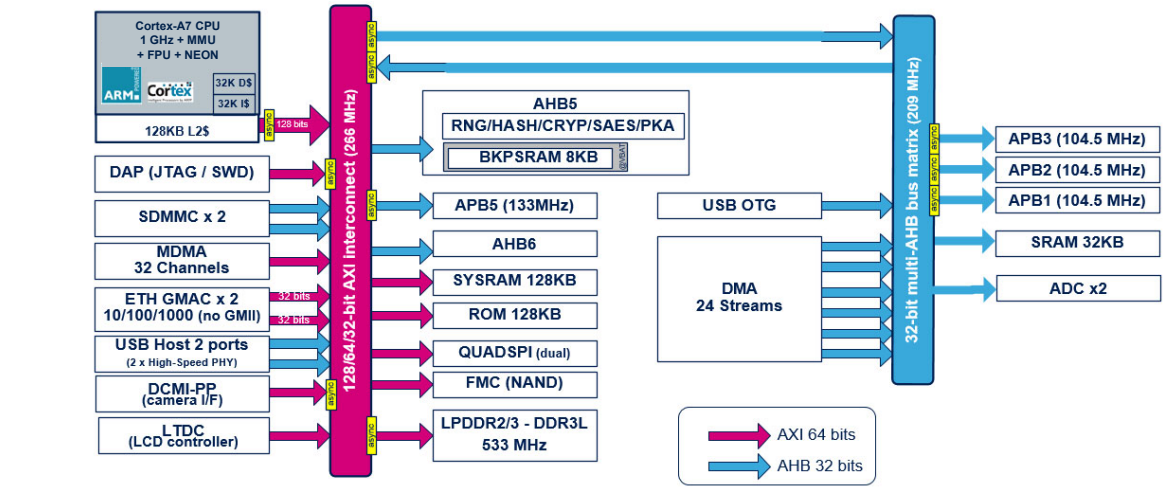
This block diagram summarizes the key features of the STM32MP135F which is part of the STM32MP1 Series.
The STM32MP135F microprocessor integrates a Cortex®-A7 32-bit core with single- and double-precision floating point units, plus the Arm® NEON™ Advanced SIMD instruction set, and can run up to 1GHz. It has a 32 Kbytes level 1 Instruction Cache and a 32 Kbytes level 1 Data Cache, plus 128 Kbytes of level 2 cache.
The internal SRAM memory size is 168 Kbytes with a scattered architecture split into:

- 128 Kbytes of AXI System RAM
- plus 32 Kbytes of AHB RAM
- and 8 Kbytes of SRAM in backup domain to keep data in the lowest power modes.

This line also includes up to 30 communication peripherals in addition to an LCD-TFT controller interface.
The STM32MP135 line also embeds low-power 12-bit ADCs running at up to 5 Msamples/s, as well as 24 timers.
And it includes a rich set of security features.

STM32MP13x bus architecture overview



The STM32MP1 bus architecture is split into two interconnected matrices (AXI Arm Cortex-A7 and AHB) operating in different frequency domains, which can be set in low power modes independently.

- A high-speed Arm CoreLink NIC-400 network interconnect AXI-based performing interconnection between masters and slaves on Arm Cortex-A7 side (called MPU-side), operating at 266 MHz (ck_aclk) and allowing an internal bandwidth up to 2 Gbytes/s between each master and slave. This matrix is optimized for low latency and very high bandwidth master transfers to and from external DDRs, as well as internal SRAMs. An external DDR memory provides a

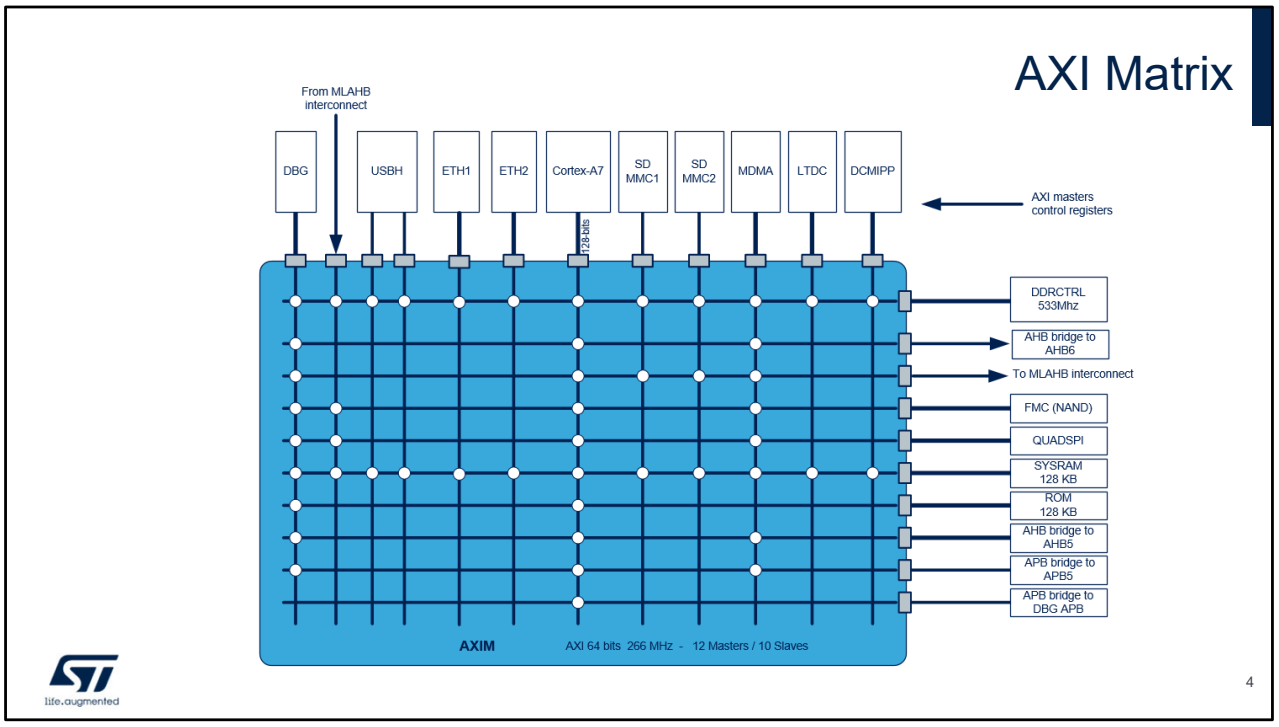
raw bandwidth up to 4 GBytes/s. Peripherals belonging to the AXI domain are connected to the AHB5, AHB6, APB4 (thru AHB6) and APB5 buses.

And

- A multi-layer AHB interconnect (MLAHB) performing interconnection between lower bandwidth masters and slaves with an architecture inherited from STM32MP15x lines MCU, and operating at 209 MHz.

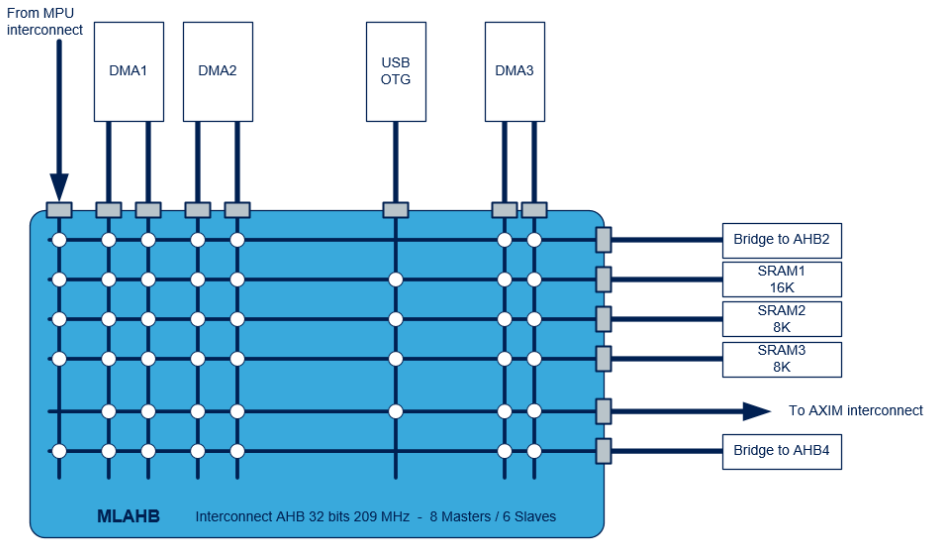
The AXI interconnect matrix (AXIM) and Multi-layer AHB (ML-AHB) are connected together to enable the sharing of any peripheral by any master.
Blocks with dashed lines are not available on all product lines.

Security is not shown in this overview.



The AXI Matrix enables the interconnection of up to 12 masters and 10 slaves peripherals.
The AXI Matrix is dedicated to high bandwidth masters, bulk memories and security peripherals.

MLAHB Matrix



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The Multilayer AHB Matrix enables the interconnection of up to 8 masters and 6 slaves peripherals.
It is dedicated to low bandwidth and real time masters and peripherals.

Memories Summary

	Memory	Type	Size	TrustZone Access Control	On the fly encryption/ decryption
Embedded memories	BOOTROM	ROM	128 KB	●	-
	SYSRAM	SRAM	128 KB	●	-
	AHB RAM	SRAM	32 KB	●	-
	BKPSRAM	SRAM (On VBAT)	8 KB	●	-
External memories	DDR SDRAM	DDR3, DDR3L, LPDDR2, LPDDR3	Up to 1 GB	●	●
	SDMMC	SD-Card, e•MMC		-	-
	QUADSPI	SPI Flash	Up to 512 MB (1) Up to 4 GB (2)	-	-
	FMC NOR	NOR Flash, SRAM	Up to 256 MB	-	-
	FMC NAND	NAND Flash	Up to 256 MB	-	-

(1) Memory-mapped mode
(2) Indirect-mode

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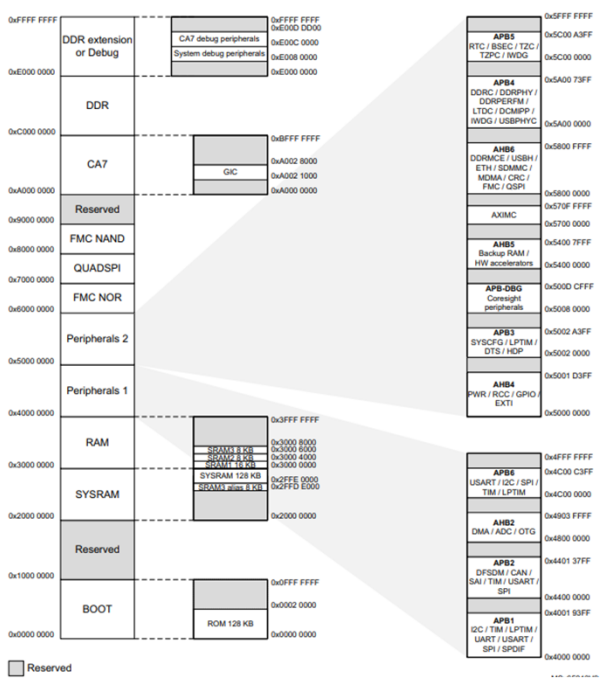
All memories are accessible by the Cortex-A7 core, and the BootROM is dedicated to Cortex-A7 core accesses.
The DDR memory benefits from the “on the fly encryption/decryption” feature.

Memory Map overview



- Uniform memory map
  - All peripherals visible at same address of every masters
  - No Remap

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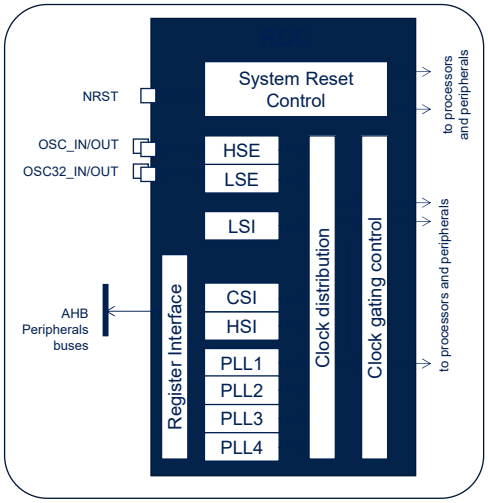
The memory map addressed by any master is the same, except for debug components which are at different addresses for debugger and Cortex-A7.
There is no dynamic memory remapping, only part of the MLAHB SRAM memory (SRAM3) is aliased in two locations, mainly to allow higher continuous memory space for the downloading of the first stage bootloader (FSBL) from the external eMMC memory during boot phase.

Reset and Clocking (RCC)



- The Reset and Clock Controller (RCC) manages:
  - The generation of all the clocks,
    - 4xPLLs, RC oscillators, Crystal oscillators…
  - The gating of all the clocks
    - Possibility to enable/disable clocks for each peripheral
  - The control of all the system and peripheral resets.

Application benefits

- High flexibility regarding the clock sources to meet consumption and accuracy requirements.
- Safe and flexible reset management

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The reset and clock controller (RCC) manages system reset and peripherals clock generation.
The STM32MP13x microprocessor embeds 3 internal oscillators, 2 oscillators for an external crystal or resonator, and 4 phase-locked loops (PLLs) managed by the RCC.
Outside the RCC, there is also one dedicated PLL for the High-Speed USB.
Many peripherals have their own clock, independent of the system clock to allow maximum flexibility.
The RCC provides high flexibility in the choice of clock sources. This enables the system designer to meet both power consumption and accuracy requirements.
The numerous independent peripheral clocks allow a designer to adjust the system power consumption without

impacting the communication baud rates, and also keep some peripherals active in low-power mode.

Power Supplies

Name	Typical or Range	Description
VDD	**1.71V – 3.6V**	Power supply input for I/Os
VDD_ANA		Power supply input for system analog like RCC, PWR. To be connected to VDD
VDD_PLL		Power supply input for PLLs. To be connected to VDD
VDDSDx (x=1,2)	**0V – 3.6V**	Power supply for I/O's in dedicated VDDSDx domain (*)
VBAT	**1.2V – 3.6V**	Backup battery supply input
VDDCORE	**1.23V – 1.29V**	Power supply input for Digital Core domain
VDDCPU	**1.30V – 1.37V** (>650MHz) **1.23V – 1.37V** (<650MHz)	Power supply for Cortex®-A7 core
VDDA	**1.62V – 3.6V**	Analog Power supply input for ADCs and voltage reference buffers
VDDQ_DDR	**1.2V / 1.35V / 1.5V****	Power supply input for DDR Physical Interface (PHY) and IOs
VDD3V3_USBHS	**3.3V**	Power supply input for USB Physical Interface (PHY) and IOs
Internally generated Power Supplies (powered by VDD, or can be powered externally)		
VDDA1V8_REG	**1.8V**	Analog Power Supply input or output, used internally for USB Physical Interface (PHY)
VDDA1V1_REG	**1.1V**	Analog Power supply input or output, used internally for USB Physical Interface (PHY)

(*) used for SDCard UHS-I mode dynamic voltage setting with no need for external level shifter
(**) LPDDR2/LPDDR3, DDR3L and DDR3 respectively

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The STM32MP13x microprocessor requires various dedicated power supplies to work.

- VDD has a wide range and is mostly used to supply the I/O's.
- VDDSD1 and VDDSD2 are the supplies for dedicated I/O's, independent from VDD, used if needed to dynamically change the I/O voltage of SDCard I/O's in UHS-I mode, without the need for external level shifters.
- VDDCORE is the main supply for the internal logic.
- VDDCPU is the supply for the Cortex-A7 MPU core. It can be used in regular or overdrive mode to reach higher frequency on the Cortex-A7.
- VDDA is used for the analog parts of the chip.
- VDDQ_DDR is the I/O voltage for the DDR interface. This voltage depends on the selected memory type and is 1.2V for LPDDR2 or LPDDR3, 1.35V for DDR3L, and 1.5V for DDR3 memories.

high-speed physical interface ports.

The STM32MP13x also embeds internal regulators to supply the USB physical interfaces.

Power Controller (PWR)

System mode	Description
Run	Clocks are active and forwarded to the system
Stop / LP-Stop	Clocks are stopped. Some platform supplies are powered down (Lp-Stop). Some peripherals could request clock while in Stop / Lp-Stop
LPLV-Stop	Clocks are stopped. Some platform supplies are powered down. VDDCORE and VDDCPU voltage can be reduced
LPLV-Stop2	Clocks are stopped. Some platform supplies are powered down. VDDCORE voltage can be reduced, VDDCPU voltage is powered down
Standby	Most platform supplies are powered down. VDDCORE and VDDCPU supplies are powered down. Backup domain may be active
Off (Vbat)	All Platform, Core and IOs supplies are powered down. Backup domain may be active

System mode	Wakeup sources (*)
Stop / LP-Stop	DBG, PVD, AVD, USBH, OTG, CEC, ETH, USARTx, I2Cx, SPIx, DTS, LPTIMx, GPIOs
LPLV-Stop / LPLV-Stop2	PVD, AVD, TEMP, USARTx, I2Cx, SPIx, DTS, LPTIMx, GPIOs
Standby	Six GPIO wakeup pins
Off (Vbat)	RTC/TAMP event could request PMIC to restore power supplies

(*) all modes: BOR, VBATH/VBATL, TEMPH/TEMPL, LSE CSS, RTC/auto wakeup, tamper pins, IWDGx

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Entering low power mode is controlled by software.
The LP-Stop system mode can be used to control external supplies so as to reduce the system power.
LPLV-Stop system mode can be used to control external supplies as well as lower VDDCORE voltage so as to reduce system power.
LPLV-Stop2 system mode can be used to control external supplies as well as reduce the VDDCORE voltage and power down the VDDCPU voltage so as to reduce system power.
External power supplies are controlled using dedicated PWR_ON or PWR_LP signals in addition to external software settings when an external Power Management IC (PMIC) is used.

Peripherals (1)

Timers	Advanced	16 bits	2
	General purpose	16 bits	8 (6 Securable)
		32 bits	2
	Basic	16 bits	2
	LP Timer	16 bits	5 (2 Securable)
	A7 Timers	64 bits	4 (Secure, Non-Secure, Virtual, Hypervisor)
	RTC/AWU		1 (Securable)
	Watchdog		2 (Independent, Independent Secure)
Communication Peripherals	SPI		5 (2 Securable)
		having I2S	4
	I2C (with SMB/PMB support)		5 (3 securable)
	USART (Smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 2 Securable USART)
	SAI		2 (up to 4 audio channels), with I²S master/slave, PCM input, SPDIF-TX
	USB	EHCI/OHCI Host	2 ports
			embedded HS PHY with BCD
		OTG HS	Yes, Embedded HS PHY with BCD (Securable)
		Embedded PHYs	2 x High-Speed shared between Host and OTG
	SPDIFRX		4 inputs
	FDCAN		2 (1 x TT-FDCAN), Clock Calibration, 10 Kbytes shared buffer

Boot Source

Boot Source

- All Peripherals Input/Output (when existing) are mapped through GPIO alternate functions

Not Available on all product lines

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Peripherals with I/Os are mapped on GPIO alternate functions (AFMUX).
Some peripherals are managed by BOOTROM and can be used as system control or program download during the initialization phase.
UART and USB are used to set up the system and/or download code into the external Flash memory.
Note that FDCAN is not available on the STM32MP131 line.

Peripherals (2)

SDMMC (SD, SDIO, eMMC)		2 (8 + 8 bits) (Secure), eMMC or SD	Boot Source
QuadSPI		1 (dual-quad) (Secure)	Boot Source
FMC	Parallel Address/Data 8/16-bits	4 x CS, up to 4 x 64MBytes	
	Parallel AD-Mux 8/16-bits	4 x CS, up to 4 x 64MBytes	
	NAND 8/16-bits	Yes, 2 x CS, SLC, BCH4/8	Boot Source
Gigabit Ethernet		2 x (MII, RMII, RGMII) with PTP and EEE	
DMA		3 instances (1 Secure) , 32 channels MDMA	
Cryptography		PKA (with DPA protection), DES, TDES, AES-256 (with DPA protection) (all Securable)	
Hash		SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3, HMAC (all Securable)	
True random number generator		True-RNG (Securable)	
Fuses (One Time Programming)		3072 effective bits (Secure, >1500 bits available to user)	
Digital Camera Interface	bus width	Up-to 16-bits Pixel clock up to 120 MHz	
LCD-TFT controller		Up-to 24-bit // RGB888 2 layers with programmable LUT (1 secure) Pixel clock up to 90 Mhz Up to WXGA (1366 x 768) @ 60 fps or Full HD (1920 x 1080) @30 fps	

GPIOs with interrupt (total count)		135
	Securable GPIOs	all
	Wakeup pins	6
	Tamper pins (Active tamper)	12 (5)
DFSDM		4 input channels with 2 filters
12 bit synchronized ADC		2 x (Securable)
	ADC channels in total (differential)	18 (8)
Internal ADC VREF generation		1.5V, 1.8V, 2.048V, 2.5V or VREF+ input
	VREF+ input pin	Yes

Not Available on all product lines or packages

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SDMMC can be a boot source by using either the SD-Card (SDMMC1) or eMMC (SDMMC2) memory cards.
QUADSPI bank1 can be a boot source for Serial-NOR or Serial-NAND Flash memories.
FMC could be a boot source for SLC parallel-NAND Flash memories.
Cryptography is not available on STM32MP13xA and STM32MP13xD devices.
There is only one ADC on STM32MP131x.
A camera interface is only available on STM32MP135x.

OTP Fuses

- OTP Fuses are One Time Programming memory
  - Initial bits are ‘0’ and are irreversibly programmed to ‘1’
  - Incremental programing of bits in a 32-bit word is possible
- Handled thru BSEC controller IP
  - Programming, reading, status and locking handled by BSEC
  - Lock mechanism to avoid read and/or program (32-bits granularity)
- OTP Content
  - Product configuration and Trimming values set by ST during production
  - Secrets and unique identification numbers set by ST during production
  - Device configuration set by OEM (e.g. MAC address, boot source, security mode, etc...)
  - Secrets set by OEM (e.g. for secure boot)
  - Up to 1184 bits available for other OEM purposes

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OTP fuses are memory fields which can be programmed once and then no longer altered.
The BSEC IP manages the control of the OTP fuses, including reading, programming and secure accesses.
The OTP content includes product configuration and unique numbers.
The OTP can contain OEM information such as the MAC address, secret keys or any relevant data.
Up to 1184 bits are fully available for various OEM purposes.

System control & Security

- System control
  - RCC
    - Reset and Clock Controller
  - PWR
    - Power modes Controller
  - EXTI
    - External Interrupt management
  - SYSCFG
    - Various system level configuration
  - MDMA, DMA1/2/3, DMAMux1/2
    - Direct Memory Access
    - MDMA chained to DMA1/2/3
    - DMAMux1/2 used for requestor flexibility
    - DMAMux2 + DMA3 used for secure transfer.

- Security
  - ETZPC
    - Control security level of some peripherals as well as SYSRAM and BKPSRAM
  - TZC
    - Security firewall for DDR data accesses
  - BSEC
    - Global security settings and OTP fuses control
    - Contains Device Electronic Signature registers
  - TAMP
    - Tamper pins and backup registers management
  - BKPSRAM
    - securable memory, Tamper protected
  - SAES
    - Secure AES coprocessor
  - CRYP, PKA, HASH, RNG and CRC
    - Secure instances

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Various blocks manage transversal system control. The major ones are the Reset and Clock Controller (RCC), and the power manager (PWR) which controls the system power modes.
Security is controlled by Trustzone inside the Cortex-A7 core as well as various blocks.
The Enhanced TrustZone Protection Controller (ETZPC) defines which peripherals are secure or not, isolated or not.
The TrustZone Address Space Controller for DDR (TZC) blocks unwanted access to DDR data.

Annex

- Keys points
  - Cortex-A7 MPU subsystem can run powerful open operating systems like Linux or Android
  - Large external DDR memory
  - Advanced security implementation
- Hardware architecture reference documents
  - STM32MP13x Datasheet
  - STM32MP13x Reference Manual
- Additional available documents
  - AN5474 – Getting started with STM32MP13x lines hardware development

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The main points to be noted from this presentation are:

- The STM32MP13x embeds a Cortex-A7 core capable of running powerful operating systems like Linux or Android.
- The STM32MP13x always needs an external DDR memory to run the operating system.
- The STM32MP13x includes advanced security implementation for highly secured applications.

Thank you

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