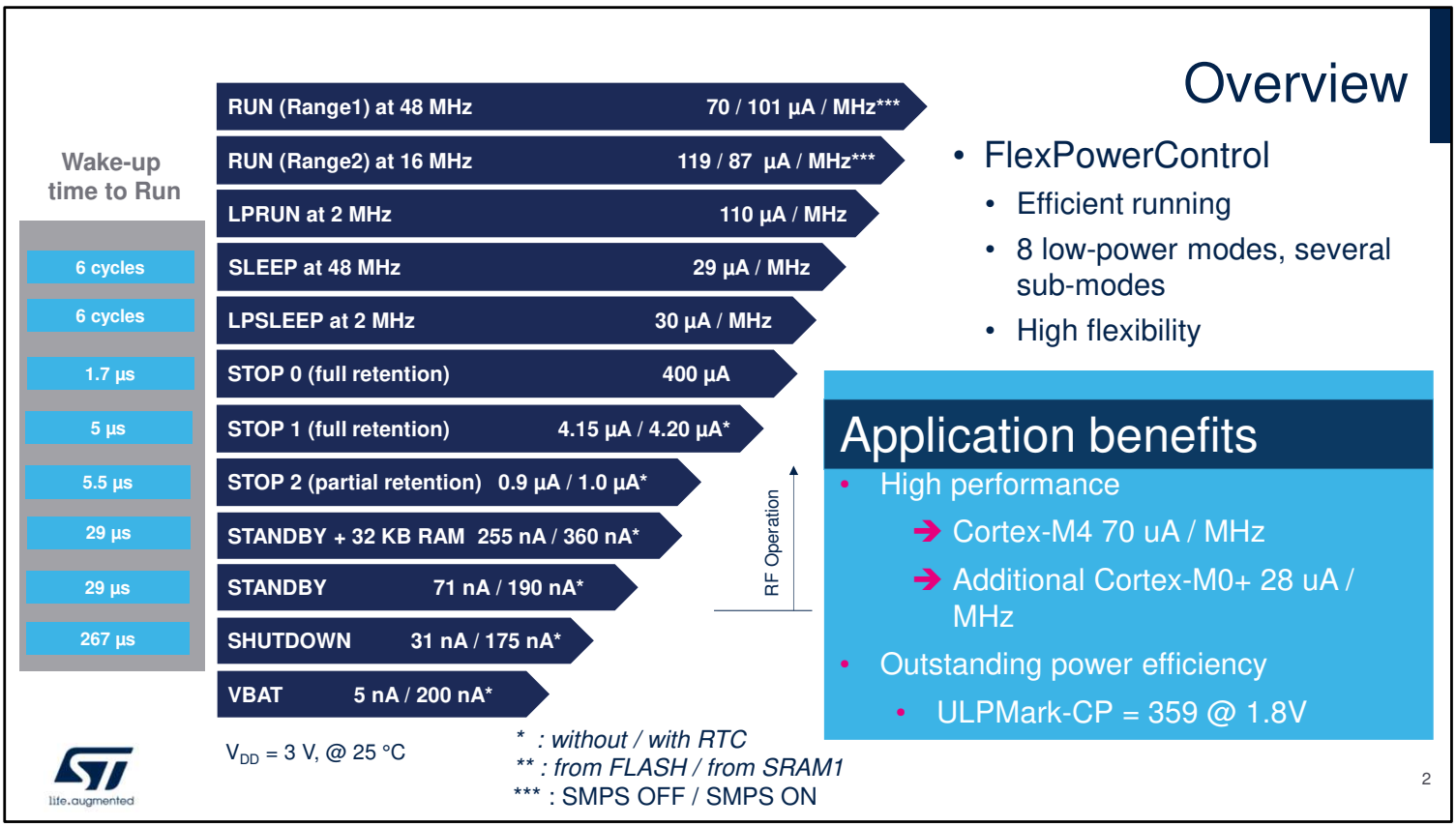
STM32WL5- PWR

Power Controller

Revision 1.0

Hello, and welcome to this presentation of the STM32WL5 power controller. Power management functions and all power modes will also be covered in this presentation.



STM32WL5 devices feature FlexPowerControl, which increases flexibility in power mode management and further reduces the overall application consumption. Run mode can support a system clock running at up to 48 MHz, with only 70 µA/MHz.

STM32WL5 devices support 8 main low-power modes: Low-power run, Sleep, Low-power sleep, Stop 0, Stop 1, Stop 2, STANDBY with RAM retention, Standby and Shutdown modes. Each mode can be configured in many ways, providing several additional sub-modes. Note that for RF operation, the system cannot go below Standby with RAM retention mode as a minimum set of contexts needs to be maintained.

In addition, STM32WL5 devices support a battery backup domain, called VBAT.

The high flexibility in power management provides performance with Cortex-M4 consumption of 70 uA / MHz and simultaneous Cortex-M0+ consumption of 28 / MHz

running also CoreaMark, together with outstanding power efficiency, demonstrated by the ULPMark-CoreProfile score equal to 359 at 1.8V and 223 @ 3V.

Key features

- 8 low-power modes with fast wakeup
  - Down to 30 nA with I/O wake-up
  - Down to 255 nA with 32 KB RAM retained
  - Wake-up from high number of peripherals
- Down to 70 µA/MHz in Run mode from Flash memory
- VBAT Battery backup mode with RTC and backup registers
- Flexible power distribution

Application benefits

- High flexibility to lower power consumption depending on active peripherals, required performance and needed wakeup sources
- Increased battery life
- Autonomous radio operation
- BOM cost-saving by removing external shifters and components

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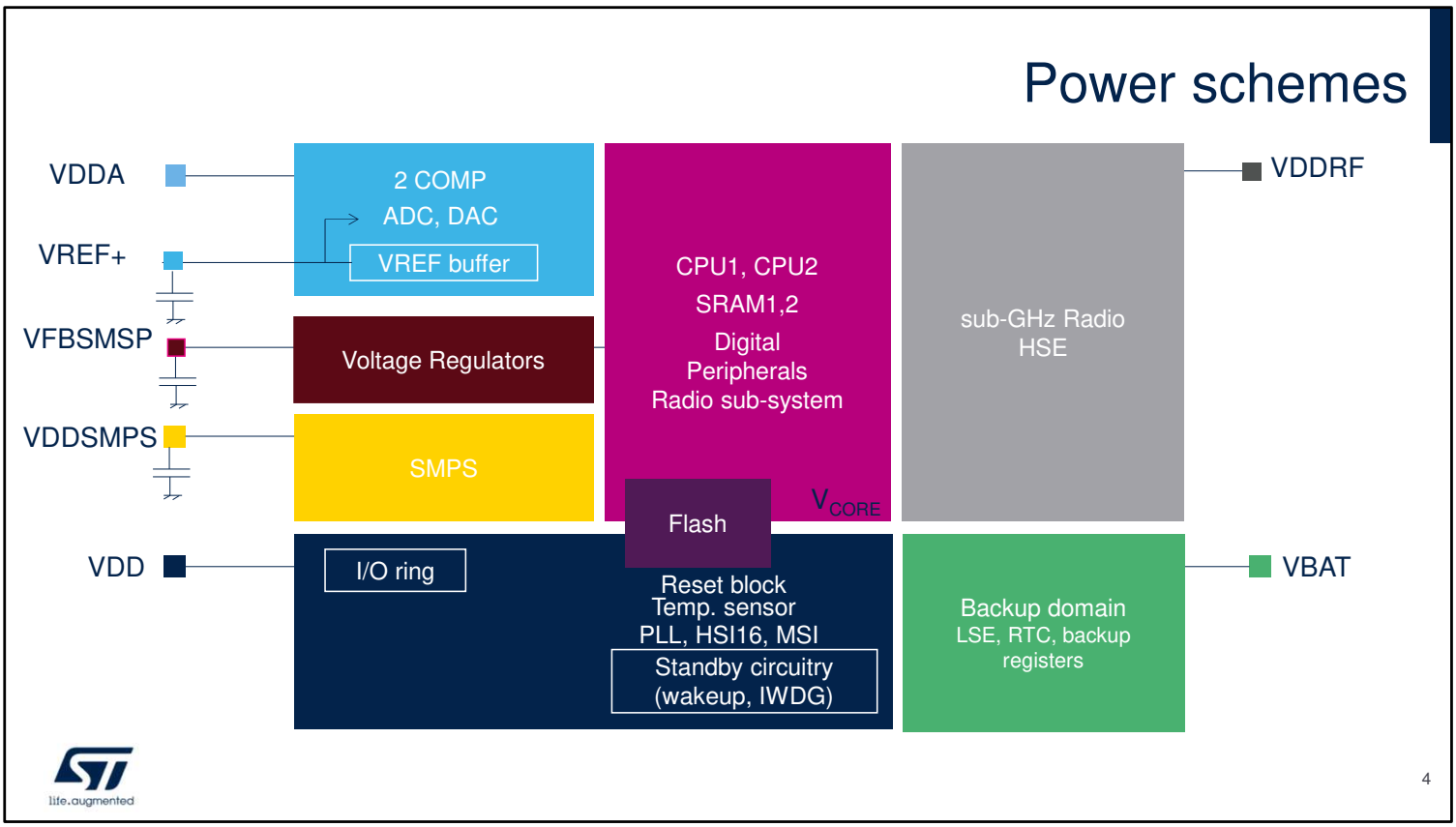
The STM32WL5 has several key features related to power management:
Several low-power modes, down to 30nA while it is still possible to wake up the MCU with an event on an I/O. For only 255 nA, 32 Kbytes of SRAM can be retained. Many peripherals can wake up from the various low-power modes.
Dynamic consumption is down to 70 µA/MHz, executing from Flash memory.
A battery backup domain, called VBAT, including the RTC and certain backup registers.
Several power supplies are independent, allowing reduction MCU power consumption while some peripherals are supplied at higher voltages.
Thanks to the large number of power modes, STM32WL5 devices offer high flexibility to minimize the power consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.



STM32WL5 devices have several independent power supplies, which can be set at different voltages or tied together.

The main power supply is V_{DD}, supplying all I/Os, the reset block, temperature sensor and most internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog as well as the Radio. V_{DD} is monitored by the BORS circuitry.

V_{DDSMPS} supplies the Switch Mode Power Supply step-down converter. Its output V_{FBSMPS} supplies the CPU with most of the digital peripherals and the SRAMs. The Flash memory is supplied by both V_{FBSMPS} and V_{DD}.

STM32WL5 features several independent supplies for peripherals: V_{DDA} for the analog peripherals, V_{DDRF} for the sub-GHz Radio.

The internal Reference Voltage used by analog block can be output on V_{REF+} pin to supply external circuitry for the application.

A backup battery can be connected to the VBAT pin to supply the backup domain.

SMPS

Improving Power Efficiently

- The SMPS is used to step down the VDD supply.
- The SMPS supplies the digital core and sub-GHz Radio (typ: 1.5 V)
- The SMPS follows the device operating modes
  - Can only be ON in Run, Low-power Run, Sleep, Low-power Sleep and Stop0 modes and when ever the sub-GHz radio is active.
  - In Stop1, 2, Standby and Shutdown modes the SMPS is automatically in Open mode.
    - When waking up it automatically resume the mode that was used before entering.

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The SMPS supplies the digital core and radio LDOs.
The SMPS operating mode (on and off) follows the device modes.
The SMPS supports switching on the fly when requested by firmware.
To remove any noise from the SMPS during ADC conversions, software may switch on the fly the SMPS mode.

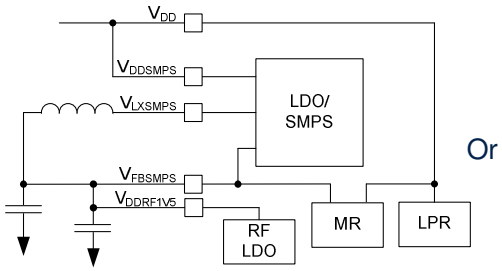
Supply configurations

Flexible selection between performance and cost

- Performance with SMPS
  - By adding an external coil the SMPS is used to lower power consumption.
- Low cost using only LDOs.
  - By not connecting the coil the SMPS mode can't be used. The LDOs are directly supplied from VDD. Saving the cost for the coil at the expense of increasing the overall power consumption.

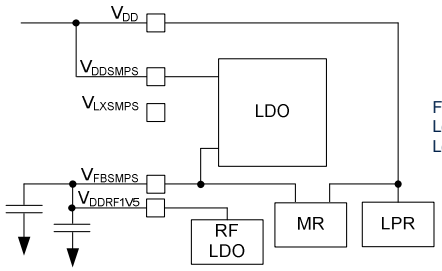
SMPS configuration

Full Vdd range [1.62..3.6V]
High efficiency SMPS



Or

LDO configuration



Full Vdd range [1.62..3.6V]
Low BOM
Low noise

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The STM32WL5 supply configuration is to be selected by hardware.
For the best power performance, use the SMPS configuration.
For the lowest cost, the LDO configuration can be used.

Power schemes

Optimized power and performance thanks to independent power supplies

- VDD , VDDSMPS and VDDRF from 1.71 to 3.6 V (down to 1.6 V at power-down)
  - 1.95 V min. for sub-GHz radio operation
- VFBSMPS regulated 1.5 V
- VDDA from 1.62 to 3.6 V
  - 1.62 V min. when ADCs or COMPs are used
  - 1.8 V min. when DAC is used
  - 2.4 V min. when VREFBUF is used
- VBAT from 1.55 to 3.6 V including the RTC and backup registers

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The main power supply V_{DD} ensures full-featured operation in all power modes from 1.71 up to 3.6 V, allowing supply by an external 1.8 V (+-5%) regulator. Device functionality is guaranteed down to 1.61 V, the minimum voltage after which a brown-out reset is generated.
sub-GHz radio operation is allowed down to 1.95 V.
Other independent supplies are provided to allow peripherals to operate at a different voltage.
The V_{DDSMPS} is connected to the same supply as V_{DD}.
The analog power supply V_{DDA} can be connected to any voltage other than V_{DD}.

When the analog-to-digital converters or comparators are used, the V_{DDA} voltage must be greater than 1.62 V.

When the digital-to-analog converted is used, V_{DDA} must be greater than 1.8 V.

When the voltage reference buffer is used, V_{DDA} must be greater than 2.4 V.

A backup domain is supplied by VBAT, which must be greater than 1.55 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the backup registers.

Voltage supply supervision (1/2)

Supply supervision enabling dynamic power management

- Supply voltage monitoring is provided on:
  - VDD via POR/PDR, BOR (reset/switching on the fly), and PVD (threshold interrupt on EXTI).
  - VDDA via PVM (threshold interrupt on EXTI)
  - VBAT via ADC
  - VBKUP monitors either VBAT or VDD (reset)
  - VFBSMPS SMPS regulated supply, via level detector (reset).
  - VDDRF via EOL (flag to be checked by firmware)

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The power supply supervisor allows dynamic power supply management.
STM32WL5 devices embed power management on main V_{DD}, analog V_{DDA}, V_{BAT} supply input, Switch Mode Power Supply V_{FBSMPS}, and sub-GHz radio V_{DDRF}.
The main V_{DD} supervision allows reset management and voltage detection via the power voltage detector (PVD) when V_{DD} crosses the selected threshold. The PVD can be enabled in all modes except Standby modes. Seven thresholds can be selected by software. The Brown-out level can be used to provide switching on the fly of the SMPS when V_{DD} drops below the threshold level.
On the analog V_{DDA} supply, a supervision circuit selected via PVM detects when V_{DDA} crosses a threshold. The PVM can be enabled in all modes except Standby modes.
On the V_{BAT} supply, a supervision circuit selected via PVM detects when V_{BAT} crosses a threshold.
On the SMPS V_{FBSMPS} supply, a supervision circuit will reset

the core when the supply is too low (<1.4 V).
On the sub-GHz radio V_{DDRF} supply an sub-GHz radio End Of Live detector is available. The sub-GHz radio supply detector can be enabled to be operational when the sub-GHz radio is active.

Power supply supervisor (2/2)

Safe and ultra-low-power reset management

- Brown-out reset is always enabled in all modes except Shutdown mode
  - 5 thresholds selected by option byte BOR_LEV[2:0], from VBOR0 = 1.7 V to VBORH4 = 2.95 V.
  - BOR1 to BOR4 can, according with option byte:
    - Ensure reset as soon as MCU drops below selected threshold, regardless of the VDD slope.
  - BOR0 (1.7 V) is always active except in Shutdown mode. BOR0 consumption in included in all datasheet figures.
- Power voltage detector active in all modes except Standby and Shutdown
  - 7 thresholds, selectable by software

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The power supply supervisor guarantees a safe and ultra-low power reset management.
STM32WL5 devices embed an ultra-low-power brown-out reset (BOR) which is always enabled in all power modes except Shutdown mode. The BOR ensures reset generation as soon as the V_{DD} drops below the selected threshold, regardless of the V_{DD} slope. Five thresholds from 1.7 to 2.95 V are selected by option byte programmed in Flash memory.
A power voltage detector can generate an interrupt when V_{DD} crosses the selected threshold. The PVD can be enabled in all modes except Standby and Shutdown modes. Seven thresholds can be selected by software. In addition, an external pin can be used to compare voltages.
The BOR consumption with the 1.7 V threshold is included in the datasheet.

Peripheral voltage monitor

Supervising Power supply

- Peripheral Voltage Monitor for VDDA comparator, with wakeup capability from Stop modes.

PWM	Power supply	PVM threshold
PVM3	V_{DDA}	VPVM3: 1.65 V

- By default, independent power supplies are electrically isolated and the peripherals/IO powered by them are not available. The power isolation must be removed by SW.

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The STM32WL5 MCU embeds one Peripheral Voltage Monitor to detect if the VDDA supply is present or not. This comparator has wake-up from Stop mode capability. The PVM3 compares the VDDA voltage with the 1.65 V threshold, intended for the comparators, analog-to-digital and digital-to-analog converters. The PVM1, PVM2 and PVM4 are not present in STM32WL5.
To guarantee any of the supply sequences on the application, power isolation has been implemented and is active by default. It is the role of software to enable the needed supplies by removing the power isolation.

Power schemes

Independent voltage reference supplies for analog performance

- VREF+: reference voltage for ADC and DAC.
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.
  - VREF+ pin, and thus the internal voltage reference, is not available on all package. On these packages, this pin is double-bonded with VDDA which can be connected to an external reference or VDD. When the internal voltage reference pin is not available its buffer must be kept disabled.
- The application SW can decide to disable the SMPS when performing analog signal conversions to reduce noise. SMPS mode change can be done on the fly.

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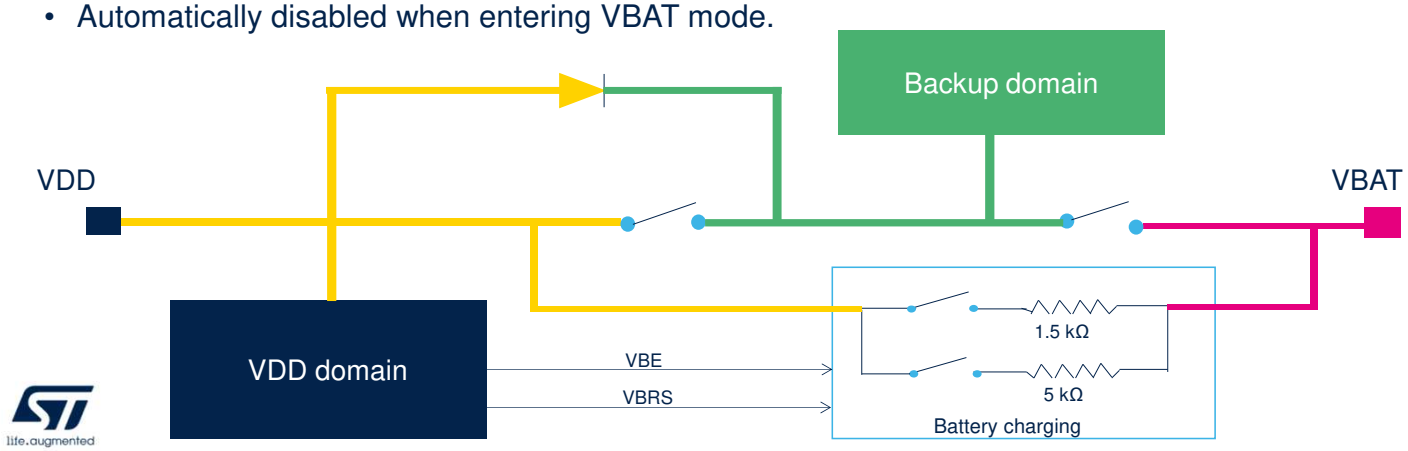
The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer. This allows improvement of the converters performance by providing an isolated and independent reference voltage. The VREF+ pin and thus the internal voltage reference, is not available on all packages. In these packages, the VREF+ is double-bonded with VDDA and the internal voltage buffer must be kept disabled. The voltage reference is provided through the VDDA pin in these packages.
The application software can decide to disable the SMPS when performing ADC or DAC conversion to reduce noise. In that case, application can decide to disable the radio sub-system during this conversion.

VBAT battery charging

Time Keeper operation

- A backup battery connected to VBAT can be charged from VDD.
  - Enabled by application Software
  - Selection between 2 charging resistor values (5 kOhm, 1.5 kOhm)
  - Automatically disabled when entering VBAT mode.



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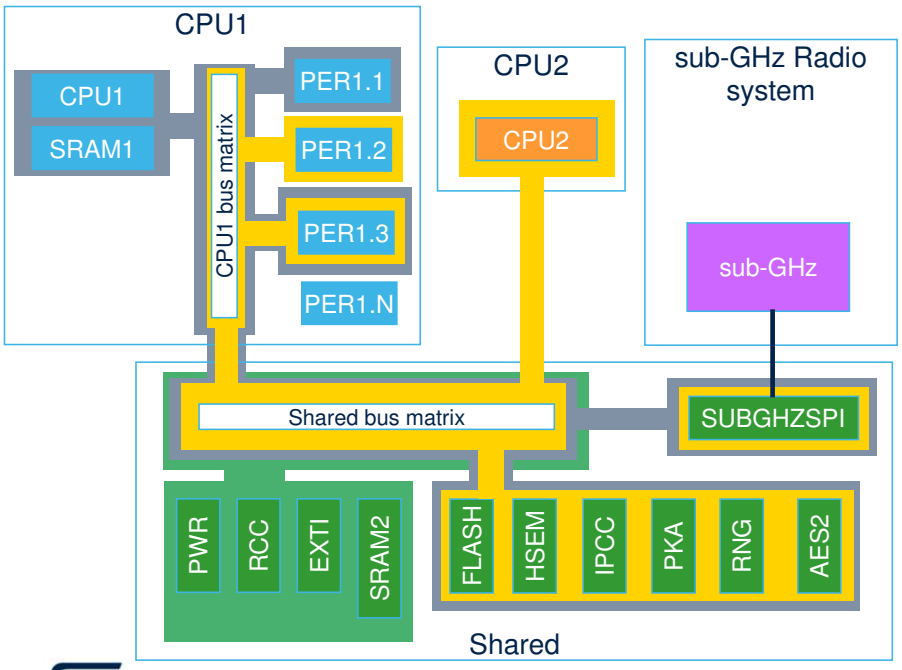
The battery charging feature allows charging a super-cap connected to VBAT pin through internal resistor when V_{DD} supply is present. The charging is enabled by software and is done either through a 5 kOhm or 1.5 kOhm resistor depending on software. Battery charging is automatically disabled in VBAT mode.

System overview



- 3 sub-systems
  - CPU1 Corex-M4 (Blue)
  - CPU2 Cortex-M0+ (Orange)
  - Radio system (Violet)
- Always clocked (Green)
- Independent operating modes
  - CRun
  - CSleep
  - CStop
- CPU peripheral allocation by enable bits in RCC (*refer to RCC presentation*)

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The STM32WL5 system contains three sub-systems. The CPU1 Cortex-M4, the CPU2 Cortex-M0+, and the sub-GHz Radio sub-system. Each of the three sub-systems can operate independently being in one of its operating modes CRun, CSleep, or CStop. Peripherals will only be clocked when the associated sub-system is in CRun mode, or CSleep when enabled in Sleep mode. The system resources such as RCC, PWR, EXTI and SRAM2, connected on the Shared bus will always be clocked when one of the CPUs in in CRun and the system is in Run mode. The other peripherals on the Shared bus may be enabled to operate with CPU1 and/or CPU2. The CPU1 bus matrix peripherals may be enabled to operate with CPU1 and/or CPU2. The sub-GHz Radio system is connected to the bus matrix via the sub-GHz serial peripheral interface. The sub-GHz Radio system may operate when both CPUs are in CStop mode, in this case all othere peripherals and all bus matrixes are stopped, and the system may be in Stop or Standby mode.

CPU sharing power modes

Automatic Power mode management

- Each CPU can decide independently which system low-power mode to use (Stop0, Stop1, Stop2, Standby, or Shutdown).
- Each CPU can decide which wakeup source will wake it up.
- When both CPUs enter WFI and/or WFE the HW mechanism executes the compatible request. It select the highest low-power mode compatible with the two CPU requirements.
- One CPU can wake up without the need to wake up the other one.
  - When the STM32WL5 wakes up from Stop modes, according the wakeup source, only the CPU registered for this wakeup source is restarted, the other one stays in WFI (or WFE) with its clock stopped.
  - When the STM32WL5 wakes up from Standby modes, according with the source, only the CPU registered for this wakeup source is restarted, the other one stays under reset mode.

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Each CPU can decide independently which low-power mode to use (Stop 0, Stop 1, Stop 2, Standby, or Shutdown).
Each CPU can decide which wakeup source (RTC, sub-GHz radio, GPIO, peripheral) will wake it up.
When both CPUs enter WFI and/or WFE, the hardware mechanism executes the compatible request. It selects the highest low-power mode compatible with the requirements from both CPUs.
One CPU can wake up without the need to wake up the other one if not required.
When the STM32WL5 wakes up from Stop mode, according with the wakeup source, only the CPU registered for this wakeup source is restarted, the other one stays in WFI or WFE with its clock stopped.
When the STM32WL5 wakes up from Standby modes, in accordance with the source, only the CPU registered for this wakeup source is restarted, the other one stays under reset mode.

Run mode (Run Range 1, Run Range 2 and Low Power Run) and Frequency selection changes are centralized to avoid conflicting configurations. This includes selection of the System clocks as well as low power enable and Voltage Range and Flash Memory configurations.

Sub-GHz radio power modes

- **Automatic Power mode management**

- The sub-GHZ radio can autonomously enter and exit its peripheral low-power modes.
- The sub-GHz radio can be woken-up by the sub-GHz radio low-power timer and by a CPU.
- The sub-GHz radio does not impact the CPUs/system low power modes. The sub-GHz radio may be active even when the system is in Stop or Standby mode.
- The sub-GHz radio can wakeup a CPU and the system from Stop and Standby modes with its wakeup interrupt.

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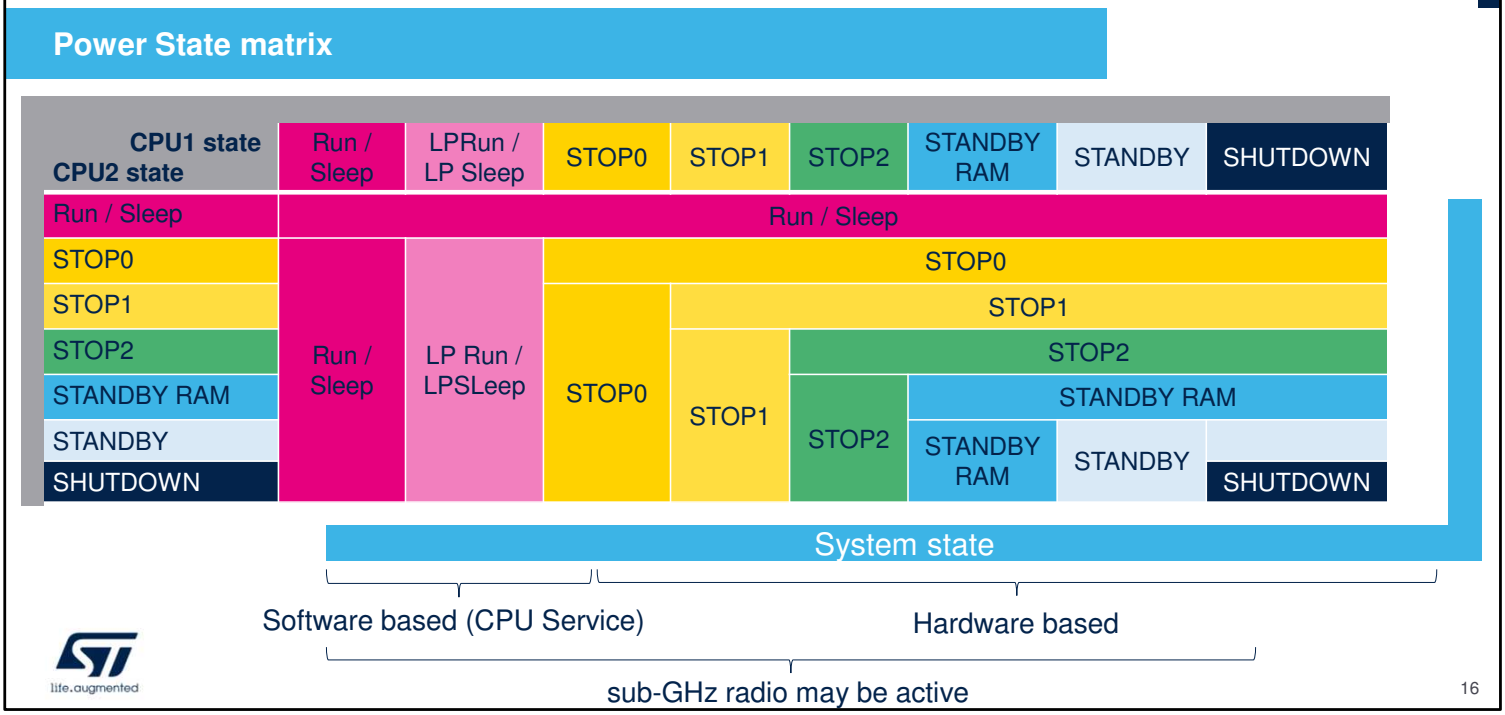
The sub-GHz radio sub-system operates autonomously and will enter and exit low-power modes on its own. It does not impact the CPUs and system low power modes.
The sub-GHz radio low-power timer and a CPU may wakeup the sub-GHz radio sub-system from its peripheral low power mode.

CPU state requirement versus allocation



According to the requirements of the CPU1 and CPU2, the Power controller hardware mechanism manages how the STM32WL5 reaches a given state. When CPU1 allows Standby mode and CPU2 allows only Stop2 mode, the system enters Stop2 mode.
Note that only the CPUs can place the system in LP Run or LP Sleep modes.
The sub-GHz radio may be active down to system Standby mode, independent from any CPU and system low power mode. The sub-GHz radio shall be disabled prior to the CPUs entering the system in Shutdown mode.

Power management

Control device supply

- Operating modes
  - CPU modes (CRun, CSleep, and CStop)
    - CPU enters low-power mode via WFI or WFE
    - CPU wakes up from interrupt, event, or reset.
  - Radio(CRun, CStop)
    - Radio enters low-power mode automatically.
    - Radio wakes up from sub-GHz radio RTC wakeup timer trigger.
  - System modes (Run, Stop, Standby, and Shutdown)
    - System enters low-power mode according to the operating mode of the 2 CPUs sub-systems
    - System wakes up from wakeup sources via EXTI or PWR.
- Voltage scaling
  - RUN mode Voltage Scaling (VOS), provides 2 ranges and a low-power Run mode.
    - Range 1 (High performance) up to 48 MHz.
    - Range 2 (low consumption) up to 16 MHz.
    - Low-power Run mode up to 2 MHz.

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Power management allows control the device power supply based on system operating mode. The system operating mode depends on the individual CPUs and Radio operating modes. The system is in Run mode whenever one of the 2 CPU sub-systems is in CRun or CSleep mode. The system enters Stop or Standby modes when both CPU sub-systems are in CStop mode.
In system Run mode, the device power supply can be scaled according to the required performance: Up to 48 MHz in Range 1, 16 MHz in range 2, and only up to 2 MHz in low-power Run mode.

CPU entering cstop

- When a CPU enters Cstop mode
  - the CPU clock domain may be clocked when the other CPU is in CRun or CSleep mode and has allocated peripherals.
  - the System may
    - stay in Run mode when the other domain CPU stay in CRun or Csleep mode, or a wakeup source remains active
    - enter Stop mode
    - enter Standby mode when allowed by both CPUs.
- The system operating mode depends on both CPUs.
- The sub-GHz radio has it own independent operating modes.

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A CPU enters the CStop mode when executing a Wait for Interrupt (WFI) or Wait for Event (WFE) with the DEEPSLEEP bit set. The system state also depends on the operating modes of the other CPU and the radio system. The CPU1 bus matrix clock is only stopped when the other CPU has no allocated peripherals on the CPU1 clock domain or the other CPU is also in CStop mode. The system may only enter Stop or Standby mode when both the other CPU and the radio system are in CStop mode. The system only enters Standby mode when allowed by both CPUs.

CPU wakeup from cstop

- To determine the system low-power mode when the CPU wakes up from CStop mode, flags are provided.
- Each CPU has its own set of flags
  - CxSTOPF, CxSTOP2F
    - System has woken up from Stop mode
      - Wakeup interrupt to the CPU will be pending in EXTI or peripheral
  - CxSBF
    - System has woken up from Standby mode
      - CPU start from reset.
- The flags of both CPUs must be checked to determine the system operating mode.

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When a CPU wakes up from its CStop mode, it has to know from which mode the system has woken up. For this, the CPU has a few dedicated flag bits SBF, STOPF, and STOP2F. These bits inform the CPU about the state of the system, and which parts of the clock, and peripherals may need to be reinitialized.

Wakeup system mode detection

System mode	C1SBF	C1STOPnF	C2SBF	C2STOPnF	CPU1 wakeup
Run	0	0	x	x	Wakeup from Run
	0	1	0	0	Wakeup from Stop, but system is already in Run due to CPU2.
	1	0	0	0	Wakeup from Standby, but system is already in Run due to CPU2.
	1	1	0	0	Wakeup from Stop, preceded by Standby, but system is already in Run.
Stop	0	1	x	1	Wakeup from Stop. (CPU2 is still in CStop)
	1	1	0	1	Wakeup from Stop, preceded by Standby. (CPU2 is still in CStop)
Standby	1	0	1	0	Wakeup from Standby. (CPU2 is still in CStop)

For example, if CPU1 has selected to enter Stop mode:

- but when it wake up, it reads C1STOPF=0, it means it never entered in System Stop mode, and so there is no need to re-initialize the clocks.
- if it reads C1STOPF=1 and C2STOPF=0, it means that it has entered System Stop but that CPU2 has woken up the system in the mean time and has probably re-initiated clocks.
- Only when both C1STOPF and C2STOPF are set the CPU wakes-up at the same time as the system exit Stop mode. In this case the clocks shall be reinitialized.

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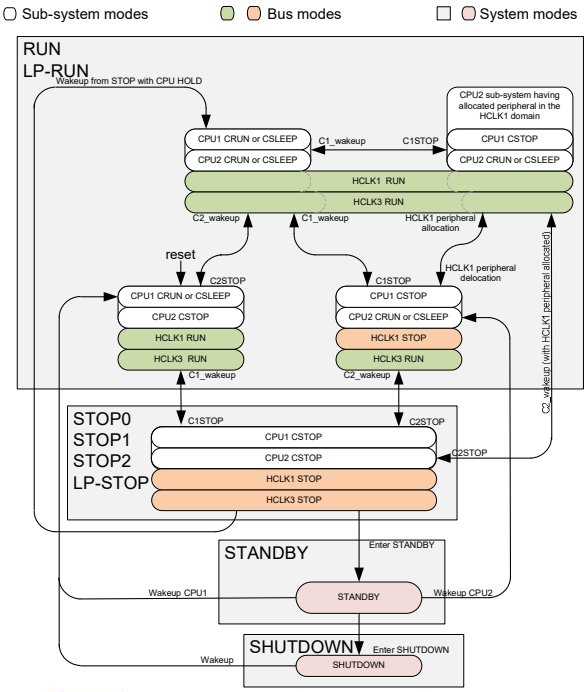
These CxSBF (Standby) and CxSTOPnF (Stop) flags have to be tested by the CPU software when waking up from CStop modes and after CPU reset. They enable the CPU application to selectively reprogram its context (RAM, Peripherals and Clocks).

Power control states



- Power state is controlled from both CPUs.
  - Run modes:
    - At least one CPU is in CRun or Csleep mode
  - Stop modes
    - Both CPUs are in CStop mode and LPMS selects Stop.
  - Standby
    - Both CPUs are in CStop mode and LPMS selects Standby.
  - Shutdown
    - Both CPUs are in CStop mode and LPMS selects Shutdown.
  - From Stop and Standby each sub-system may wake up independently.
  - From Shutdown and Reset, only the CPU1 Cortex-M4 is woken up.

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This figure gives the complete overview of the power modes in relation to the CPUs operating modes. Whenever a CPU is in CRun or CSleep mode, the system is in Run mode. Low-power Stop, Standby and Shutdown modes are only entered when both CPUs are in CStop mode. The low-power mode is selected by the Low-Power Mode Select (LPMS) bits. Each CPU has its own Low-Power Mode select bits and the system enters the highest consuming low power mode selected. From Stop and Standby modes, each sub-system can be woken-up independently by its own enabled wakeup sources. From Shutdown mode and Reset, only the CPU1 Cortex-M4 is woken-up. It is up to the Cortex-M4 application software to wake up the CPU1 Cortex-M0+.
The sub-GHz radio peripheral operation has no impact on the CPUs and system operating mode.

Run and low-power run modes

Flexibility between required performance and consumption

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except the Flash interface clock.
  - SRAM1 and SRAM2 clocks are always ON in Run mode.
- When running from SRAM1 or SRAM2; in Low-power run:
  - Flash memory can be put in Power-down mode (if none of the CPUs are using it)
  - Flash memory clock can be switched off
  - Interrupt vectors must also be re-mapped to SRAM

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Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes. By default, all peripherals clocks are OFF, except the Flash interface clock. The SRAM1 and SRAM2 clocks are always ON in Run mode. When running from SRAM1 or SRAM2 (in Low-power run mode), the Flash memory can be put in Power-down mode thanks to software, and the Flash clock can be switched off. The Flash memory must not be accessed when it is switched off, consequently interrupts must be mapped in SRAM, using the CPU Vector Table Offset Register.

PWR interrupts

Interrupt event	Description	Availability
WKUP[3:1]	External wakeup to GPIO Wakeup pins.	Run, Stop and Standby
PVDO	Programmable Voltage detection via EXTI	Run, Stop and Standby
PVMO[3]	Peripheral Voltage monitoring via EXTI	Run and Stop
CPU2 Hold	CPU1 wakeup to re-initialize system before releasing CPU2	Stop and Standby
sub-GHz radio busy	Start or end of sub-GHz radio busy.	Run, Stop and Standby

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Here is a summary of the PWR control related interrupts.

Run and low-power run modes

Flexibility between required performance and consumption

Voltage range	CPU	HCLK1 HCLK2	MSI	HSI16	PLL
Range 1	CPU1 CPU2	48 MHz max 48 MHz max	48 MHz range	16 MHz	48 MHz VCO max = 344 MHz
Range 2	CPU1 CPU2	16 MHz max 16 MHz max	16 MHz range	16 MHz	16 MHz VCO max = 128 MHz
Low-power run	CPU1 CPU2	2 MHz max 2 MHz max	2 MHz range	Allowed	Not allowed

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The Run mode, thanks to voltage scaling, and the Low-power run modes offer flexibility between required performance and consumption.
In Run mode range 1, the system clock is limited to 48 MHz and the internal and external oscillators and the PLL can be used. In Run mode range 2, the system clock is limited to 16 MHz and the internal and external oscillators as well as the PLL can be used but must be limited to 16 MHz. In Low-power run mode, the system clock must be limited to 2 MHz and the PLL cannot be used.

Sleep and low-power sleep modes

All peripherals available and fastest wakeup time

- Core is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing WFI (Wait For Interrupt) or WFE (Wait For Event)
- Two mechanisms to enter this mode:
  - Sleep Now: MCU enters Sleep mode as soon as WFI/WFE instruction are executed
  - Sleep on Exit: MCU enters Sleep mode as soon as it exits the lowest priority ISR
    - The stack is not popped before entering Sleep mode, it will not be pushed when the next interrupt occurs, saving running time.
  - Controlled by Cortex System Control Register [SLEEPONEXIT]

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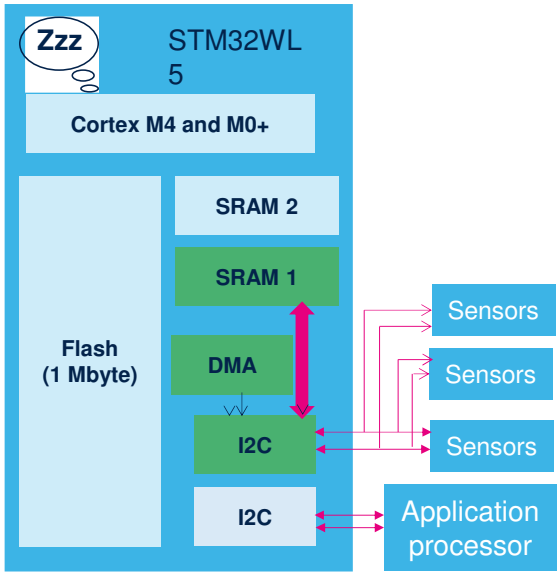
Sleep and Low-power sleep modes allow all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped, and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembler instruction Wait for Interrupt (WFI) or Wait for Event (WFE).
When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the Cortex M4 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine. This last configuration allows you to save time and consumption by saving the need to pop and push the stack.

Batch acquisition mode (BAM)

Optimized mode for transferring data with communication peripherals, while the rest of the device is in low-power mode.

- Only the needed communication peripheral + 1 DMA + SRAM are configured with clock enabled in Sleep mode
- When both CPU are in Sleep mode, the Flash memory is put in Power-down mode and Flash memory clock is gated off during Sleep mode
- Enter either Sleep or Low-power sleep mode
  - Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing 1 MHz Fast-mode Plus support. U(S)ART/LPUART clock can also be HSI16.



Batch Acquisition Mode is an optimized mode for transferring data.
Only the needed communication peripheral + DMA + SRAM1 or SRAM2 are configured with clock enable in Sleep mode.
Flash memory is put in Power-down mode and the Flash memory clock is gated off during Sleep mode.
Then it can enter either Sleep or Low-power sleep mode.
Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing support for 1-MHz Fast-mode Plus.
The USART and LPUART clocks can also be based on the high-speed internal oscillator. Typical applications are sensor hubs.

Stop 0 and 1 modes

Lowest power modes with full retention

- All memory and all peripheral registers are retained
- All high-speed clocks are stopped
  - Except the HSI16 used as kernel clock for peripherals capable of operating in Stop mode.
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup can be HSI16 or MSI up to 48 MHz (1 µs wakeup time on RAM, 5 µs on Flash memory
- Stop 1 consumption is lower, Stop 0 supports more active peripherals.

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STM32WL5 devices features two Stop modes with full retention: Stop 0, and Stop 1, which are the lowest power modes with full retention and fast wakeup time to Run mode at maximum 48 MHz.
The contents of SRAMs and all peripherals registers are preserved in Stop 0 and Stop 1 modes.
All high-speed clocks are stopped, except the ones used as kernel clock for peripherals capable of operating in Stop modes.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up can be the internal high-speed and multi-speed oscillators up to 48 MHz, with only a 1 µs wakeup time from SRAM or 5 µs from Flash memory.
Stop 1 consumption is lower than Stop 0 but supports less active wakeup peripherals.

Stop 2 mode

Low power modes with partial retention

- All memory the CPUs and some peripherals are retained.
  - I2C3, LPTIM1, LPUART, RCC, PWR, GTZC, EXTI, IPCC, IWDG, WWDG, GPIO, CRC, SYSCFG, RTC, and TAMP.
  - Peripherals not retained are to be reinitialized after wakeup from Stop 2 mode.
- All high-speed clocks are stopped
  - Except the HSI16 used as kernel clock for peripherals capable of operating in Stop mode.
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup can be:
  - HSI16 or MSI up to 48 MHz (1 µs wakeup time on RAM, 5 µs on Flash memory
- Stop 1 consumption is lower, Stop 0 supports more active peripherals.

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STM32WL5 devices features one Stop mode with partial retention: Stop 2 mode with partial retention provides still fast wakeup time to Run mode at maximum 48 MHz.
The contents of SRAMs and the CPUs, and some peripherals are preserved in Stop 2 mode.
All high-speed clocks are stopped, except the ones used as kernel clock for peripherals capable of operating in Stop modes.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up can be the internal high-speed and multi-speed oscillators up to 48 MHz, with only a 1 µs wakeup time from SRAM or 5 µs from Flash memory.
Stop 1 consumption is lower than Stop 0 but supports less active wakeup peripherals.

Stop mode comParison

Voltage range	Stop 0	Stop 1	Stop 2
Consumption	25 °C, 3 V		
	TBD µA	TBD µA w/o RTC	TBD µA w/o RTC
Wakeup time to 32 MHz (1)	1.7 µs in Flash memory 2 µs in RAM	4.7 µs in Flash memory 3.4 µs in RAM	5.1 µs in Flash memory 5 µs in RAM
Wakeup clock	MSI configurable up to 48 MHz or HSI16 at 16 MHz		
	Full retention		Partial retention
Regulator	Main regulator	Low power regulator	
Peripherals	RTC, I/Os, BOR, PVD, PVM, IWDG		
	3x LP TIMERs 1x LP UART (Start, address match or byte reception) 2x UART (Start, address match or byte reception) 3x I2C (address match)		1x LP TIMER (LPTIM1) 1x LP UART (LPUART1 Start, address match or byte reception) 1x I2C (I2C3 address match)

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When comparing Stop modes:
Stop 0 mode has the highest consumption as it keeps the Main Regulator ON.
Stop 1 mode consumption is higher than Stop 2 mode consumption, but the wakeup time is shorter, and the number of active peripherals is higher.
Stop 2 mode only provides partial retention including all memories, both CPUs and some peripherals. The following peripherals are not retained and need initialization after wakeup from Stop 2 mode. HSEM, LPTIM2 and 3, I2C1 and 2, USART1 and 2, SPI1, SPI2S2 and SUBGHZSPI, TIM1, 2, 16 and 17, DMA1 and 2 and DMAMUX, ADC , DAC, AES, PKA, true RNG.

The I2C address recognition is functional in all Stop modes and can generate a wakeup event in case of an address match. Only one I2C is supported in Stop2 versus three I2Cs in Stop 0 and Stop 1 modes.

The UART byte reception is functional in all Stop modes and can generate a wakeup event in case of Start detection or Byte reception or Address match event. Only the low-power UART is supported in Stop2 mode. In other Stop modes, all UARTs and the low-power UART can generate a wakeup event.
When clocked by the internal or external low-speed oscillator, or when clocked by an external pin, the low-power timer can wake up the MCU with all its events. In Stop 0 and Stop 1 modes, all low-power timers are supported whereas only LPTIM1 is supported in Stop 2 mode.

Stop hold mode

Allows the CPU1 to re-initialize the clock system.

- When waking up from Stop modes, the clock system is reset.
- The Stop Hold function allows the CPU1 to re-initialize the clock system.
  - A wake-up interrupt to the CPU2 holds the CPU2 and issues a wake-up hold interrupt to the CPU1.
  - The CPU1 after having re-initialized the clock system removes the hold on the CPU2.

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To allow the CPU1 to re-initialize the clock system when exiting from Stop modes, the Stop hold function holds the CPU2 until the CPU1 has re-initialized the system. To ensure this, a wake-up from Stop mode interrupt holds the CPU2 and wakes up the CPU1 with a wake-up hold interrupt. Once the CPU1 has re-initialized the system, it releases the CPU2 hold.

Standby mode

Lowest power mode with SRAM2 retention, switch to V_{BAT} and I/O control

- RTC and backup registers always retained.
- Possibility to retain 32 Kbytes of SRAM2
- Wakeup sources:
  - sub-GHz Radio, PVD, RTC, TAMP, IWDG
  - 3 wakeup pins: the polarity of each of the wakeup pins is configurable
- Ultra Low Power BOR0 always ON: safe reset regardless of VDD slope.
- Configurable pull-up or pull-down or none for each I/O
  - PWR_PUCRx / PWR_PDCRx registers (x = A,B,…H), applied when APC is set in PWR_CxCR3 register
  - => Allows the control of external component inputs state
- Wakeup clock is MSI 4 MHz.

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The Standby mode is the lowest power mode in which 32 Kbytes of SRAM2 can be retained, the automatic switch from V_{DD} to V_{BAT} is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry. By default, the voltage regulators are in Power down mode and the SRAMs and the peripherals registers are lost. The backup registers are always retained.
The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the V_{DD} slope.
Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bits. This allows control of the inputs state of external components even during Standby mode.
Wakeup sources are:

- the sub-GHz radio
- PVD
- RTC, TAMP, IWDG.
- 3 configurable wakeup pins.

The wakeup clock is MSI with a frequency of 4 MHz.

Shutdown mode

Lowest power mode: 30 nA !!

- Similar to Standby but
  - NO power monitoring:
  - NO BOR,
  - NO switch to VBAT
  - NO LSI, NO IWDG, NO SRAM2
  - NO sub-GHz radio
  - BOR0 reset is generated when exiting Shutdown mode
    - => all registers except those in Backup domain are reset.
    - => Calibrated reset pulse generated on the NRST pad
- Wakeup sources:
  - 3 wakeup pins
  - RTC and 3 Tamper
- Wakeup clock is MSI 4 MHz.

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A Shutdown mode is the lowest power mode of the STM32WL5, with only 30 nA at 1.8 V.
This mode is similar to Standby mode but without any power monitoring: the brown-out reset is disabled and the switch to VBAT is not supported in Shutdown mode.
The LSI is not available, and consequently the independent watchdog is also not available. A brown-out reset is generated when the device exits Shutdown mode: all registers are reset except those in the backup domain, and a reset signal is generated on the pad.
The backup registers are retained in Shutdown mode.
The wakeup sources are the 3 wakeup pins and the RTC.
When exiting Shutdown mode, the wakeup clock is MSI at 4 MHz.

VBAT mode

RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator
  - 3 tamper detection pins with time-stamping to detect intrusion
  - backup registers
- If VBAT goes below the VBKUP threshold, the backup domain is reset
- Automatic internal switch between VBAT and VDD when VDD is powered down and powered up.

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The backup domain allows you to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. Three tamper pins are functional in VBAT mode and will erase the backup registers also included in the VBAT domain, in case of intrusion detection.
The backup domain also contains the RTC clock control logic.
In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD .
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery level.
When VDD is present, the battery connected to VBAT can

be charged from the VDD supply.

Power modes summary

Mode	Regulator	Radio	CPU	Flash	SRAM	Clocks	Peripherals
Run	R1	**Yes**	**Yes**	**On**	**On**	Any	All
	R2						All except true RNG
LPRun	LPR	**Yes**	**Yes**	**On**	**On**	Any except PLL	All except true RNG
Sleep	R1	**Yes**	No	**On**	**On**	Any	All
	R2						All except true RNG
LPSleep	LPR	**Yes**	No	**On**(1)	**On**(2)	Any except PLL	All except true RNG
Stop 0	R1/R2	**Yes**	No	Off	**On**	LSE/LSI/HSI16/HSE32	Reset pin, all I/Os BOR,PVD,PVM,RTC,IWDG, USARTx, LPUART,I2Cx,LPTIMx, sub-GHz radio
Stop 1	LPR	**Yes**	No	Off	**On**	LSE/LSI/HSI16/HSE32	Reset pin, all I/Os BOR,PVD,PVM,RTC,IWDG, USARTx, LPUART,I2Cx,LPTIMx, sub-GHz radio
Stop 2	LPR	**Yes**	No	Off	**On**	LSE/LSI/HSI16/HSE32	Reset pin, all I/Os BOR,PVD,PVM,RTC,IWDG, LPUART,I2C3,LPTIM1, sub-GHZ radio
Standby + RAM	LPR	**Yes**	Reset	Off	**SRAM2**	LSE/LSI/HSE32	Reset pin, 3 WKUPx pins BOR, PVD, RTC, IWDG, sub-GHz radio
Standby	OFF	**Yes**			**Off**		
Shutdown	OFF	Reset	Reset	Off	**Off**	LSE	Reset pin, 3 WKUPx pins RTC

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Here you can see the summary of all the STM32WL5 operating modes.

Option bytes

Avoiding entering unwanted low power modes

- 3 option bits can be configured in Flash options bytes to prohibit a given low-power mode:
  - nRST_SHDW: When cleared, a reset is generated when entering Shutdown mode
  - nRST_STDBY: When cleared, a reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a reset is generated when entering any Stop modes

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Three bits are available in the Flash option bytes to prohibit a given low-power mode. When cleared, an option bit configures reset generation when entering Shutdown mode. Another bit configures reset generation when entering Standby mode and the last bit configures reset generation when entering Stop 0, Stop 1 or Stop 2 modes.

Low-power debug information

Keeping the debugger alive while in Low Power modes

- 3 bits in DBGMCU_CR register allows debug in Sleep, Stop, and Standby modes:
  - DBG_SLEEP: When set, HCLK and FCLK remain ON in Sleep and Low-power sleep modes.
  - DBG_STOP: When set, HCLK and FCLK remain ON in Stop modes, and power remains on all logic.
  - DBG_STANDBY: When set, the digital part is not unpowered in Standby mode, and HCLK and FCLK remain ON. In addition, the MCU in under system reset during Standby.
- When those bits are set, the connection with the debugger is kept during the low-power mode. After wake-up, the debug is still possible.

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Three bits are also available in the Debug Control Register for debugging in Sleep, Stop, and Standby mode. When the related bit is set, the power is kept on all logic in Standby and Stop 2 mode, and the HCLK and FCLK clocks remain ON to keep the debugger active. This maintains the connection with the debugger during the low-power modes and continues debugging after wake-up. Remember to clear these bits when the MCU is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the clocks and the regulators to remain enabled.

Related peripherals

- Refer to the following list of peripherals training for more details of their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Interrupts (NVIC, EXTI)
  - Comparator (COMP)
  - Low-power timer (LPTIM)
  - Independent watchdog (IWDG)
  - Real-time clock (RTC)
  - Inter-integrated circuit (I2C) interface
  - Universal synchronous asynchronous receiver transmitter (USART)
  - Low-power universal asynchronous receiver transmitter (LPUART)

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In addition to this training, you can refer to the Reset and Clock Control, Interrupts trainings as well as those for all the peripherals with wakeup from Stop and Standby capability.