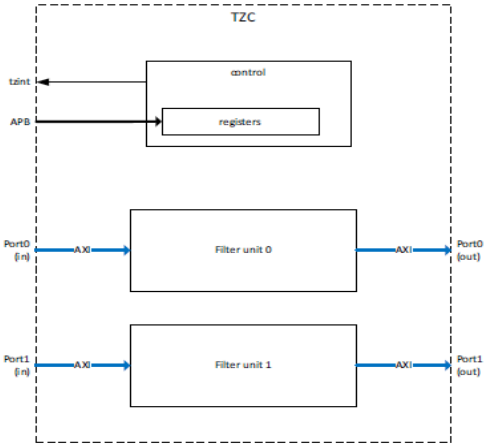
Hello, and welcome to this presentation of the STM32MP1 TrustZone Address Space Controller.

Overview

- TZC is intended to filter DDR read and write accesses according to TrustZone® security controls and NSAID (Non-Secure master Address ID) as defined by Programmable Regions.
- TZC contains 2 filters (one per AXI port)



On STM32MP13x lines there is only 1 AXI Port so only 1 TZPC port and 1 filter

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The TrustZone® Address Space Controller (TZC) is intended to filter DDR accesses according to security rules and non-secure master address ID.
This is a simplified diagram of TZC.
TZC is composed of two filter units, one per AXI port. The filters work concurrently.
The two filters are controlled by a common control register set via the APB interface.

Key Features (1/2)

- 2 filter units working concurrently
- 9 regions:
  - Region 0 is always enabled and covers the whole DDR address range
  - Regions 1 to 8 have programmable start/end addresses with a 4KByte granularity and can be assigned to one or both filters.
- Secure and non-secure access permissions are programmed per region
- Non-secure accesses are filtered according to the non-secure master address ID (NSAID)
- Regions controlled by the same filter must not overlap

On STM32MP13x lines there is only 1 AXI Port so only 1 TZPC port and 1 filter

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TZC is composed of 2 filter units working concurrently on two AXI ports.

Access filtering can support up to 9 regions:

- Region 0 is always enabled and covers the whole DDR address range
- Regions 1 to 8 have programmable start and end addresses with a 4 KByte granularity. A region can be assigned to one or both filters.

Secure and non-secure access permissions are defined per region.

Non-secure accesses are filtered according to the non-secure master address ID.

Regions controlled by the same filter must not overlap.

Key Features (2/2)

- Failed permission checks may be signaled with an AXI Bus error and/or interrupt
- 32-bit APB4 Interface
- TZC configuration is supported by secure masters only
- Read access path supports up to 256 outstanding transactions
- Gate keeper logic can enable and disable each filter
- Supports speculative access

Note: TZC has 2 cycle latency, Fast path (FPID) with reduced outstanding capability is not supported in the STM32MP1 series

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Failed permission checks can be signaled either with an AXI Bus error or with interrupt or both.

TZC is programmed via a 32-bit APB4 Interface.

TZC configuration is supported by secure masters only.

Read-access path supports up to 256 outstanding transactions to DDR.

Some Gate keeper logic is used to enable and disable each filter.

TZC can support speculative accesses.

Note: TZC has 2 cycle latency. Fast path (FPID) with reduced outstanding capability is not supported in the STM32MP1 series.

Programming Guidelines

- Region 0 is the base region, it is covering the full address range and is always enabled.
- Region 0 can be used to catch any access outside Regions 1 to 8.
- Regions 1 to 8 must not overlap each other when assigned to the same filter
- Semi Static programming, need to block all accesses (Gate) before reprograming filter settings.
- TZC supports independent Read and Write settings
- Secure and Non secure settings are independent, however secure check is applicable to any master, while non secure check is filtered per master (NSAID selective)

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TZC programming should observe the following guidelines:

- Region 0 is the base region covering the full address range and is always enabled.
- Region 0 can be used to catch any access outside Regions 1 to 8.
- Regions 1 to 8 must not overlap when assigned to the same filter.
- In case of reconfiguration by Semi Static programming, all accesses (Gate) must be blocked before reprograming filter settings.

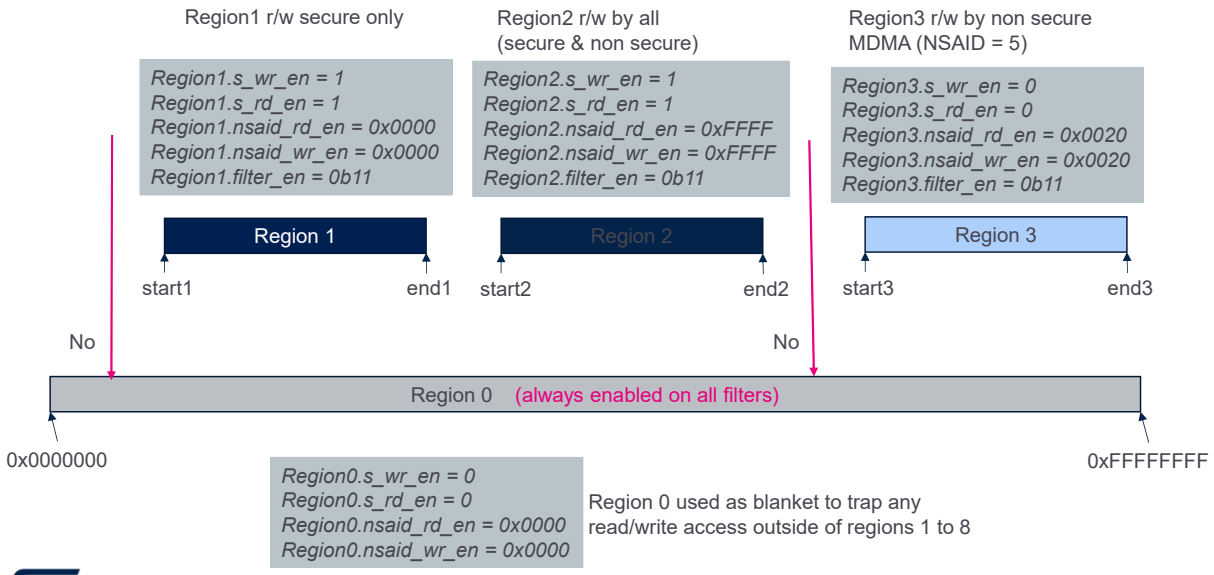
TZC access filtering is based on:

- Independent Read and Write settings (read-only, write-

only, read-write, and no access)

- Secure and Non-secure settings are independent, however secure check is applicable to any master, but non-secure check is filtered per master (NSAID selective).

Programming example



This slide shows an example of simple programming.
The DDR space supports 3 non-overlapping regions.

- Region 1 is defined between the start1 and end1 addresses. Region 1 is read- and write-accessible only by secure applications.
- Region 2 is defined between the start2 and end2 addresses. Region 2 is a shared region, read- and write-accessible by secure and non-secure applications.
- And Region 3 is defined between the start3 and end3 addresses. Region 3 is read- and write-accessible only by the non-secure MDMA engine (with NSAID=5).

The register settings and programming sequence are for wr_en and rd_en parameters. NSAIDs are listed in the table in the next slide.

Region 0 is always enabled and covers the full DDR address space. It is set as a blanket to trap any access outside of

these regions.
Hence no access is allowed outside of the 3 defined regions.

NSAID table

STM32MP15x lines	
MasterUSBH (EHCI)	NSAID[0:3]
CA7	0b0000
CM4	0b0001
LTDC	0b0011
GPU	0b0100
MDMA	0b0101
DMA 1/2	0b0110
USBH (EHCI/OHCI)	0b0111
OTG	0b1000
SDMMC 1/2/3	0b1001
ETH 1	0b1010
DAP	0b1111

STM32MP13x lines	
MasterUSBH (EHCI)	NSAID[0:3]
CA7	0b0000
-	-
LTDC	0b0011
DCMIPP	0b0100
MDMA	0b0101
DMA 1/2/3	0b0110
USBH (EHCI/OHCI)	0b0111
OTG	0b1000
SDMMC 1/2	0b1001
ETH 1/2	0b1010
DAP	0b1111

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Non-secure master address ID (NSAID) is encoded on 4 bits according to Master as listed in this table.

Thank you

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